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EEPROM Serial 4 kB I²C

CAS24C04

Description

The CAS24C04 is a 4-Kb I²C Serial EEPROM device organized internally as 32 pages of 16 bytes each. The device supports both the Standard (100 kHz) as well as Fast (400 kHz) I²C protocol.

Data is written by providing a starting address, then loading 1 to 16 contiguous bytes into a Page Write Buffer, and then writing all data to non-volatile memory in one internal write cycle. Data is read by providing a starting address and then shifting out data serially while automatically incrementing the internal address count.

External address pins make it possible to address up to four CAS24C04 devices on the same bus.

Features

- Supports Standard and Fast I²C Protocol
- 1.7 V to 5.5 V Supply Voltage Range
- 16-Byte Page Write Buffer
- Hardware Write Protection for Entire Memory
- Schmitt Triggers and Noise Suppression Filters on I²C Bus Inputs (SCL and SDA)
- Low power CMOS Technology
- More than 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Industrial and Extended Temperature Range
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



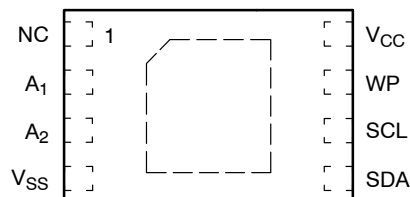
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**UDFN8-EP
HU4 SUFFIX
CASE 517AZ**

PIN ASSIGNMENT



UDFN-EP (HU4) (Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

CAS24C04

PIN CONFIGURATIONS AND MARKING INFORMATION

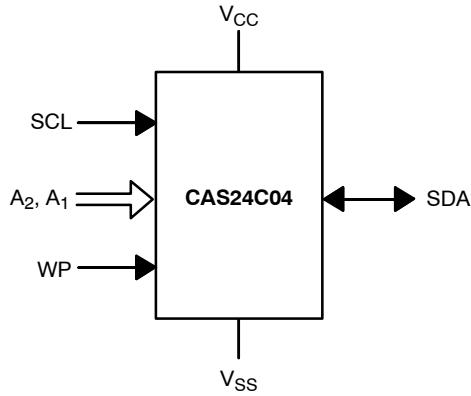


Figure 1. Functional Symbol

Table 1. PIN FUNCTION

Pin Name†	Function
A1, A2	Device Address Input
SDA	Serial Data Input/Output
SCL	Serial Clock Input
WP	Write Protect Input
V _{CC}	Power Supply
V _{SS}	Ground
NC	No Connect

† The exposed pad for the UDFN packages can be left floating or connected to Ground.

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
Storage Temperature	-65 to +150	°C
Voltage on any pin with respect to Ground (Note 1)	-0.5 to +6.5	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- During input transitions, voltage undershoot on any pin should not exceed -1 V for more than 20 ns. Voltage overshoot on pins A₀, A₁, A₂ and WP should not exceed V_{CC} + 1 V for more than 20 ns, while voltage on the I²C bus pins, SCL and SDA, should not exceed the absolute maximum ratings, irrespective of V_{CC}.

Table 3. RELIABILITY CHARACTERISTICS (Note 2)

Symbol	Parameter	Min	Units
N _{END} (Note 3)	Endurance	1,000,000	Program / Erase Cycles
T _{DR}	Data Retention	100	Years

- These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.
- Page Mode, V_{CC} = 5 V, 25°C.

Table 4. D.C. OPERATING CHARACTERISTICS

(V_{CC} = 1.8 V to 5.5 V, T_A = -40°C to +125°C and V_{CC} = 1.7 V to 5.5 V, T_A = -40°C to +85°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions		Min	Max	Units
V _{CC}	Supply Voltage	T _A = -40°C to +85°C		1.7	5.5	V
I _{CCR}	Read Current	Read, f _{SCL} = 400 kHz			1	mA
I _{CCW}	Write Current	Write, f _{SCL} = 400 kHz			2	mA
I _{SB}	Standby Current	All I/O Pins at GND or V _{CC}	T _A = -40°C to +85°C V _{CC} ≤ 3.3 V		1	μA
			T _A = -40°C to +85°C V _{CC} > 3.3 V		3	
			T _A = -40°C to +125°C		5	
I _L	I/O Pin Leakage	Pin at GND or V _{CC}			2	μA
V _{IL}	Input Low Voltage			-0.5	0.3 x V _{CC}	V
V _{IH}	Input High Voltage	A ₀ , A ₁ , A ₂ and WP		0.7 x V _{CC}	V _{CC} + 0.5	V
		SCL and SDA		0.7 x V _{CC}	5.5	
V _{OL}	Output Low Voltage	V _{CC} > 2.5 V, I _{OL} = 3 mA			0.4	
		V _{CC} < 2.5 V, I _{OL} = 1 mA			0.2	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 5. PIN IMPEDANCE CHARACTERISTICS(V_{CC} = 1.8 V to 5.5 V, T_A = -40°C to +125°C and V_{CC} = 1.7 V to 5.5 V, T_A = -40°C to +85°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Max	Units
C _{IN} (Note 4)	SDA Pin Capacitance	V _{IN} = 0 V, f = 1.0 MHz, V _{CC} = 5.0 V	8	pF
	Other Pins		6	pF
I _{WP} (Note 5)	WP Input Current	V _{IN} < V _{IH} , V _{CC} = 5.5 V	130	μA
		V _{IN} < V _{IH} , V _{CC} = 3.3 V	120	
		V _{IN} < V _{IH} , V _{CC} = 1.7 V	80	
		V _{IN} > V _{IH}	2	
I _A (Note 5)	Address Input Current (A0, A1, A2)	V _{IN} < V _{IH} , V _{CC} = 5.5 V	50	μA
		V _{IN} < V _{IH} , V _{CC} = 3.3 V	35	
		V _{IN} < V _{IH} , V _{CC} = 1.7 V	25	
		V _{IN} > V _{IH}	2	

4. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.
5. When not driven, the WP, A0, A1 and A2 pins are pulled down to GND internally. For improved noise immunity, the internal pull-down is relatively strong; therefore the external driver must be able to supply the pull-down current when attempting to drive the input HIGH. To conserve power, as the input level exceeds the trip point of the CMOS input buffer (~ 0.5 x V_{CC}), the strong pull-down reverts to a weak current source.

Table 6. A.C. CHARACTERISTICS(Note 6) (V_{CC} = 1.8 V to 5.5 V, T_A = -40°C to +125°C and V_{CC} = 1.7 V to 5.5 V, T_A = -40°C to +85°C, unless otherwise specified.)

Symbol	Parameter	Standard		Fast		Units
		Min	Max	Min	Max	
F _{SCL}	Clock Frequency		100		400	kHz
t _{HD:STA}	START Condition Hold Time	4		0.6		μs
t _{LOW}	Low Period of SCL Clock	4.7		1.3		μs
t _{HIGH}	High Period of SCL Clock	4		0.6		μs
t _{SU:STA}	START Condition Setup Time	4.7		0.6		μs
t _{HD:DAT}	Data In Hold Time	0		0		μs
t _{SU:DAT}	Data In Setup Time	250		100		ns
t _R	SDA and SCL Rise Time		1000		300	ns
t _F (Note 6)	SDA and SCL Fall Time		300		300	ns
t _{SU:STO}	STOP Condition Setup Time	4		0.6		μs
t _{BUF}	Bus Free Time Between STOP and START	4.7		1.3		μs
t _{AA}	SCL Low to Data Out Valid		3.5		0.9	μs
t _{DH}	Data Out Hold Time	100		100		ns
T _i (Note 6)	Noise Pulse Filtered at SCL and SDA Inputs		100		100	ns
t _{SU:WP}	WP Setup Time	0		0		μs
t _{HD:WP}	WP Hold Time	2.5		2.5		μs
t _{WR}	Write Cycle Time		5		5	ms
t _{PU} (Notes 7, 8)	Power-up to Ready Mode		1		1	ms

6. Test conditions according to "AC Test Conditions" table.
7. Tested initially and after a design or process change that affects this parameter.
8. t_{PU} is the delay between the time V_{CC} is stable and the device is ready to accept commands.

Table 7. A.C. TEST CONDITIONS

Input Drive Levels	$0.2 \times V_{CC}$ to $0.8 \times V_{CC}$
Input Rise and Fall Time	≤ 50 ns
Input Reference Levels	$0.3 \times V_{CC}$, $0.7 \times V_{CC}$
Output Reference Level	$0.5 \times V_{CC}$
Output Test Load	Current Source $I_{OL} = 3$ mA ($V_{CC} \geq 2.5$ V); $I_{OL} = 1$ mA ($V_{CC} < 2.5$ V); $C_L = 100$ pF

Power-On Reset (POR)

Each CAS24C04 incorporates Power-On Reset (POR) circuitry which protects the internal logic against powering up in the wrong state.

A CAS24C04 device will power up into Standby mode after V_{CC} exceeds the POR trigger level and will power down into Reset mode when V_{CC} drops below the POR trigger level. This bi-directional POR feature protects the device against 'brown-out' failure following a temporary loss of power.

Pin Description

SCL: The Serial Clock input pin accepts the Serial Clock generated by the Master.

SDA: The Serial Data I/O pin receives input data and transmits data stored in EEPROM. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.

A0, A1 and A2: The Address inputs set the device address when cascading multiple devices. When not driven, these pins are pulled LOW internally.

WP: The Write Protect input pin inhibits all write operations, when pulled HIGH. When not driven, this pin is pulled LOW internally.

Functional Description

The CAS24C04 supports the Inter-Integrated Circuit (I^2C) Bus data transmission protocol, which defines a device that sends data to the bus as a transmitter and a device receiving data as a receiver. Data flow is controlled by a Master device, which generates the serial clock and all START and STOP conditions. The CAS24C04 acts as a Slave device. Master and Slave alternate as either transmitter or receiver.

I^2C Bus Protocol

The I^2C bus consists of two 'wires', SCL and SDA. The two wires are connected to the V_{CC} supply via pull-up resistors. Master and Slave devices connect to the 2-wire bus via their respective SCL and SDA pins. The transmitting device pulls down the SDA line to 'transmit' a '0' and releases it to 'transmit' a '1'.

Data transfer may be initiated only when the bus is not busy (see AC Characteristics).

During data transfer, the SDA line must remain stable while the SCL line is high. An SDA transition while SCL is

high will be interpreted as a START or STOP condition (Figure 2). The START condition precedes all commands. It consists of a HIGH to LOW transition on SDA while SCL is HIGH. The START acts as a 'wake-up' call to all receivers. Absent a START, a Slave will not respond to commands. The STOP condition completes all commands. It consists of a LOW to HIGH transition on SDA while SCL is HIGH.

NOTE: The I/O pins of CAS24C04 do not obstruct the SCL and SDA lines if the VCC supply is switched off. During power-up, the SCL and SDA pins (connected with pull-up resistors to VCC) will follow the VCC monotonically from VSS (0 V) to nominal VCC value, regardless of pull-up resistor value. The delta between the VCC and the instantaneous voltage levels during power ramping will be determined by the relation between bus time constant (determined by pull-up resistance and bus capacitance) and actual VCC ramp rate.

Device Addressing

The Master initiates data transfer by creating a START condition on the bus. The Master then broadcasts an 8-bit serial Slave address. For normal Read/Write operations, the first 4 bits of the Slave address are fixed at 1010 (Ah). The next 3 bits are used as programmable address bits when cascading multiple devices and/or as internal address bits. The last bit of the slave address, R/W, specifies whether a Read (1) or Write (0) operation is to be performed. The 3 address space extension bits are assigned as illustrated in Figure 3. A₂, A₁ and A₀ must match the state of the external address pins, and a₁₀, a₉ and a₈ are internal address bits.

Acknowledge

After processing the Slave address, the Slave responds with an acknowledge (ACK) by pulling down the SDA line during the 9th clock cycle (Figure 4). The Slave will also acknowledge the address byte and every data byte presented in Write mode. In Read mode the Slave shifts out a data byte, and then releases the SDA line during the 9th clock cycle. As long as the Master acknowledges the data, the Slave will continue transmitting. The Master terminates the session by not acknowledging the last data byte (NoACK) and by issuing a STOP condition. Bus timing is illustrated in Figure 5.

CAS24C04

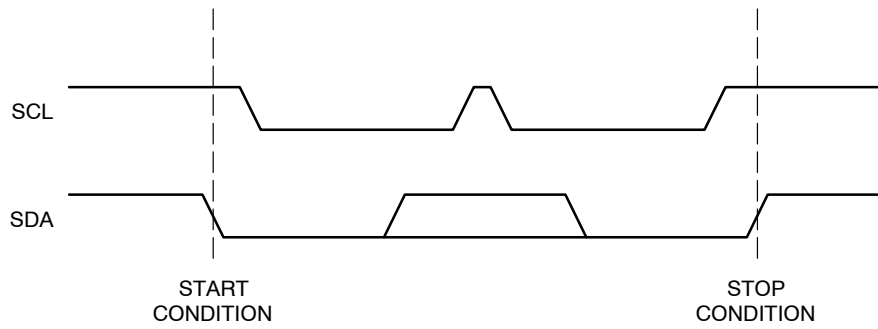


Figure 2. Start/Stop Timing

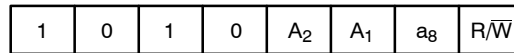


Figure 3. Slave Address Bits

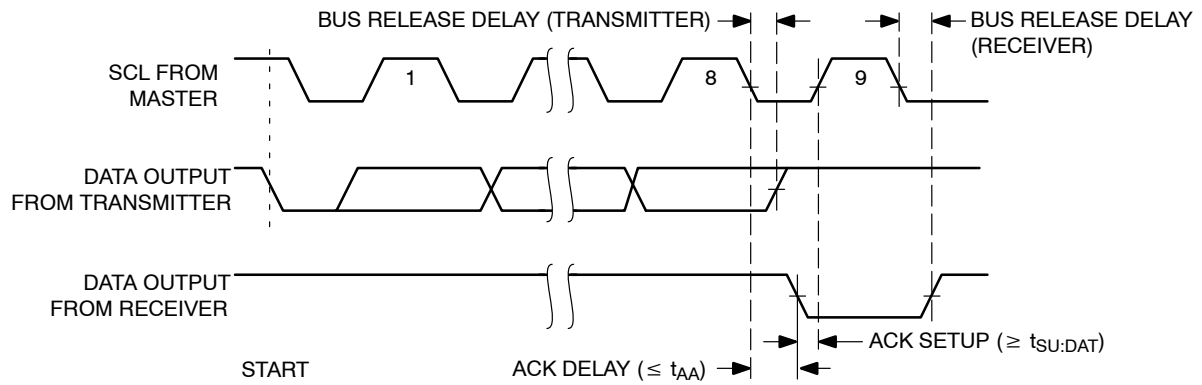


Figure 4. Acknowledge Timing

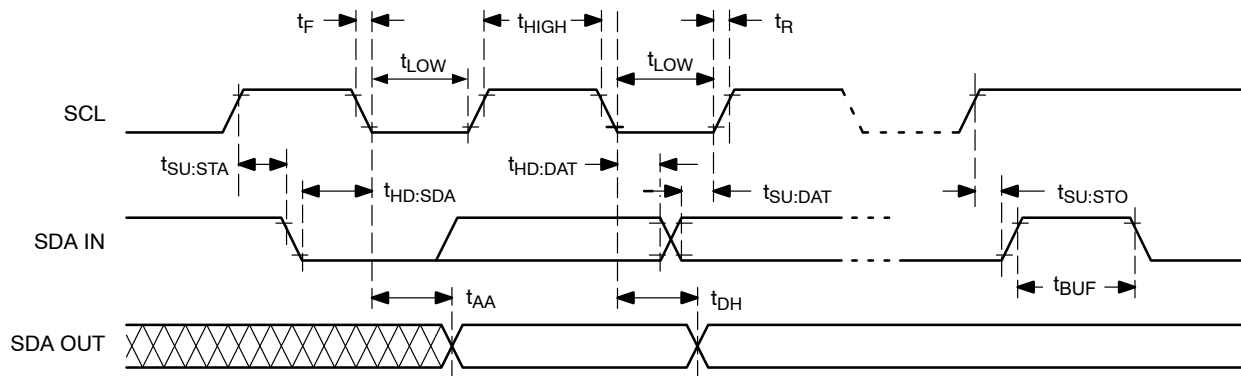


Figure 5. Bus Timing

WRITE OPERATIONS

Byte Write

In Byte Write mode, the Master sends the START condition and the Slave address with the R/W bit set to zero to the Slave. After the Slave generates an acknowledge, the Master sends the byte address that is to be written into the address pointer of the CAS24C04. After receiving another acknowledge from the Slave, the Master transmits the data byte to be written into the addressed memory location. The CAS24C04 device will acknowledge the data byte and the Master generates the STOP condition, at which time the device begins its internal Write cycle to nonvolatile memory (Figure 6). While this internal cycle is in progress (t_{WR}), the SDA output will be tri-stated and the CAS24C04 will not respond to any request from the Master device (Figure 7).

Page Write

The CAS24C04 writes up to 16 bytes of data in a single write cycle, using the Page Write operation (Figure 8). The Page Write operation is initiated in the same manner as the Byte Write operation, however instead of terminating after the data byte is transmitted, the Master is allowed to send up to fifteen additional bytes. After each byte has been transmitted the CAS24C04 will respond with an acknowledge and internally increments the four low order address bits. The high order bits that define the page address remain unchanged. If the Master transmits more than sixteen bytes prior to sending the STOP condition, the address counter 'wraps around' to the beginning of page and previously transmitted data will be overwritten. Once all

sixteen bytes are received and the STOP condition has been sent by the Master, the internal Write cycle begins. At this point all received data is written to the CAS24C04 in a single write cycle.

Acknowledge Polling

The acknowledge (ACK) polling routine can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write operation, the CAS24C04 initiates the internal write cycle. The ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the CAS24C04 is still busy with the write operation, NoACK will be returned. If the CAS24C04 has completed the internal write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

Hardware Write Protection

With the WP pin held HIGH, the entire memory is protected against Write operations. If the WP pin is left floating or is grounded, it has no impact on the operation of the CAS24C04. The state of the WP pin is strobed on the last falling edge of SCL immediately preceding the first data byte (Figure 9). If the WP pin is HIGH during the strobe interval, the CAS24C04 will not acknowledge the data byte and the Write request will be rejected.

Delivery State

The CAS24C04 is shipped erased, i.e., all bytes are FFh.

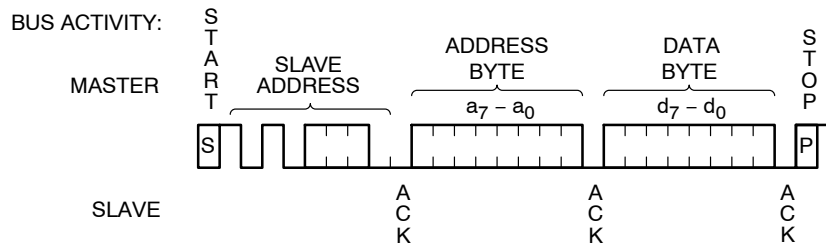


Figure 6. Byte Write Sequence

CAS24C04

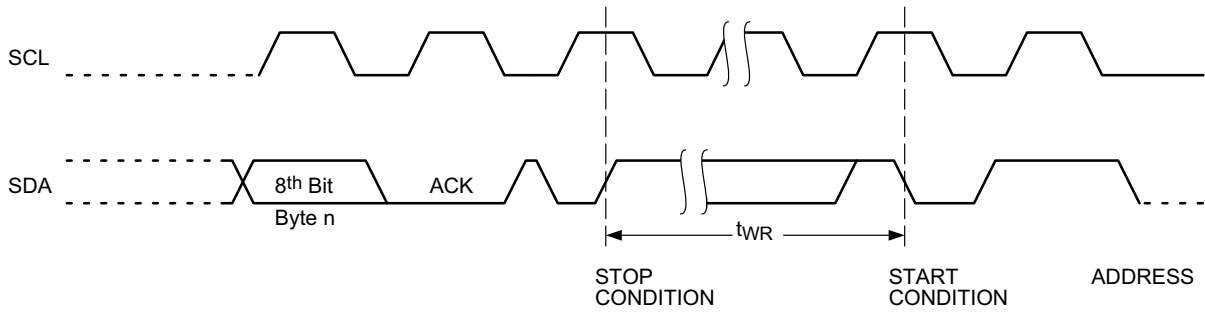


Figure 7. Write Cycle Timing

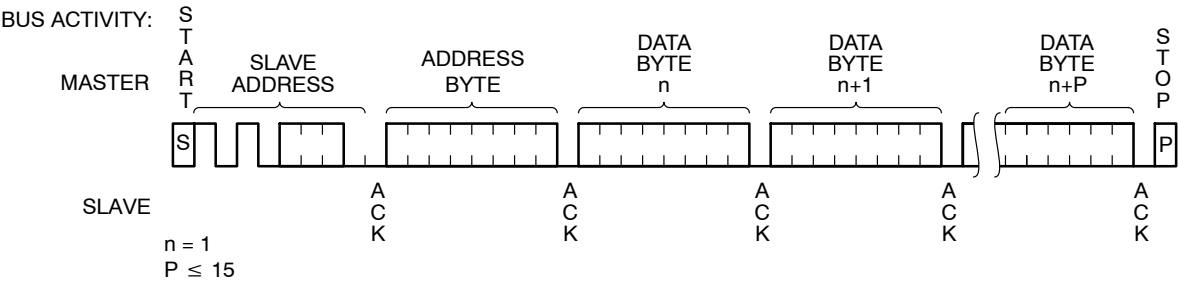


Figure 8. Page Write Sequence

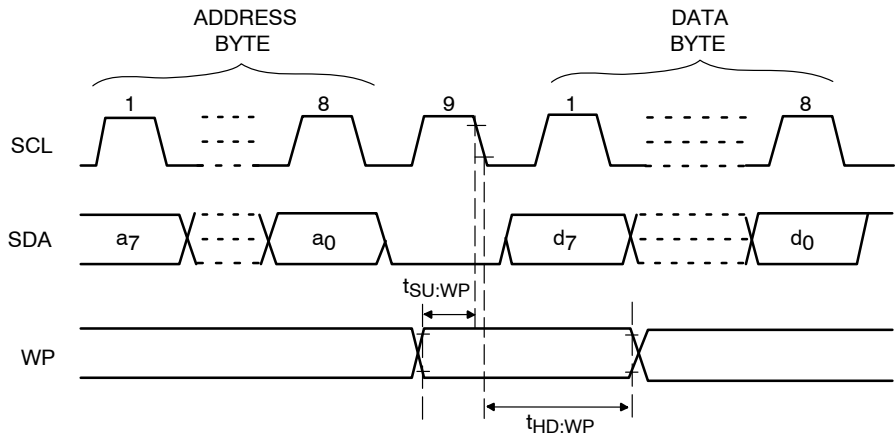


Figure 9. WP Timing

READ OPERATIONS

Immediate Read

Upon receiving a Slave address with the R/W bit set to '1', the CAS24C04 will interpret this as a request for data residing at the current byte address in memory. The CAS24C04 will acknowledge the Slave address, will immediately shift out the data residing at the current address, and will then wait for the Master to respond. If the Master does not acknowledge the data (NoACK) and then follows up with a STOP condition (Figure 10), the CAS24C04 returns to Standby mode.

Selective Read

Selective Read operations allow the Master device to select at random any memory location for a read operation. The Master device first performs a 'dummy' write operation by sending the START condition, slave address and byte

address of the location it wishes to read. After the CAS24C04 acknowledges the byte address, the Master device resends the START condition and the slave address, this time with the R/W bit set to one. The CAS24C04 then responds with its acknowledge and sends the requested data byte. The Master device does not acknowledge the data (NoACK) but will generate a STOP condition (Figure 11).

Sequential Read

If during a Read session, the Master acknowledges the 1st data byte, then the CAS24C04 will continue transmitting data residing at subsequent locations until the Master responds with a NoACK, followed by a STOP (Figure 12). In contrast to Page Write, during Sequential Read the address count will automatically increment to and then wrap-around at end of memory (rather than end of page).

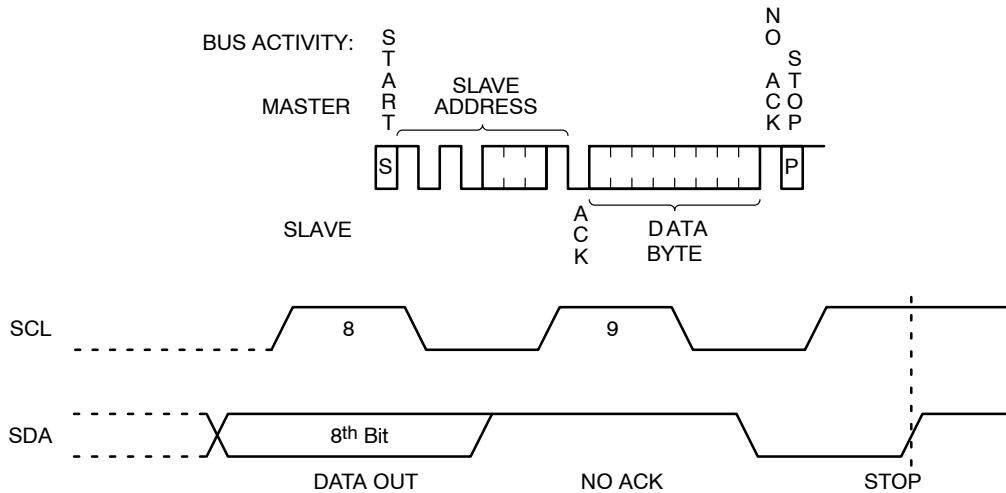


Figure 10. Immediate Read Sequence and Timing

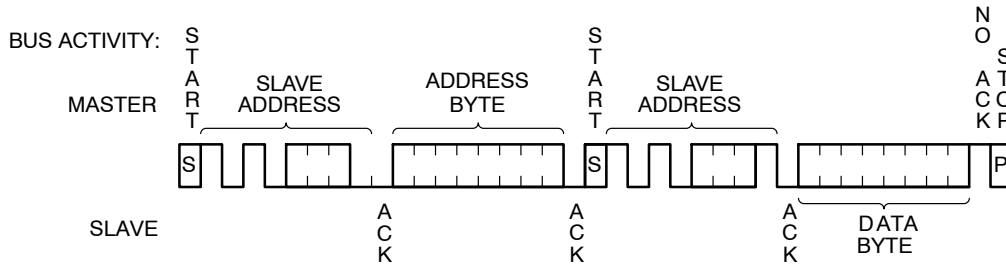


Figure 11. Selective Read Sequence

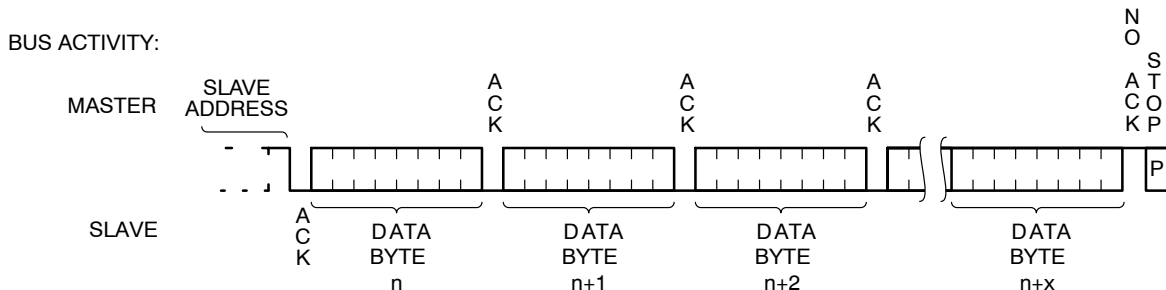


Figure 12. Sequential Read Sequence

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Ordering Information

CAS24C04 Ordering Information

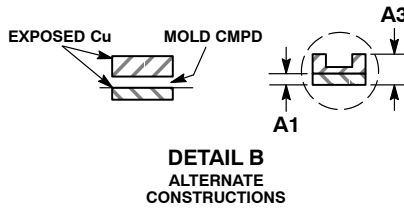
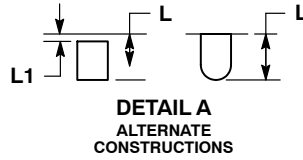
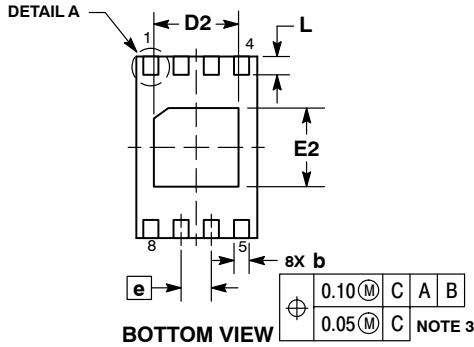
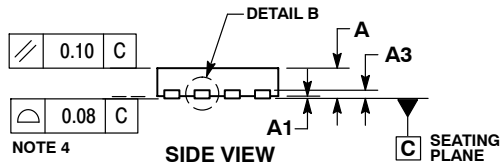
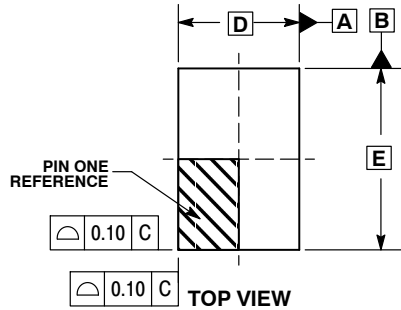
Device Order Number	Specific Device Marking	Package Type	Temperature Range	Lead Finish	Shipping†
CAS24C04HU4I-GT3	S2U	UDFN8-EP	-40 to 125°C	NiPdAu	Tape & Reel, 3,000 Units / Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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PACKAGE DIMENSIONS

UDFN8, 2x3 EXTENDED PAD CASE 517AZ ISSUE A

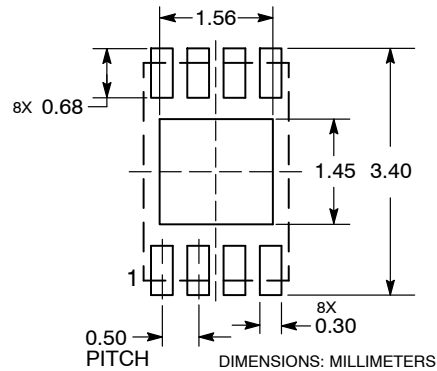


NOTES:


1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13	REF
b	0.20	0.30
D	2.00	BSC
D2	1.35	1.45
E	3.00	BSC
E2	1.25	1.35
e	0.50	BSC
L	0.25	0.35
L1	---	0.15

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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