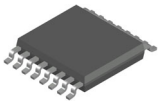
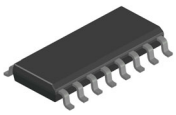
Dual 2-to-4 Decoder/Demultiplexer

74VHC139



TSSOP−16,
CASE 948AH



SOIC−16,
CASE 751BG

General Description

The VHC139 is an advanced high speed CMOS Dual 2−to−4 Decoder/Demultiplexer fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

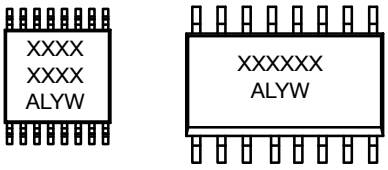
The active LOW enable input can be used for gating or it can be used as a data input for demultiplexing applications. When the enable input is held HIGH, all four outputs are fixed at a HIGH logic level independent of the other inputs. An input protection circuit ensures that 0 V to 5.5 V can be applied to the input pins without regard to the supply voltage.

This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

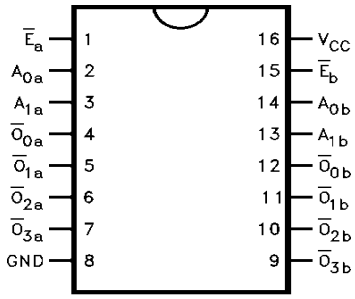
- High Speed: t_{PD} = 5.0 ns (typ.) at T_A = 25°C
- Low Power Dissipation: I_{CC} = 4 μA (Max.) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min.)
- Power Down Protection is Provided on All Inputs
- Pin and Function Compatible with 74HC139
- Pb−Free, Halogen Free/BFR Free and RoHS Compliant

MARKING DIAGRAM



XXXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW,W = Work Week

CONNECTION DIAGRAM



TRUTH TABLE

Inputs			Outputs			
$\overline{E}$	A_0	A_1	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

PIN DESCRIPTION

Pin Names	Description
A_0, A_1	Address Inputs
$\overline{E}$	Enable Inputs
$\overline{O}_0$−$\overline{O}_3$	Enable Inputs

ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Ratings	Unit
V_{CC}	DC Supply Voltage		−0.5 to + 6.5	V
V_I	DC Input Voltage		−0.5 to + 6.5	V
V_{OUT}	DC Output Voltage		−0.5 V to V_{CC} + 0.5	V
I_{IN}	DC Input Current, Per pin		±20	mA
I_{OUT}	DC Output Current, Per pin		±25	mA
I_{CC}	DC Supply Current Current, V_{CC} and GND Per pins		±75	mA
I_{IK}	Input Clamp Current		−20	mA
I_{OK}	Output Clamp Current		±20	°C
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 secs		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 2)	SOIC−16 QFN16 TSSOP−16	126 118 159	°CW
P_D	Power Dissiption in Still Air at 25°C	SOIC−16 QFN16 TSSOP−16	995 1062 787	mW
MSL	Moisture Sensitivity		Level 1	−
F_R	Flammability Rating (Note 2)	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.139 in	−
V_{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model	2000 N/A	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri−stated.
2. Measured with minimum pad spacing on an FR4 board, using 76mm−by−114mm, 2−ounce copper trace no air flow per JESD51−7.
3. HBM tested to EIA / JESD22−A114−A. CDM tested to JESD22−C101−A. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS (Note 3)

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{IN}	DC Input Voltage (Note 4)		0	5.5	V
V_{OUT}	DC Output Voltage (Note 4)		0	V_{CC}	V
T_A	Operating Temperature		−40	+85	°C
t_r,t_f	Input Rise or Fall Rate	V_{CC} = 3.0 V to 3.6 V V_{CC} = 4.5 V to 5.5 V	0 0	100 20	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions		V_{CC} (V)	T_A = 25°C			T_A = −40°C to +85°C		Unit
					Min	Typ	Max	Min	Max	
V_{IH}	HIGH Level Input Voltage			2.0	1.50	–	–	1.50	–	V
				3.0–5.5	0.7 V_{CC}	–	–	0.7 V_{CC}	–	
V_{IL}	LOW Level Input Voltage			2.0	–	–	0.50	–	0.50	V
				3.0–5.5	–	–	0.3 V_{CC}	–	0.3 V_{CC}	
V_{OH}	HIGH Level Output Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA	2.0	1.9	2.0	–	1.9	–	V
				3.0	2.9	3.0	–	2.9	–	
				4.5	4.4	4.5	–	4.4	–	
			I_{OH} = −4 mA	3.0	2.58	–	–	2.48	–	
			I_{OH} = −8 mA	4.5	3.94	–	–	3.80	–	
V_{OL}	LOW Level Output Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	2.0	–	0.0	0.1	–	0.1	V
				3.0	–	0.0	0.1	–	0.1	
				4.5	–	0.0	0.1	–	0.1	
			I_{OL} = 4 mA	3.0	–	–	0.36	–	0.44	
			I_{OL} = 8 mA	4.5	–	–	0.36	–	0.44	
I_{IN}	Input Leakage Current	V_{IN} = 5.5 V or GND		0–5.5	–	–	±0.1	–	±1.0	μA
I_{CC}	Quiescent Supply Current	V_{IN} = V_{CC} or GND		5.5	–	–	40.0	–	40.0	μA

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = 25°C			T_A = −40°C to +85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	C_L = 15 pF	3.3 ±0.3	–	7.2	11.0	1.0	13.0	ns
		C_L = 50 pF		–	9.7	14.5	1.0	16.5	
t_{PHL}	A_n to $\overline{O}_n$	C_L = 15 pF	5.0 ±0.5	–	5.0	7.2	1.0	8.5	ns
		C_L = 50 pF		–	6.5	9.2	1.0	10.5	
t_{PLH}	Propagation Delay	C_L = 15 pF	3.3 ±0.3	–	6.4	9.2	1.0	11.0	ns
		C_L = 50 pF		–	8.9	12.7	1.0	14.5	
t_{PHL}	$\overline{E}_n$ to $\overline{O}_n$	C_L = 15 pF	5.0 ±0.5	–	4.4	6.3	1.0	7.5	ns
		C_L = 50 pF		–	5.9	8.3	1.0	9.5	
C_{IN}	Input Capacitance	V_{CC} = Open	–	–	4	10	–	10	pF
C_{PD}	Power Dissipation Capacitance	(Note 3)	–	–	26	–	–	–	pF

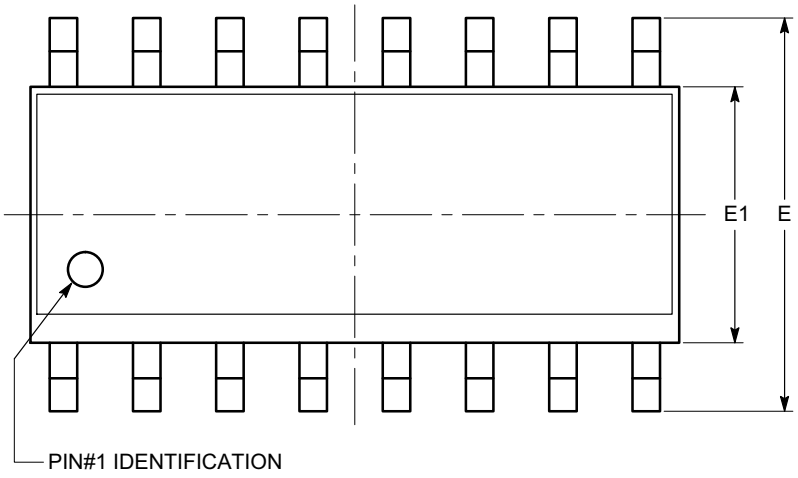
ORDERING INFORMATION

Device	Marking	Package	Shipping†
74VHC139MX	VHC139	SOIC−16	2,500 Units / Tape & Reel
74VHC139MTCX	VHC 139	TSSOP−16	2,500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

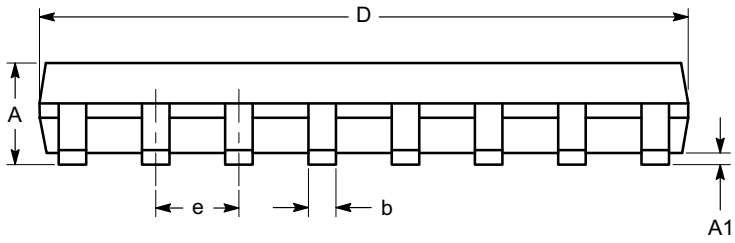
SOIC−16, 150 mils
CASE 751BG
ISSUE O

DATE 19 DEC 2008

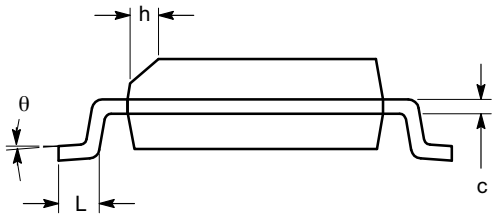


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

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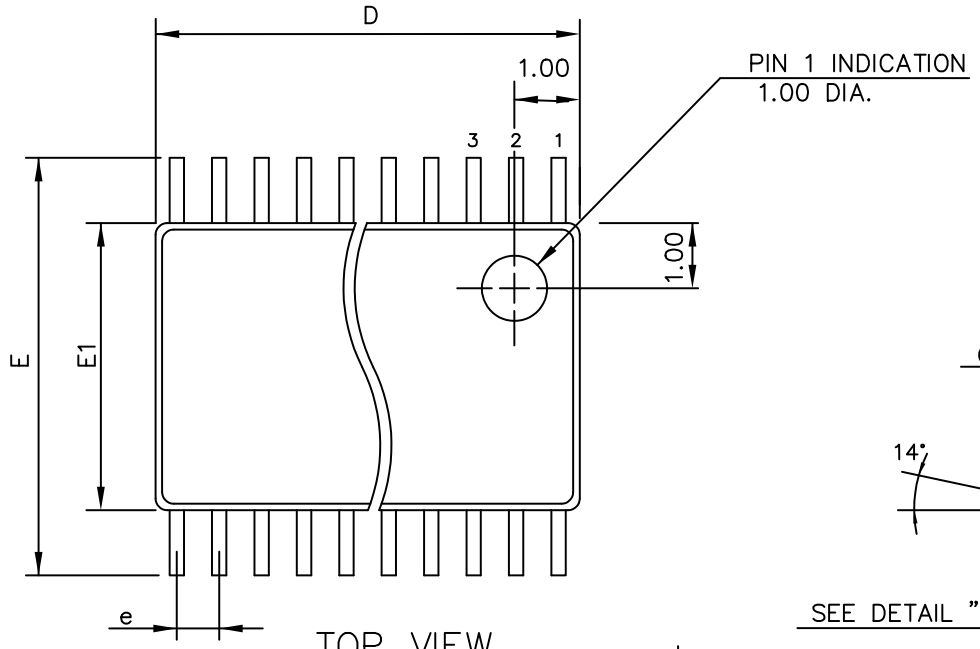
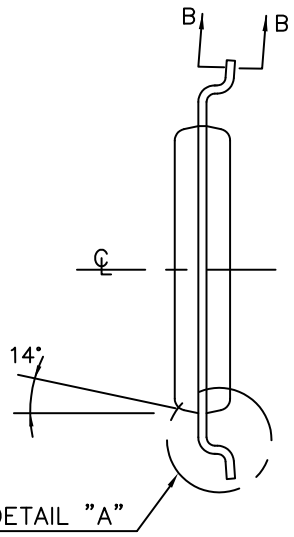
DESCRIPTION:	**SOIC−16, 150 mils**		**PAGE 1 OF 1**

TSSOP 16
CASE 948AH
ISSUE O

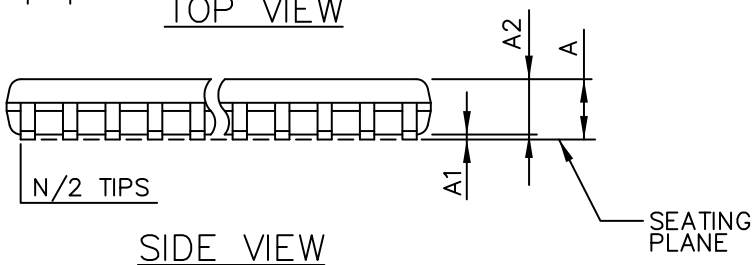
DATE 19 SEP 2008



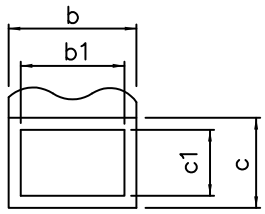
TOP VIEW



END VIEW



SIDE VIEW

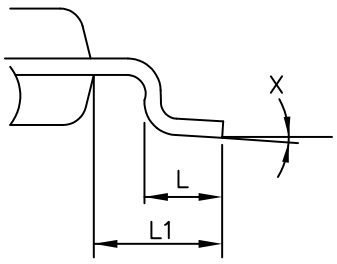


SECTION "B–B"

THIS TABLE FOR 0.65mm PITCH

SYMBOL	COMMON DIMENSIONS		
	MIN.	NOM.	MAX.
A	——	——	1.10
A_1	0.05	——	0.15
A_2	0.85	0.90	0.95
b	0.19	–	0.30
b1	0.19	0.22	0.25
c	0.09	–	0.20
c1	0.09	0.127	0.16
D	SEE VARIATIONS		
E1	4.30	4.40	4.50
e	0.65 BSC		
E	6.40 BSC		
L	0.50	0.60	0.70
L1	1.00 REF		
N	SEE VARIATIONS		
X	0°	——	8°

NOTE VARIATIONS	D	N
AA/AAT	3.00 BSC	8
AB–1/ABT	5.00 BSC	14
AB/ABT	5.00 BSC	16
AD/ADT	7.80 BSC	24



DETAIL 'A'

ALL DIMENSIONS IN MILLIMETERS

MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm ON D PER SIDE

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