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74VCX16244

Low Voltage 16-Bit Buffer/Line Driver with 3.6V Tolerant Inputs and Outputs

General Description

The VCX16244 contains sixteen non-inverting buffers with 3-STATE outputs to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble (4-bit) controlled. Each nibble has separate 3-STATE control inputs which can be shorted together for full 16-bit operation.

The 74VCX16244 is designed for low voltage (1.2V to 3.6V) V_{CC} applications with I/O capability up to 3.6V.

The 74VCX16244 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

- 1.2V to 3.6V V_{CC} supply operation
- 3.6V tolerant inputs and outputs
- t_{PD}
 - 2.5 ns max for 3.0V to 3.6V V_{CC}
- Power-off high impedance inputs and outputs
- Supports live insertion and withdrawal (Note 1)
- Static Drive (I_{OL})
 - +24 mA at 3.0V V_{CC}
- User programmable noise/EMI reduction circuitry
- Latch-up performance exceeds 300 mA
- ESD performance:
 - Human body model > 2000V
 - Machine model > 200V
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA)

Note 1: To ensure the high impedance state during power up or power down, OE should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Ordering Code

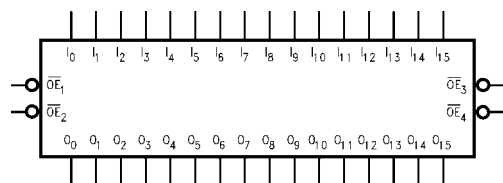
Order Number	Package Number	Package Description
74VCX16244 (Note 2, Note 3)	BGA54A	54-Pall Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
74VCX16244MTD (Note 3)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Note 2: Ordering Code "G" indicates Tray.

Note 3: Devices also available in tape and reel. Specify by appending the suffix letter "X" to the ordering code.

74VCX16244 Low Voltage 16-Bit Buffer/Line Driver with 3.6V Tolerant Inputs and Outputs

Logic Symbol

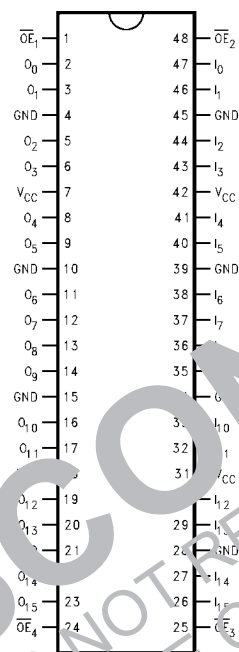


Pin Descriptions

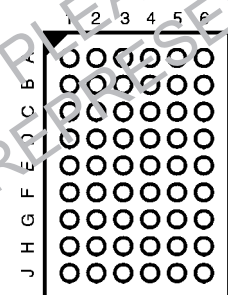
Pin Names	Description
\overline{OE}_n	Output Enable Input (Active LOW)
I_0 – I_{15}	Inputs
O_0 – O_{15}	Outputs
NC	No Connect

Connection Diagrams

Pin Assignment for TSSOP



Pin Assignment for FBGA



(Top Thru View)

FBGA Pin Assignments

	1	2	3	4	5	6
A	O ₀	NC	\overline{OE}_1	\overline{OE}_2	NC	O ₁
B	O ₂	O ₁	V _{CC}	NC	O ₃	I ₂
C	O ₄	O ₅	V _{CC}	GND	I ₄	I ₃
D	O ₆	O ₇	GND	GND	I ₅	I ₆
E	O ₈	O ₉	GND	GND	I ₇	I ₈
F	O ₁₀	O ₁₁	GND	GND	I ₉	I ₁₀
G	O ₁₂	O ₁₃	V _{CC}	V _{CC}	I ₁₁	I ₁₂
H	O ₁₄	O ₁₅	NC	NC	I ₁₃	I ₁₄
J	O ₁₅	NC	\overline{OE}_4	\overline{OE}_3	NC	I ₁₅

Truth Tables

Inputs		Outputs
\overline{OE}_1	I_0 – I_3	O_0 – O_3
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
\overline{OE}_3	I_8 – I_{11}	O_8 – O_{11}
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
\overline{OE}_2	I_4 – I_7	O_4 – O_7
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
\overline{OE}_4	I_{12} – I_{15}	O_{12} – O_{15}
L	L	L
L	H	H
H	X	Z

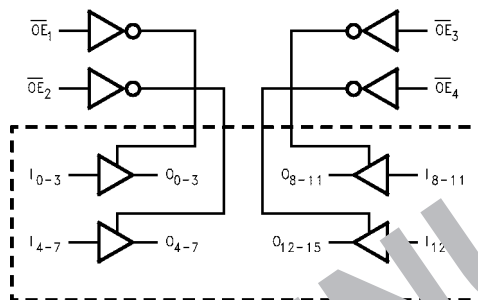
H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial (HIGH or LOW, inputs may not float)
 Z = High Impedance

Functional Description

The 74VCX16244 contains sixteen non-inverting buffers with 3-STATE outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of each other. The control pins may be shorted together to obtain full 16-bit operation. The 3-STATE out-

puts are controlled by an Output Enable (\overline{OE}_n) input. When \overline{OE}_n is LOW, the outputs are in the 2-state mode. When \overline{OE}_n is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the inputs.

Logic Diagram



Absolute Maximum Ratings (Note 4)

Supply Voltage (V_{CC})	-0.5V to +4.6V
DC Input Voltage (V_I)	-0.5V to +4.6V
Output Voltage (V_O)	
Outputs 3-STATED	-0.5V to +4.6V
Outputs Active (Note 5)	-0.5V to $V_{CC} + 0.5V$
DC Input Diode Current (I_{IK}) $V_I < 0V$	-50 mA
DC Output Diode Current (I_{OK})	
$V_O < 0V$	-50 mA
$V_O > V_{CC}$	+50 mA
DC Output Source/Sink Current	
(I_{OH}/I_{OL})	± 50 mA
DC V_{CC} or GND Current per	
Supply Pin (I_{CC} or GND)	± 100 mA
Storage Temperature Range (T_{STG})	-65°C to +150°C

Recommended Operating Conditions (Note 6)

Power Supply	
Operating	1.2V to 3.6V
Input Voltage	-0.3V to +3.6V
Output Voltage (V_O)	
Output in Active States	0.0V to V_{CC}
Output in 3-State	0.0V to 3.6V
Output Current in I_{OH}/I_{OL}	
$V_{CC} = 3.0V$ to 3.6V	24 mA
$V_{CC} = 2.3V$ to 2.7V	13 mA
$V_{CC} = 1.65V$ to 2.3V	6 mA
$V_{CC} = 1.4V$ to 1.6V	± 2 mA
$V_{CC} = 1.2V$	$\pm 100 \mu A$
Free Air Operating Temperature	-40°C to +55°C
Minimum Output Rise/Fall Rate (dV/dt)	
$V_{IN} = 0.8V$ to $2.0V$, $V_{CC} = 1.0V$	10 ns/V

Note 4: Absolute Maximum Ratings are those values beyond which the safe operation of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 5: I_{OK} Absolute Maximum Rating must be observed.

Note 6: Floating or unused inputs must be held HIGH or LOW.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		2.7 - 3.6	2.0		V
			2.3 - 2.7	1.6		
			1.65 - 2.3	$0.65 \times V_{CC}$		
			1.4 - 1.6	$0.65 \times V_{CC}$		
			1.2	$0.65 \times V_{CC}$		
V_{IL}	LOW Level Input Voltage		2.7 - 3.6		0.8	V
			2.3 - 2.7		0.7	
			1.65 - 2.3		$0.35 \times V_{CC}$	
			1.4 - 1.6		$0.35 \times V_{CC}$	
			1.2		$0.05 \times V_{CC}$	
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	2.7 - 3.6	$V_{CC} - 0.2$		V
		$I_{OH} = -12$ mA	2.7	2.2		
		$I_{OH} = -18$ mA	3.0	2.4		
		$I_{OH} = -24$ mA	3.0	2.2		
		$I_{OH} = -100 \mu A$	2.3 - 2.7	$V_{CC} - 0.2$		
		$I_{OH} = -6$ mA	2.3	2.0		
		$I_{OH} = -12$ mA	2.3	1.8		
		$I_{OH} = -18$ mA	2.3	1.7		
		$I_{OH} = -100 \mu A$	1.65 - 2.3	$V_{CC} - 0.2$		
		$I_{OH} = -6$ mA	1.65	1.25		
		$I_{OH} = -100 \mu A$	1.4 - 1.6	$V_{CC} - 0.2$		
		$I_{OH} = -2$ mA	1.4	1.05		
		$I_{OH} = -100 \mu A$	1.2	$V_{CC} - 0.2$		

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V _{CC} (V)	Min	Max	Units
V _{OL}	LOW Level Output Voltage	I _{OL} = 100 μ A	2.7 - 3.6		0.2	V
		I _{OL} = 12 mA	2.7		0.4	
		I _{OL} = 18 mA	3.0		0.4	
		I _{OL} = 24 mA	3.0		0.55	
		I _{OL} = 100 μ A	2.3 - 2.7		0.2	
		I _{OL} = 12 mA	2.3		0.4	
		I _{OL} = 18 mA	2.3		0.6	
		I _{OL} = 100 μ A	1.65 - 2.3		0	
		I _{OL} = 6 mA	1.65		0.3	
		I _{OL} = 100 μ A	1.4 - 1.6		0.2	
I _{OZ}	3-STATE Output Leakage	I _{OL} = 2 mA	1.4		0.35	μ A
		I _{OL} = 100 μ A	1.2		0.2	
I _I	Input Leakage Current	0 \leq V _I \leq 3.6V	1.2 - 3.6		\pm 5.0	μ A
I _{OFF}	Power-OFF Leakage Current	0 \leq (V _I , V _O) \leq 3.6V			\pm 0.0	μ A
I _{CC}	Quiescent Supply Current	V _I = V _{CC} or GND	1.2 - 3.6		20.0	μ A
		V _{CC} \leq (V _I , V _O) \leq 3.6V (Note)	1.2 - 3.6		\pm 20.0	μ A
Δ I _{CC}	Increase in I _{CC} per Input	V _{IH} = V _{CC} \pm 0.5V	2.7 - 3.6		75.0	μ A

Note 7: Outputs disabled or 3-STATE only.**AC Electrical Characteristics** (Note 8)

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = -40°C to +85°C		Units	Figure Number
			V _I	Min	Max		
t _{PHL} t _{PLH}	Propagation Delay	C _L = 30 pF, R _L = 500 Ω	3.3 \pm 0.3	0.8	2.5	ns	Figures 1, 2
			2.5 \pm 0.2	1.0	3.0		
		C _L = 15 pF, R _L = 2k Ω	1.8 \pm 0.15	1.5	6.0		Figures 5, 6
			1.5 \pm 0.1	1.0	12.0		
t _{PZL} t _{PZH}	Propagation Delay	C _L = 30 pF, R _L = 500 Ω	3.3 \pm 0.3	0.8	3.5	ns	Figures 1, 3, 4
			2.5 \pm 0.2	1.0	4.1		
		C _L = 15 pF, R _L = 2k Ω	1.8 \pm 0.15	1.5	8.2		Figures 5, 7, 8
			1.5 \pm 0.1	1.0	16.4		
t _{PHZ} t _{PHZ}	Output Disable Time	C _L = 30 pF, R _L = 500 Ω	3.3 \pm 0.3	0.8	3.5	ns	Figures 1, 3, 4
			2.5 \pm 0.2	1.0	3.8		
		C _L = 15 pF, R _L = 2k Ω	1.8 \pm 0.15	1.5	6.8		Figures 5, 7, 8
			1.5 \pm 0.1	1.0	13.6		
t _{OSHL} t _{OSLH}	Output to Output Skew (Note 9)	C _L = 30 pF, R _L = 500 Ω	3.3 \pm 0.3		0.5	ns	
			2.5 \pm 0.2		0.5		
		C _L = 15 pF, R _L = 2k Ω	1.8 \pm 0.15		0.75		
			1.5 \pm 0.1		1.5		

Note 8: For C_L = 50 pF, add approximately 300 ps to the AC maximum specification.**Note 9:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

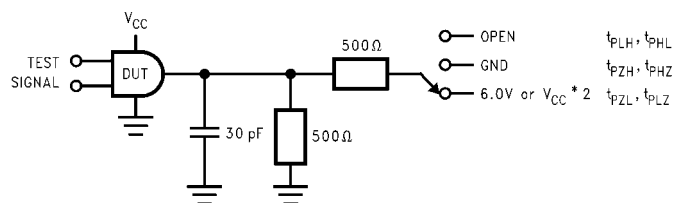
Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = +25°C	Units
				Typical	
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.8	0.25	V
			2.5	0.6	
			3.3	0.8	
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.8	-0.25	V
			2.5	-0.6	
			3.3	-0.8	
V _{OHV}	Quiet Output Dynamic Valley V _{OH}	C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.8	1.5	V
			2.5	1.9	
			3.3	2.2	

Capacitance

Symbol	Parameter	Conditions	T _A = +25°C	Units
			Typical	
C _{IN}	Input Capacitance	V _{CC} = 1.8, 2.5V or 3.3V, V _I = 0V or V _{CC}	5.0	pF
C _{OUT}	Output Capacitance	V _I = 0V or V _{CC} , V _{CC} = 1.8V, 2.5V or 3.3V	7.0	pF
C _{PD}	Power Dissipation Capacitance	V _I = 0V or V _{CC} , f = 100 kHz, V _{CC} = 1.8V, 2.5V or 3.3V	20.0	pF

AC Loading and Waveforms ($V_{CC} 3.3V \pm 0.3V$ to $1.8V \pm 0.15V$)



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at $V_{CC} = 3.3 \pm 0.3V$; $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V; 1.8V \pm 0.15V$
t_{PZH}, t_{PHZ}	GND

FIGURE 1. AC Test Circuit

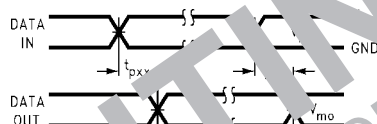


FIGURE 2. Waveforms for Inverting and Non-Inverting Functions

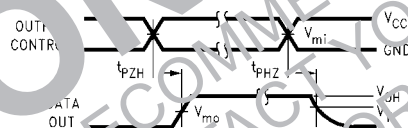


FIGURE 3. Enable and Disable Times for Low Voltage Logic

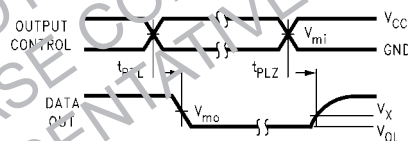
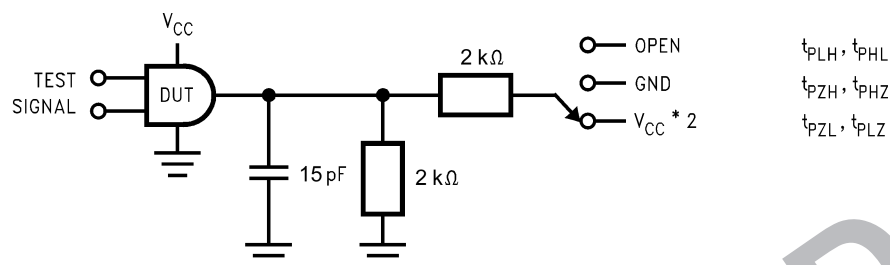


FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

Symbol	V_{CC}		
	$3.3V \pm 0.3V$	$2.5V \pm 0.2V$	$1.8V \pm 0.15V$
V_{mi}	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_{mo}	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_X	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$	$V_{OL} + 0.15V$
V_Y	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$	$V_{OH} - 0.15V$

AC Loading and Waveforms ($V_{CC} = 1.5 \pm 0.1V$ to $1.2V$)

TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	$V_{CC} \times 2$ at $V_{CC} = 1.5 \pm 0.1V$
t_{PZH}, t_{PHZ}	GND

FIGURE 5. AC Test Circuit



FIGURE 6. Waveforms for Inverting and Non-Inverting Functions

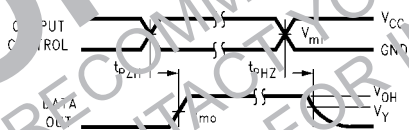


FIGURE 7. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

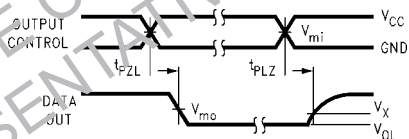
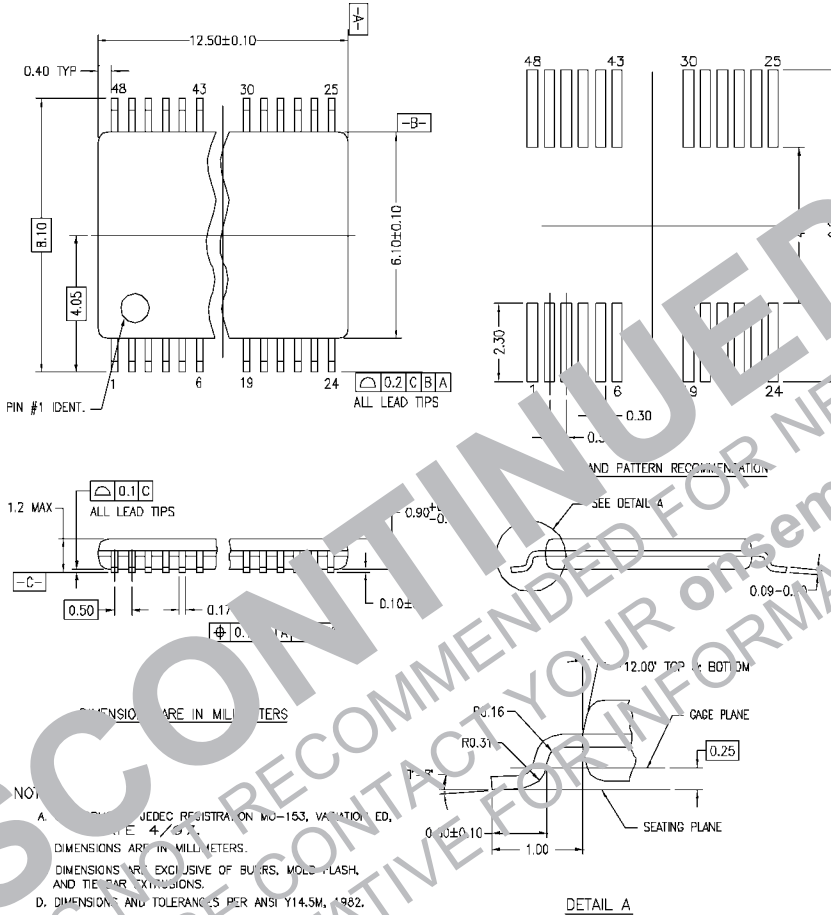


FIGURE 8. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

Symbol	V_{CC}
	$1.5V \pm 0.1V$
V_{mi}	$V_{CC}/2$
V_{mo}	$V_{CC}/2$
V_X	$V_{OL} + 0.1V$
V_Y	$V_{OH} - 0.1V$

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

**4th-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48**

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