onsemi

74LCX240

The LCX240 is an inverting octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver. The device is designed for low voltage V_{CC} applications with capability of interfacing to a 5 V signal environment.

The LCX240 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5 V Tolerant Inputs and Outputs
- 1.65 V-5.5 V V_{CC} Specifications Provided
- 6.5 ns t_{PD} Max. (V_{CC} 3.3 V), 10 μa I_{CC} Max.
- Power-down High Impedance Inputs and Outputs
- Supports Live Insertion/Withdrawal¹
- ± 24 mA Output Drive (V_{CC} = 3.0 V)
- Implements Proprietary Noise/EMI Reduction Circuitry
- Latch-up Performance Exceeds 100 mA
- ESD Performance:
 - ♦ Human Body Model >2000 V
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



SOIC-20W CASE 751BJ



CASE 948AQ



ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

1. To ensure the high-impedance state during power up or down, \overline{OE} should be tied to V_{CC} through a pull-up resistor: the minimum value or the resistor is determined by the current-sourcing capability of the driver.

1

74LCX240



Figure 1. Connection Diagram

Table 1. PIN DESCRIPTION

Pin Names	Description
$\overline{OE}_1, \overline{OE}_2$	3-STATE Output Enable Inputs
I ₀ —I ₇	Inputs
$\overline{O}_0 - \overline{O}_7$	Outputs



Figure 2. Logic Diagram

TRUTH TABLE

Inputs		Outputs
OE ₁	I _n	(Pins 12, 14, 16, 18)
L	L	н
L	Н	L
Н	Х	Z

OE ₂	I _n	(Pins 3, 5, 7, 9)
L	L	Н
L	Н	L
Н	Х	Z

H = High Voltage Level L = Low Voltage Level X = Immaterial Z = High Impedance

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V _{CC}	DC Supply Voltage		-0.5 to +6.5	V
VI	DC Input Voltage (Note 1)		-0.5 to +6.5	V
Vo	DC Output Voltage (Note 1) Active-Mo Power-D	de (High or Low State) Tri-State Mode own Mode (V _{CC} = 0 V)	-0.5 to V _{CC} +0.5 -0.5 to +6.5 -0.5 to +6.5	V
l _{IK}	DC Input Diode Current	V _{IN} < GND	-50	mA
I _{OK}	DC Output Diode Current	-50	mA	
Ι _Ο	DC Output Source/Sink Current	±50	mA	
I _{CC} or I _{GND}	DC Supply Current per Supply Pin or Ground Pin	±100	mA	
T _{STG}	Storage Temperature Range	-65 to +150	°C	
ΤL	Lead Temperature, 1 mm from Case for 10 secs	260	°C	
TJ	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 2)	SOIC-20W WQFN20 TSSOP-20	96 99 150	°C/W
PD	Power Dissipation in Still Air	SOIC-20W WQFN20 TSSOP-20	1302 1256 833	mW
MSL	Moisture Sensitivity	SOIC-20W All Other Packages	Level 3 Level 1	-
F _R	Flammability Rating C	0xygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	-
V _{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model	2000 N/A	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected. 1. I_O absolute maximum rating must be observed.

Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.
HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A.

RECOMMENDED OPERATING CONDITIONS (Note 4)

Symbol	Pa	Min	Max	Unit	
V _{CC}	Supply Voltage	Operating Data Retention Only	1.65 1.5	5.5 5.5	V
VI	Digital Input Voltage		0	5.5	V
Vo	Output Voltage	Active Mode (High or Low State) Tri-State Mode Power Down Mode (V _{CC} = 0 V)	0 0 0	V _{CC} 5.5 5.5	V
T _A	Operating Free-Air Temperature		-40	+125	°C
t _r , t _f	Input Rise or Fall Rate	$\begin{array}{c} V_{CC} = 1.65 \; V \; to \; 1.95 \; V \\ V_{CC} = 2.3 \; V \; to \; 2.7 \; V \\ V_{IN} \; from \; 0.8 \; V \; to \; 2.0 \; V, \; V_{CC} = 3.0 \; V \\ V_{CC} = 4.5 \; V \; to \; 5.5 \; V \end{array}$	0 0 0 0	20 20 10 5	nS/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS

				T _A = −40 °C to +85 °C		T _A = −40 °C to +125 °C		
Symbol	Parameter	Conditions	V _{CC} (V)	Min	Max	Min	Max	Unit
V _{IH}	High-Level		1.65 to 1.95	0.65 x V _{CC}		0.65 x V _{CC}		V
	input voitage		2.3 to 2.7	1.7		1.7		
			2.7 to 3.6	2.0		2.0		
			4.5 to 5.5	0.7 x V _{CC}		0.7 x V _{CC}		
V _{IL}	Low-Level		1.65 to 1.95		$0.35 \times V_{CC}$		0.35 x V _{CC}	V
	Input Voltage		2.3 to 2.7		0.7		0.7	
			2.7 to 3.6		0.8		0.8	
			4.5 to 5.5		0.3 x V _{CC}		0.3 x V _{CC}	
V _{OH}	High-Level	$V_I = V_{IH} \text{ or } V_{IL}$						V
	Voltage	I _{OH} = -100 μA	1.65 to 5.5	V _{CC} - 0.1	-	V _{CC} – 0.1	-	
		I _{OH} = -4 mA	1.65	1.2	-	1.2	-	
		I _{OH} = -8 mA	2.3	1.8	-	1.8	-	
		I _{OH} = -12 mA	2.7	2.2	-	2.2	-	
		I _{OH} = -16 mA	3.0	2.4	-	2.4	-	
		I _{OH} = -24 mA	3.0	2.2	-	2.2	-	
		I _{OH} = -32 mA	4.5	3.8		3.8		
V _{OL}	Low-Level	$V_I = V_{IH} \text{ or } V_{IL}$						V
	Voltage	I _{OL} = 100 μA	1.65 to 5.5	-	0.1	_	0.1	
		I _{OL} = 4 mA	1.65	-	0.45	-	0.45	
		I _{OL} = 8 mA	2.3	-	0.6	_	0.6	
		l _{OL} = 12 mA	2.7	-	0.4	_	0.4	
		l _{OL} = 16 mA	3.0	-	0.4	-	0.4	
		I _{OL} = 24 mA	3.0	-	0.55	-	0.55	
		I _{OL} = 32 mA	4.5		0.6		0.6	
lı	Input Leakage Current	V _I = 0 to 5.5 V	3.6	-	±5.0	-	±5.0	μΑ
I _{OZ}	3-State Output Leakage Current		3.6	_	±5.0	_	±5.0	μΑ
I _{OFF}	Power Off Leakage Current	$V_{I} = 5.5 V \text{ or}$ $V_{O} = 5.5 V$	0	_	10	_	10	μΑ
I _{CC}	Quiescent	V_{I} = 5.5 V or GND	2.3 to 3.6	-	10	-	10	μΑ
	Current	3.6 V ≤ V _I , V _O ≤ 5.5 V (Note 5)			±10.0		±10.0	
ΔI_{CC}	Increase in I _{CC} per Input	$V_{IH} = V_{CC} - 0.6 V$	2.3 to 3.6	_	500	-	500	μΑ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions. 5. Outputs disabled or 3-STATE only.

74LCX240

AC ELECTRICAL CHARACTERISTICS

				T _A = -40 °C	C to +85 °C	T _A = -40 °C	to +125 °C	
Symbol	Parameter	Test Condition	V _{CC} (V)	Min	Max	Min	Max	Unit
t _{PLH} , t _{PHL}	Propagation Delay, D	See Figures	1.65 to 1.95	-	10.3	-	10.3	ns
	to U	3 and 4	2.3 to 2.7	-	7.8	-	7.8	
			2.7	-	7.5	-	7.5	
			3.0 to 3.6	-	6.5	-	6.5	
			4.5 to 5.5	-	5.9	-	5.9	
t _{PZH} , t _{PZL}	Output Enable Time,	See Figures	1.65 to 1.95	-	13.0	-	13.0	ns
	UE to U	3 and 4	2.3 to 2.7	-	10.0	-	10.0	
			2.7	-	9.0	-	9.0	
			3.0 to 3.6	-	8.0	-	8.0	
			4.5 to 5.5	-	7.3	-	7.3	
t _{PHZ} , t _{PLZ}	Output Disable Time,	See Figures	1.65 to 1.95	-	11.0	-	11.0	ns
		3 and 4	2.3 to 2.7	-	8.4	-	8.4	
			2.7	-	8.0	-	8.0	
			3.0 to 3.6	-	7.0	-	7.0	
			4.5 to 5.5	-	6.0	-	6.0	
t _{OSHL} ,	Output to Output		1.65 to 1.95	-	-	-	-	ns
^I OSLH	Skew (INDLE D)		2.3 to 2.7	-	-	-	-	
			2.7	-	-	-	-	
			3.0 to 3.6	-	1.0	-	1.0	

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation I_{CC(OPR)} = C_{PD} x V_{CC} x f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption: P_D = C_{PD} x V_{CC}² x f_{in} + I_{CC} x V_{CC}.

DYNAMIC SWITCHING CHARACTERISTICS

			Vee	T _A = +25 °C	
Symbol	Characteristic	Condition	(V)	Тур	Unit
V _{OLP}	Quiet Output	C_{L} = 50 pF, V_{IH} = 3.3 V, V_{IL} = 0 V	3.3	0.8	V
	Dynamic Peak VOL	C_L = 30 pF, V_{IH} = 2.5 V, V_{IL} = 0 V	2.5	0.6	
V _{OLV}	Quiet Output	C_L = 50 pF, V_{IH} = 3.3 V, V_{IL} = 0 V	3.3	-0.8	V
	Dynamic valley vol	C_L = 30 pF, V_{IH} = 2.5 V, V_{IL} = 0 V	2.25	-0.6	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Тур	Unit
C _{IN}	Input Capacitance	V_{CC} = 3.3 V, V_{I} = 0 V or V_{CC}	7	pF
C _{OUT}	Output Capacitance	V_{CC} = 3.3 V, V_{I} = 0 V or V_{CC}	8	pF
C _{PD}	Power Dissipation Capacitance	10 MHz, V_{CC} = 3.3 V, V_{I} = 0 V or V_{CC}	25	pF



Test	Switch Position
t _{PLH} / t _{PHL}	Open
t _{PLZ} / t _{PZL}	V _{LOAD}
t _{PHZ} / t _{PZH}	GND

 R_T is Z_{OUT} of pulse generator (typically 50 Ω) f = 1 MHz

 $^{\ast}\text{C}_{\text{L}}$ includes probe and jig capacitance



Figure 3. Test Circuit



V _{CC} , V	R_L, Ω	C _L , pF	V _{LOAD}	V _{mi} , V	V _{mo} , V	V _Y , V
1.65 to 1.95	500	30	$2 \times V_{CC}$	V _{CC} /2	V _{CC} /2	0.15
2.3 to 2.7	500	30	$2 \times V_{CC}$	V _{CC} /2	V _{CC} /2	0.15
2.7	500	50	6 V	1.5	V _{CC} /2	0.3
3.0 to 3.6	500	50	6 V	1.5	V _{CC} /2	0.3
4.5 to 4.5	500	50	2 x V _{CC}	V _{CC} /2	V _{CC} /2	0.3

Figure 4. Switching Waveforms



ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
74LCX240MTCX	LCX 240	TSSOP-20 (Pb-Free)	2500 / Tape & Reel

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, <u>BRD8011/D</u>.



SOIC-20, 300 mils CASE 751BJ ISSUE O

DATE 19 DEC 2008



TOP VIEW





Notes:

(1) All dimensions are in millimeters. Angles in degrees.

(2) Complies with JEDEC MS-013.



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TSSOP20, 4.4x6.5 CASE 948AQ ISSUE A

DATE 19 MAR 2009



SYMBOL	MIN	NOM	MAX
А			1.20
A1	0.05		0.15
A2	0.80		1.05
b	0.19		0.30
с	0.09		0.20
D	6.40	6.50	6.60
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
е		0.65 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°		8°





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