Low Voltage Quad 2-Input Multiplexer

With 5 V Tolerant Inputs

74LCX157

The LCX157 is a high-speed quad 2-input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four outputs present the selected data in the true (non-inverted) form.

The LCX157 can also be used as a function generator.

The 74LCX157 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5 V Tolerant Inputs
- 1.65 V to 5.5 V, V_{CC} Specifications Provided
- 5.8 ns t_{PD} Max. (V_{CC} = 3.3 V), 10 μA I_{CC} Max.
- Power Down High Impedance Inputs and Outputs
- ±24 mA Output Drive (V_{CC} = 3.0 V)
- Implements Patented Noise/EMI Reduction Circuitry
- Latch-up Performance Exceeds 100 mA
- ESD Performance: Human Body Model >2000 V
- These are Pb-Free Devices

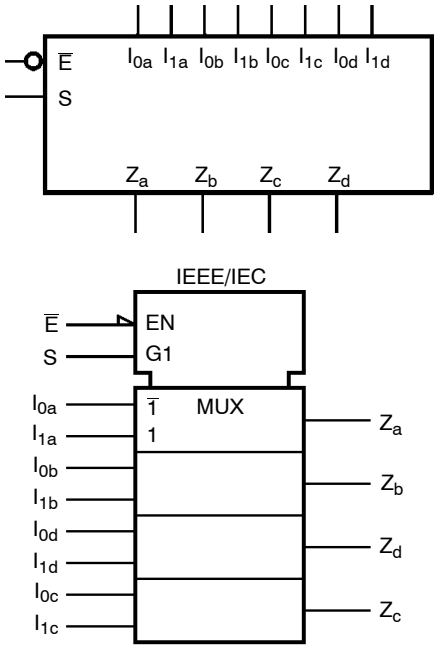
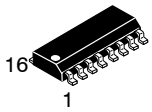
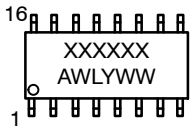


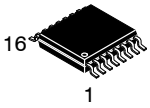
Figure 1. Logic Symbols

MARKING DIAGRAMS

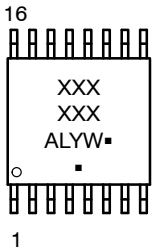


SOIC-16, 150 mils
CASE 751BG





TSSOP-16
CASE 948AH



A	= Assembly Location
WL, L	= Wafer Lot
Y	= Year
WW, W	= Work Week
G or ▪	= Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

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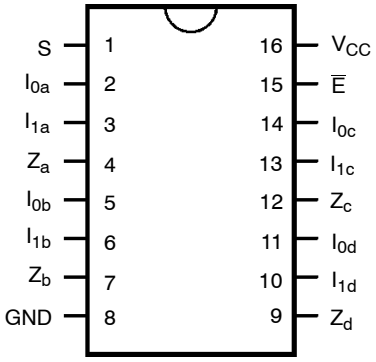


Figure 2. Connection Diagram

PIN DESCRIPTIONS

Pin Names	Description
I_{0a}–I_{0d}	Source 0 Data Inputs
I_{1a}–I_{1d}	Source 1 Data Inputs
$\overline{E}$	Enable Input
S	Select Inputs
Z_a–Z_d	Outputs

Functional Description

The LCX157 is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input ($\overline{E}$) is active-LOW. When $\overline{E}$ is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The LCX157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$Za = \overline{E} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S})$

$Zb = \overline{E} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$

$Zc = \overline{E} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S})$

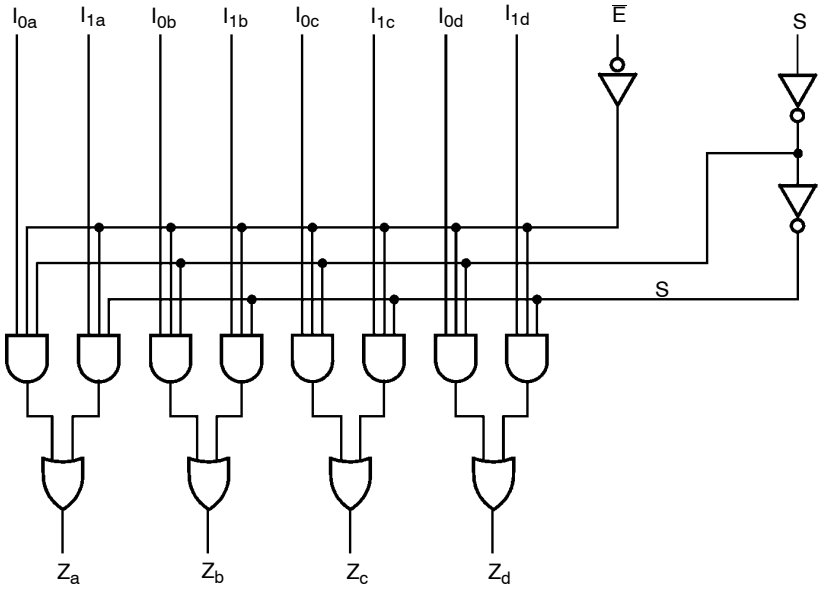
$Zd = \overline{E} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$

A common use of the LCX157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The LCX157 can generate any four of the sixteen different functions of two variables with one variable common. This is useful for implementing gating functions.

TRUTH TABLE

Inputs				Outputs
$\overline{E}$	S	I_0	I_1	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial



NOTE: Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 3. Logic Diagram

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +6.5	V
V_I	DC Input Voltage (Note 1)		−0.5 to +6.5	V
V_O	DC Output Voltage (Note 1)	Active-Mode (High or Low State) Tri-State Mode Power-Down Mode (V_{CC} = 0 V)	−0.5 to V_{CC} + 0.5 −0.5 to +6.5 −0.5 to +6.5	V
I_{IK}	DC Input Diode Current	V_I < GND	−50	mA
I_{OK}	DC Output Diode Current	V_O < GND	−50	mA
I_O	DC Output Source/Sink Current		±50	mA
I_{CC} or I_{GND}	DC Supply Current per Supply Pin or Ground Pin		±100	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 secs		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 1)	SOIC-16 TSSOP-16	126 159	°C/W
P_D	Power Dissipation in Still Air at 125°C	SOIC-16 TSSOP-16	995 787	mW
MSL	Moisture Sensitivity		Level 1	–
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	–
V_{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model	2000 N/A	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.
2. Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51−7.
3. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	Operating Data Retention Only	1.65 1.5	3.3 3.3	5.5 5.5	V
V_I	Digital Input Voltage		0	–	5.5	V
V_O	Output Voltage	Active Mode (High or Low State) Tri-State Mode Power Down Mode (V_{CC} = 0 V)	0 0 0	– – –	V_{CC} 5.5 5.5	V
T_A	Operating Free-Air Temperature		−40	–	+125	°C
t_r, t_f	Input Rise or Fall Rate	V_{CC} = 1.65 V to 1.95 V V_{CC} = 2.3 V to 2.7 V V_{IN} from 0.8 V to 2.0 V, V_{CC} = 3.0 V V_{CC} = 4.5 V to 5.5 V	0 0 0 0	– – – –	20 20 10 5	nS/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		T_A = −40°C to +125°C		Unit
				Min	Max	Min	Max	
V_{IH}	HIGH Level Input Voltage		1.65 – 1.95	0.65 x V_{CC}	–	0.65 x V_{CC}	–	V
			2.3 – 2.7	1.7	–	1.7	–	
			3.0 – 3.6	2.0	–	2.0	–	
			4.5 – 5.5	0.70 x V_{CC}	–	0.70 x V_{CC}	–	
V_{IL}	LOW Level Input Voltage		1.65 – 1.95	–	0.35 x V_{CC}	–	0.35 x V_{CC}	V
			2.3 – 2.7	–	0.7	–	0.7	
			3.0 – 3.6	–	0.8	–	0.8	
			4.5 – 5.5	–	0.30 x V_{CC}	–	0.30 x V_{CC}	
V_{OH}	High-Level Output Voltage	V_I = V_{IH} or V_{IL}						V
		I_{OH} = −100 μA	1.65 – 5.5	V_{CC} – 0.1	–	V_{CC} – 0.1	–	
		I_{OH} = −4 mA	1.65	1.29	–	1.29	–	
		I_{OH} = −8 mA	2.3	1.8	–	1.8	–	
		I_{OH} = −12 mA	2.7	2.2	–	2.2	–	
		I_{OH} = −16 mA	3.0	2.4	–	2.4	–	
		I_{OH} = −24 mA	3.0	2.2	–	2.2	–	
		I_{OH} = −32 mA	4.5	3.7		3.7		
V_{OL}	Low-Level Output Voltage	V_I = V_{IH} or V_{IL}						V
		I_{OL} = 100 μA	1.65 – 5.5	–	0.1	–	0.1	
		I_{OL} = 4 mA	1.65	–	0.24	–	0.24	
		I_{OL} = 8 mA	2.3	–	0.3	–	0.3	
		I_{OL} = 12 mA	2.7	–	0.4	–	0.4	
		I_{OL} = 16 mA	3.0	–	0.4	–	0.4	
		I_{OL} = 24 mA	3.0	–	0.55	–	0.55	
		I_{OL} = 32 mA	4.5	–	0.6	–	0.6	
I_I	Input Leakage Current	V_I = 0 to 5.5 V	1.65 – 5.5	–	±5.0	–	±5.0	μA
I_{OFF}	Power Off Leakage Current	V_I = 5.5 V or V_O = 5.5 V	0	–	10	–	10	μA
I_{CC}	Quiescent Supply Current	V_I = 5.5 V or GND	1.65 – 5.5	–	10	–	10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} – 0.6 V	2.3 – 3.6	–	500	–	500	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	V_{CC} (V)	T_A = −40°C to +85°C		T_A = −40°C to +125°C		Unit
				Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay, S to Z_n	See Figures 4 and 5	1.65 to 1.95	–	11.6	–	11.6	ns
			2.3 to 2.7	–	8.4	–	8.4	
			2.7	–	8.0	–	8.0	
			3.0 to 3.6	–	7.0	–	7.0	
			4.5 to 5.5	–	5.8	–	5.8	
t_{PLH}, t_{PHL}	Propagation Delay, $\overline{E}$ to Z_n	See Figures 4 and 5	1.65 to 1.95	–	11.6	–	11.6	ns
			2.3 to 2.7	–	8.4	–	8.4	
			2.7	–	8.0	–	8.0	
			3.0 to 3.6	–	7.0	–	7.0	
			4.5 to 5.5	–	5.8	–	5.8	
t_{PLH}, t_{PHL}	Propagation Delay, I_n to Z_n	See Figures 4 and 5	1.65 to 1.95	–	11.2	–	11.2	ns
			2.3 to 2.7	–	7.0	–	7.0	
			2.7	–	6.3	–	6.3	
			3.0 to 3.6	–	5.8	–	5.8	
			4.5 to 5.5	–	4.8	–	4.8	
t_{OSHL}, t_{OSLH}	Output to Output Skew (Note 5)		1.65 to 1.95	–	–	–	–	ns
			2.3 to 2.7	–	–	–	–	
			2.7	–	–	–	–	
			3.0 to 3.6	–	1.0	–	1.0	
			4.5 to 5.5	–	–	–	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = 25°C	Unit
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	C_L = 50 pF, V_{IH} = 3.3 V, V_{IL} = 0 V	3.3	0.8	V
		C_L = 30 pF, V_{IH} = 2.5 V, V_{IL} = 0 V	2.5	0.6	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	C_L = 50 pF, V_{IH} = 3.3 V, V_{IL} = 0 V	3.3	−0.8	V
		C_L = 30 pF, V_{IH} = 2.5 V, V_{IL} = 0 V	2.5	−0.6	

CAPACITANCE

Symbol	Parameter	Condition	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, V_I = 0 V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 3.3 V, V_I = 0 V or V_{CC}, f = 10 MHz	25	pF

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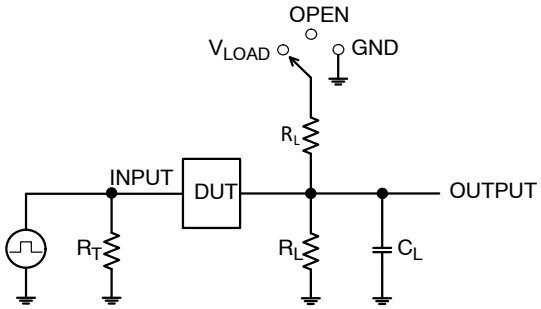
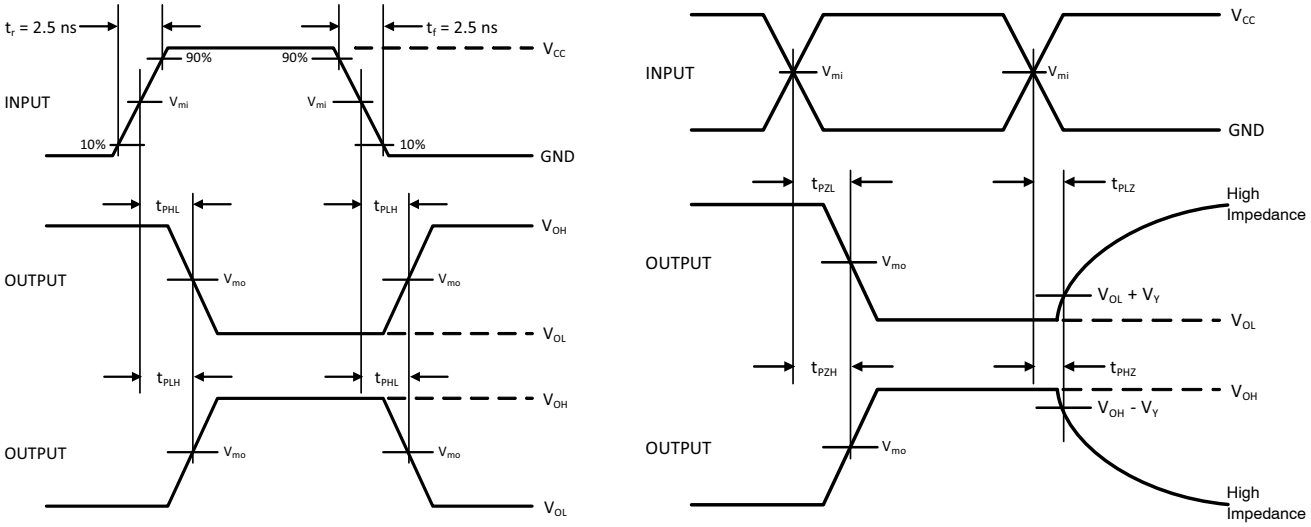


Test	Switch Position
t_{PLH} / t_{PHL}	Open
t_{PLZ} / t_{PZL}	V_{LOAD}
t_{PHZ} / t_{PZH}	GND

C_L includes probe and jig capacitance
R_T is Z_{OUT} of pulse generator (typically 50 Ω)
f = 1 MHz

Figure 4. Test Circuit



V_{CC}, V	R_L, Ω	C_L, pF	V_{LOAD}	V_m, V	V_Y, V
1.65 to 1.95	500	30	2 x V_{CC}	V_{CC}/2	0.15
2.3 to 2.7	500	30	2 x V_{CC}	V_{CC}/2	0.15
2.7	500	50	6 V	1.5	0.3
3.0 to 3.6	500	50	6 V	1.5	0.3
4.5 to 5.5	500	50	2 x V_{CC}	V_{CC}/2	0.3

Figure 5. Switching Waveforms

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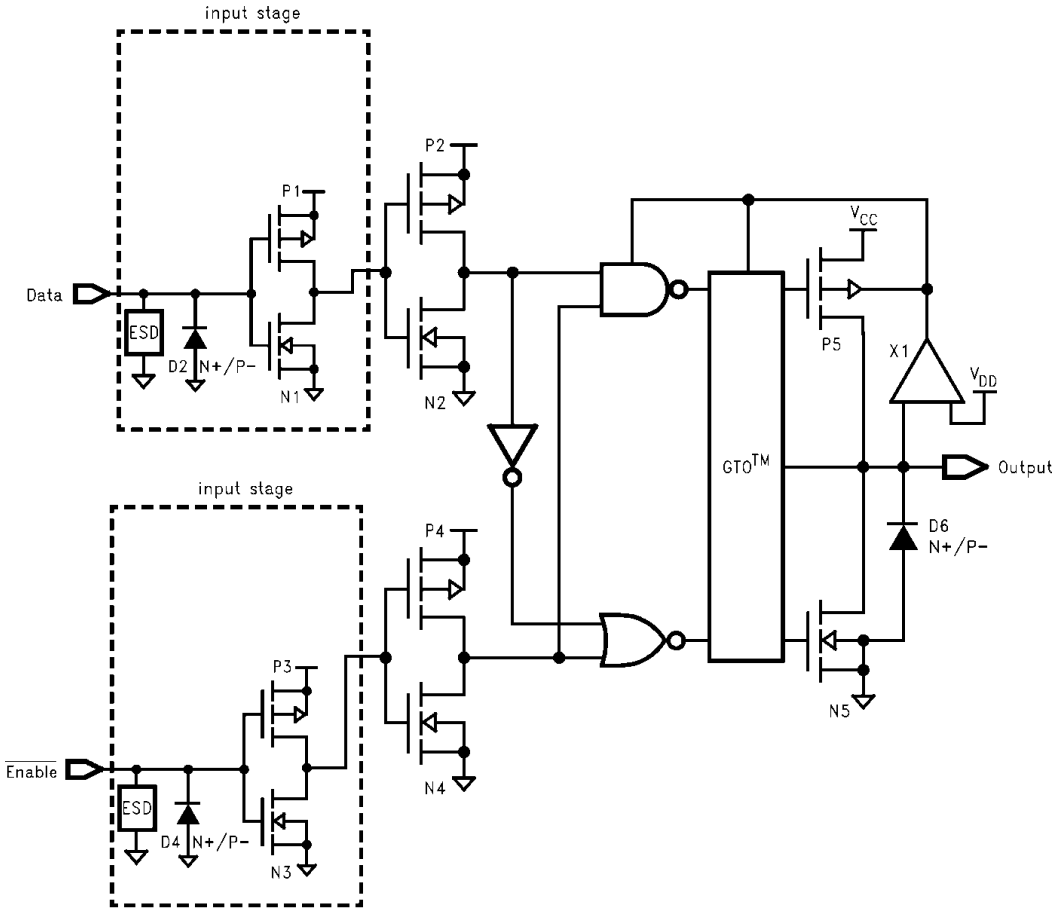

Figure 6. Schematic Diagram (Generic for LCX Family)

ORDERING INFORMATION

Device	Marking	Package	Shipping†
74LCX157MX	LCX157G	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel
74LCX157MTCX	LCX 157	TSSOP-16 (Pb-Free)	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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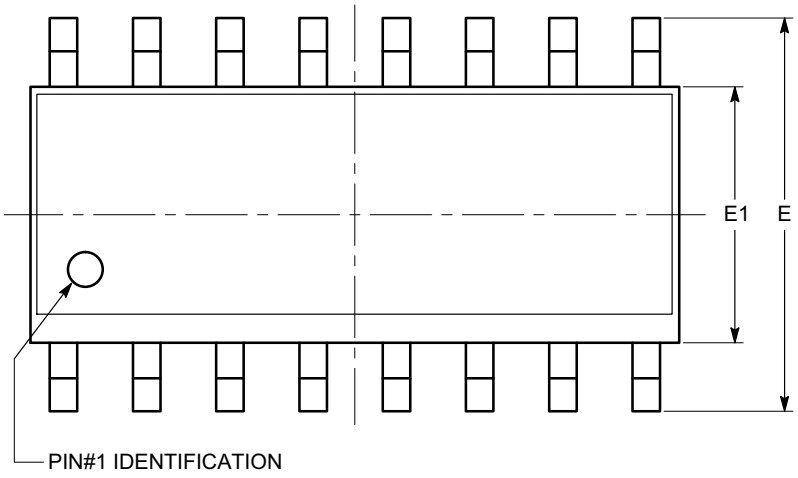
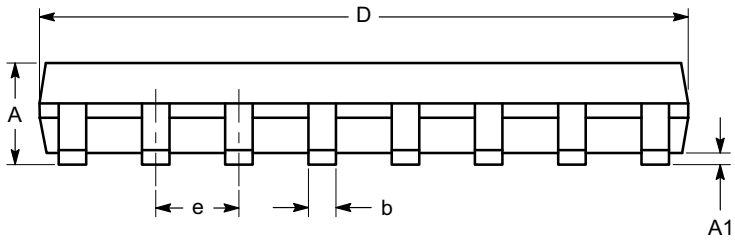
DATE 19 DEC 2008

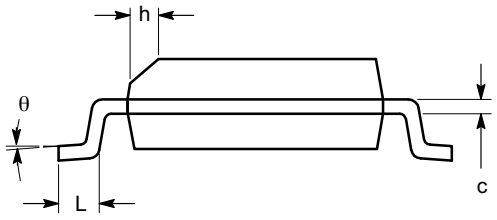


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

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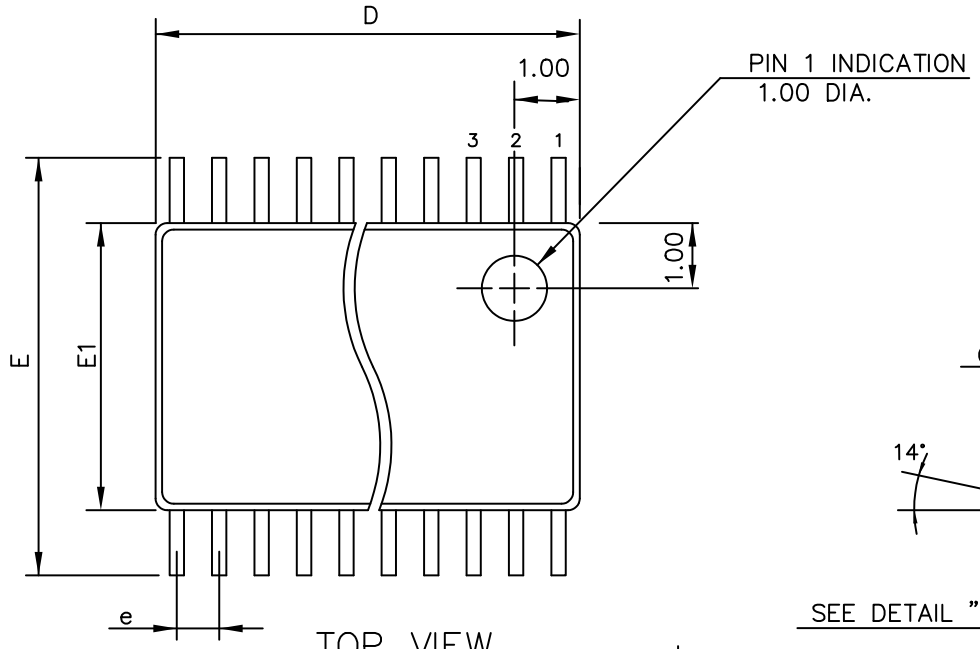
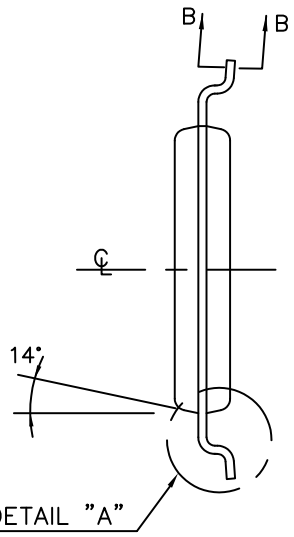
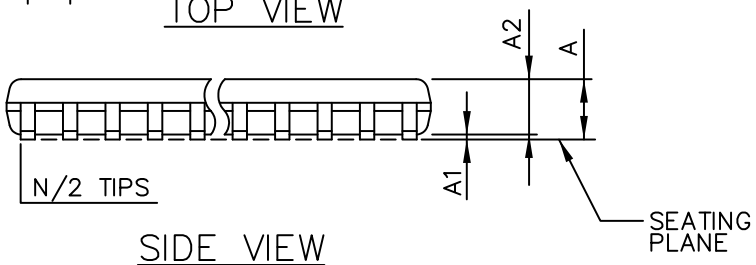


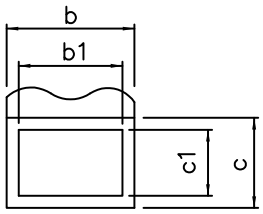
TOP VIEW



END VIEW



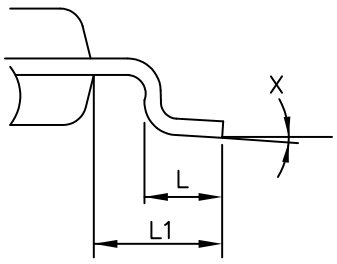
SIDE VIEW



SECTION "B–B"

THIS TABLE FOR 0.65mm PITCH

SYMBOL	COMMON DIMENSIONS			NOTE VARIATIONS	D	N
	MIN.	NOM.	MAX.			
A	——	——	1.10	AA/AAT	3.00 BSC	8
A_1	0.05	——	0.15	AB–1/ABT	5.00 BSC	14
A_2	0.85	0.90	0.95	AB/ABT	5.00 BSC	16
b	0.19	–	0.30	AD/ADT	7.80 BSC	24
b1	0.19	0.22	0.25			
c	0.09	–	0.20			
c1	0.09	0.127	0.16			
D	SEE VARIATIONS					
E1	4.30	4.40	4.50			
e	0.65 BSC					
E	6.40 BSC					
L	0.50	0.60	0.70			
L1	1.00 REF					
N	SEE VARIATIONS					
X	0°	——	8°			



DETAIL 'A'

ALL DIMENSIONS IN MILLIMETERS

MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm ON D PER SIDE

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