Field Effect Transistor - N-Channel, Enhancement Mode

2N7002DW

Features
• Dual N–Channel MOSFET
• Low On–Resistance
• Low Gate Threshold Voltage
• Low Input Capacitance
• Fast Switching Speed
• Low Input/Output Leakage
• Ultra–Small Surface Mount Package
• These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Ratings</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_DSS</td>
<td>Drain–Source Voltage</td>
<td>60</td>
<td>V</td>
</tr>
<tr>
<td>V_DGR</td>
<td>Drain–Gate Voltage (R_GS ≤ 1.0 MΩ)</td>
<td>60</td>
<td>V</td>
</tr>
<tr>
<td>V_GSS</td>
<td>Gate–Source Voltage</td>
<td>Continuous</td>
<td>±20</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Pulsed</td>
<td>±40</td>
</tr>
<tr>
<td>I_D</td>
<td>Drain Current</td>
<td>Continuous</td>
<td>115</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Continuous at 100°C</td>
<td>73</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Pulsed</td>
<td>800</td>
</tr>
<tr>
<td>T_J, T_STG</td>
<td>Junction and Storage Temperature Range</td>
<td>–55 to +150</td>
<td>°C</td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Ratings</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>P_D</td>
<td>Total Device Dissipation</td>
<td>200</td>
<td>mW</td>
</tr>
<tr>
<td></td>
<td>Derate Above T_A = 25°C</td>
<td>1.6</td>
<td>mW/°C</td>
</tr>
<tr>
<td>R_JJA</td>
<td>Thermal Resistance, Junction–to–Ambient (Note 1)</td>
<td>415</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

1. Device mounted on FR–4 PCB, 1 inch x 0.85 inch x 0.062 inch. Minimum land pad size.
ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Top Mark</th>
<th>Package</th>
<th>Shipping†</th>
</tr>
</thead>
<tbody>
<tr>
<td>2N7002DW</td>
<td>2N</td>
<td>SC70–6 (Pb-Free)</td>
<td>3000 / Tape &amp; Reel</td>
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</tbody>
</table>

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS \( (T_A = 25^\circ C \text{ unless otherwise noted}) \)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
</table>
| **OFF CHARACTERISTICS** \( (\text{Note 2}) \)
| \( BV_{DSS} \) | Drain–Source Breakdown Voltage \( V_{GS} = 0 \text{ V}, I_D = 10 \mu\text{A} \) | \( V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V} \) | 60   | 78  | –    | V    |
| \( I_{DSS} \) | Zero Gate Voltage Drain Current \( V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 125^\circ C \) | \( V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V} \) | –    | 0.001 | 1.0 | \mu A |
| \( I_{GSS} \) | Gate–Body Leakage \( V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V} \) | –    | 0.2  | \pm10 | nA  |

| **ON CHARACTERISTICS** \( (\text{Note 2}) \)
| \( V_{GS(th)} \) | Gate Threshold Voltage \( V_{DS} = V_{GS}, I_D = 250 \mu\text{A} \) | \( V_{GS} = 5 \text{ V}, I_D = 0.05 \text{ A} \) | 1.00 | 1.76 | 2.0 | V    |
| \( R_{\text{DS(on)}} \) | Static Drain–Source On–Resistance \( V_{GS} = 10 \text{ V}, I_D = 0.5 \text{ A} \), \( V_{GS} = 10 \text{ V}, I_D = 0.5 \text{ A}, T_J = 125^\circ C \) | \( V_{GS} = 10 \text{ V}, V_{DS} = 7.5 \text{ V} \) | 0.50 | 1.43 | –   | A    |
| \( g_{FS} \) | Forward Transconductance \( V_{DS} = 10 \text{ V}, I_D = 0.2 \text{ A} \) | \( V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V}, f = 1.0 \text{ MHz} \) | 80.0 | 356.5 | –   | mS   |

| **DYNAMIC CHARACTERISTICS** |
| \( C_{iss} \) | Input Capacitance \( V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V}, f = 1.0 \text{ MHz} \) | –  | 37.8 | 50  | pF   |
| \( C_{oss} \) | Output Capacitance \( V_{DD} = 30 \text{ V}, I_D = 0.2 \text{ A}, V_{GEN} = 10 \text{ V}, R_L = 150 \text{ \Omega}, R_{GEN} = 25 \text{ \Omega} \) | –  | 12.4 | 25  | pF   |
| \( C_{rss} \) | Reverse Transfer Capacitance \( V_{DD} = 30 \text{ V}, I_D = 0.2 \text{ A}, V_{GEN} = 10 \text{ V}, R_L = 150 \text{ \Omega}, R_{GEN} = 25 \text{ \Omega} \) | –  | 6.5  | 7   | pF   |

| **SWITCHING CHARACTERISTICS** \( (\text{Note 2}) \)
| \( I_{D(ON)} \) | Turn–On Delay Time \( V_{DD} = 30 \text{ V}, I_D = 0.2 \text{ A}, V_{GEN} = 10 \text{ V}, R_L = 150 \text{ \Omega}, R_{GEN} = 25 \text{ \Omega} \) | –  | 5.85 | 20  | ns   |
| \( I_{D(OFF)} \) | Turn–Off Delay Time \( V_{DD} = 30 \text{ V}, I_D = 0.2 \text{ A}, V_{GEN} = 10 \text{ V}, R_L = 150 \text{ \Omega}, R_{GEN} = 25 \text{ \Omega} \) | –  | 12.5 | 20  | ns   |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Short duration test pulse used to minimize self–heating effect.

TYPICAL PERFORMANCE CHARACTERISTICS

![Figure 1. On–Region Characteristics](image1)

![Figure 2. On–Resistance Variation with Gate Voltage and Drain Current](image2)
NOTES:
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMITIES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS L AND E APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.14 FROM THE TOP.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION HAT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADUS OF THE FOOT.

<table>
<thead>
<tr>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIM</td>
</tr>
<tr>
<td>a</td>
</tr>
<tr>
<td>A1</td>
</tr>
<tr>
<td>b</td>
</tr>
<tr>
<td>c</td>
</tr>
<tr>
<td>D</td>
</tr>
<tr>
<td>E1</td>
</tr>
<tr>
<td>E2</td>
</tr>
<tr>
<td>L</td>
</tr>
<tr>
<td>L2</td>
</tr>
<tr>
<td>m</td>
</tr>
<tr>
<td>bbb</td>
</tr>
<tr>
<td>ccc</td>
</tr>
</tbody>
</table>

XXX = Specific Device Code
M = Date Code*
* = Pb-Free Package

(Note: Microdot may be in either location)
*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free Indicator, "G" or microdot *, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2
<table>
<thead>
<tr>
<th>Style</th>
<th>Pins</th>
</tr>
</thead>
</table>
| Style 1: | 1. EMITTER 2  
2. BASE 2  
3. COLLECTOR 1  
4. EMITTER 1  
5. BASE 1  
6. COLLECTOR 2 |
| Style 2: | CANCELLED |
| Style 3: | CANCELLED |
| Style 4: | 1. CATHODE  
2. CATHODE  
3. COLLECTOR  
4. EMITTER  
5. BASE  
6. ANODE |
| Style 5: | 1. ANODE  
2. CATHODE  
3. COLLECTOR  
4. EMITTER  
5. BASE  
6. ANODE |
| Style 6: | PIN 1. ANODE  
2. N/C  
3. CATHODE 1  
4. ANODE 1  
5. N/C  
6. CATHODE 2 |
| Style 7: | PIN 1. SOURCE 2  
2. DRAIN 2  
3. GATE 1  
4. SOURCE 1  
5. DRAIN 1  
6. GATE 2 |
| Style 8: | CANCELLED |
| Style 9: | 1. EMITTER 2  
2. EMITTER 1  
3. COLLECTOR 1  
4. BASE 1  
5. BASE 2  
6. COLLECTOR 2 |
| Style 10: | 1. SOURCE 2  
2. SOURCE 1  
3. GATE 1  
4. DRAIN 1  
5. DRAIN 2  
6. GATE 2 |
| Style 11: | PIN 1. CATHODE  
2. CATHODE  
3. ANODE 1  
4. CATHODE 1  
5. CATHODE 1  
6. ANODE 2 |
| Style 12: | PIN 1. ANODE  
2. N/C  
3. COLLECTOR  
4. EMITTER  
5. BASE  
6. CATHODE |
| Style 13: | 1. ANODE  
2. GND  
3. COLLECTOR  
4. EMITTER  
5. BASE  
6. CATHODE |
| Style 14: | PIN 1. VREF  
2. GND  
3. GND  
4. IOUT  
5. VEN  
6. VCC |
| Style 15: | PIN 1. ANODE  
2. N/C  
3. ANODE 2  
4. CATHODE 2  
5. N/C  
6. CATHODE 1 |
| Style 16: | PIN 1. BASE 1  
2. EMITTER 2  
3. COLLECTOR 2  
4. BASE 2  
5. EMITTER 1  
6. COLLECTOR 1 |
| Style 17: | PIN 1. D1 (i)  
2. GND  
3. D2 (i)  
4. D2 (c)  
5. VBUS  
6. D1 (c) |
| Style 18: | PIN 1. VIN  
2. GND  
3. GND  
4. IOUT  
5. VEN  
6. VCC |

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.