onsemi is Delivering a Breakthrough in Power Integration

Embedded Power Platform

Architecture Overview

Power Demands Are Outgrowing Traditional System Architectures

Growing Power Demands

- AI, automotive and industrial markets are driving demand for more power in less space
- Designers must improve efficiency while managing heat, size and cost
- Power density is becoming a critical constraint in next-generation systems

Traditional Architectures Create Trade-Offs

- Electrical, mechanical and thermal systems are often optimized separately
- Improvements in one area can result in performance trade-offs elsewhere
- Sequential development adds complexity and can lead to costly late-stage design changes

Introducing Embedded Power Platform (EPP)

Silicon Embedded Package

Heterogenous die embedded into silicon and connected through wafer-level redistribution layers

Co-Developed by Design

Integrates electrical, mechanical and thermal considerations **from the outset**

Package as a Performance Enabler

Transforms the package from passive housing into an **active contributor to system performance**

Built to Scale

Technology-agnostic platform **supporting different applications**, different semiconductor materials and scalable across multiple power levels

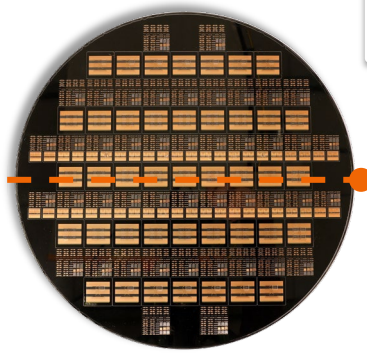
Embedded Power Platform

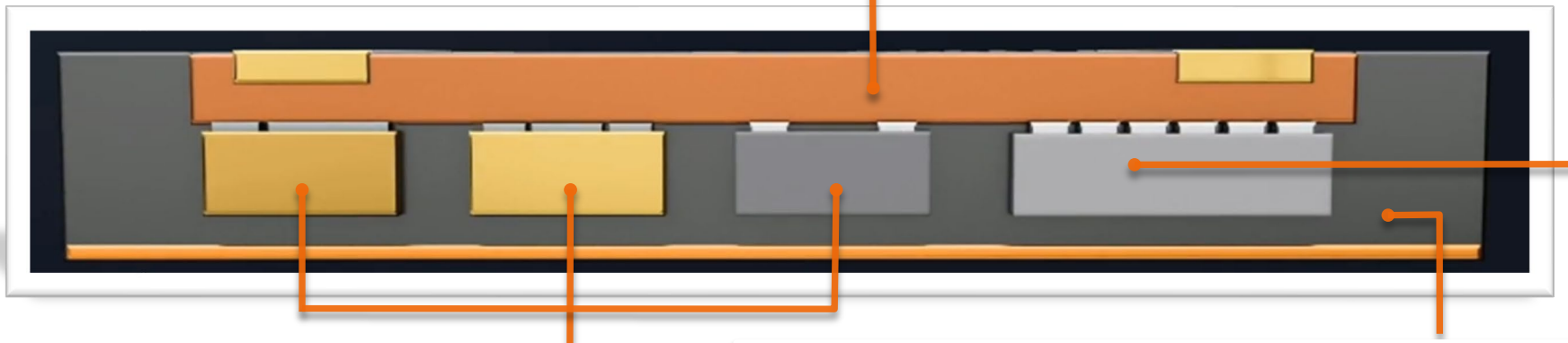
Wafer-Level Metallization

- Replaces wire bonds with precision redistribution layers
- Brings semiconductor-fab precision to electrical interconnects
- Reduces parasitic inductance
- Enables better device control and higher switching frequencies

Embedded Control Functions

- Integrates drivers and controllers with power devices
- Enables tighter electrical coupling
- Combines power and control within one platform
- Reduces system-level complexity





Embedded Power Die

- Supports Si, SiC, GaN and future technologies
- Enables configurable power-device combinations
- Adapts to different applications and power levels
- Evolves with semiconductor innovation

Silicon-Based Package

- Builds on established silicon design and fab infrastructure
- Leverages mature simulation and validation capabilities for faster time to market
- Provides a lower-resistance thermal path for better thermal performance
- Integrates high-voltage isolation within the package

EPP Brings Semiconductor Precision to Power System Integration

From Assembly to Wafer-Level Processing

EPP shifts critical integration steps from mechanically assembled structures into a controlled semiconductor fabrication environment

Wafer-Level Metallization

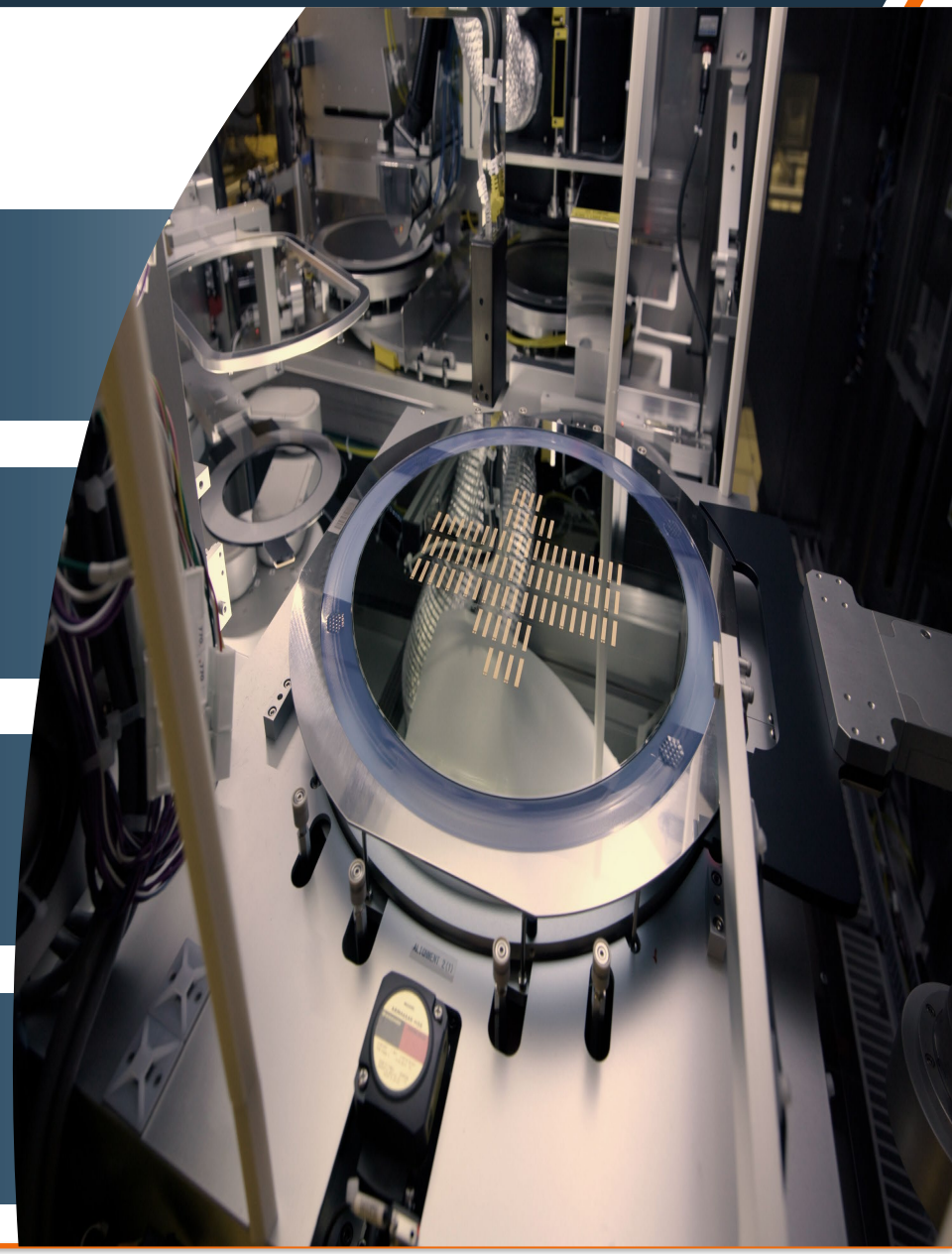
Precisely patterned redistribution layers connect embedded power die without traditional wire-bond interconnects reducing parasitic inductance and improving switching control

Heterogeneous Die Integration

Configurable combinations of power transistors, gate drivers, controllers and other semiconductor functions can be embedded and interconnected

Integrated Architecture

Embedded die, metallization and high-voltage isolation are brought together within a common silicon-based platform



Higher Power Density Through Electrical, Thermal and Mechanical Co-Optimization

Thermal Performance

A silicon-based architecture and **full-footprint thermal conduction** improve heat dissipation and support higher continuous power operation

Embedded Isolation

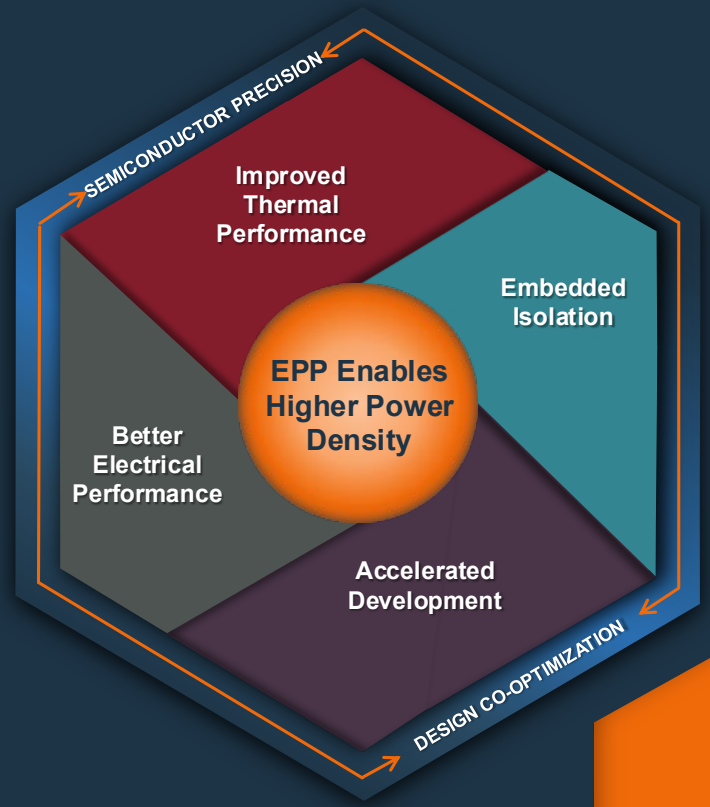
Integrated high-voltage isolation reduces reliance on thermally inefficient insulating materials while enabling more compact and highly integrated power architectures

Electrical Performance

Wafer-level redistribution layers and shorter, more controlled electrical paths **reduce parasitic inductance**, enabling better device control and higher switching frequencies

Fast Development

Digital twin simulation and multi-physics co-optimization enable **rapid design iteration**, reducing hardware builds, shortening development cycles and accelerating time to market.

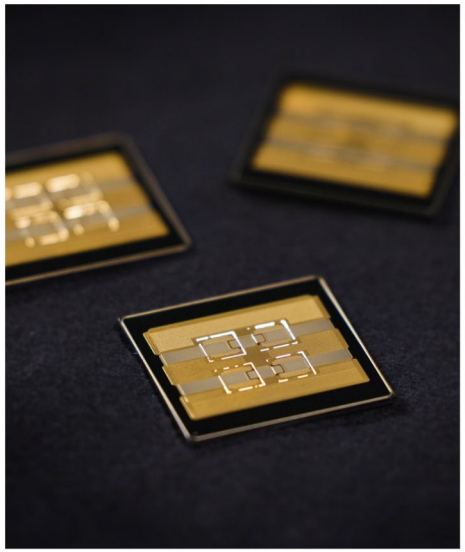


Unlock More from Today's Technologies

EPP co-optimizes electrical, thermal and mechanical performance to maximize the capability of existing power semiconductor technologies

A New Path to Higher Power Density

System-level co-optimization enables greater power density without relying solely on advancements in semiconductor devices



Technology-Agnostic by Design

A common architecture supports current and future generations of silicon, silicon carbide, gallium nitride and emerging semiconductor technologies

Built on onsemi's Core Strengths

Wafer-level integration applies semiconductor manufacturing precision to power system design, bringing more of the value creation into the fab

Unlocking More From Every Generation of Power Technology

Enabling the Next Generation of Power Systems

Vehicle Electrification

Smarter, Lighter Vehicle Architectures

- Lower inductance enabling faster switching frequencies
- Improved thermal performance
- Smaller, lighter, and more efficient traction inverter systems
- Scalable architecture across vehicle platforms and power levels

AI Power Infrastructure

More Compute in Less Space

- Higher power density frees valuable board and rack space
- Full-footprint thermal conduction enables thermally efficient designs
- Improved thermal performance supports growing energy demands
- Enables compact, highly integrated power delivery architectures

Beyond AI and EV

A Platform for Innovation

- Fast-charging infrastructure
- Energy storage systems
- Grid modernization
- Industrial Automation
- Future semiconductor technologies

One Architecture, Multiple Industries, One Platform for Innovation

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