FAN9672/FAN9673 Tips and Tricks

AND9925/D

INTRODUCTION

FAN967x is multi−channel interleaved continuous−conduction−mode (CCM) power−factor−correction (PFC) controller. It is intrinsically an average−current−mode PWM controller that makes average inductor current track real−time input−voltage waveform. FAN9672 has two gate outputs, and FAN9673 has three, which control three parallel−connected boost converters. By making gate−drive signals in each channel interleaved, it reduces switching ripple of both input current and output voltage.

Since FAN967x has abundant of functionalities to make PFC pre−regulator (PFC converter) works flawlessly, functional description and design guideline on data sheets [1−2] and another application note [3] were written more commonly, focusing on making the design process easier to follow. They aim at most typical applications: universal input range (90 to 264 Vac) and European input range (180 to 264 Vac) with design equations simplified according to pre−assumed designed values.

This application note means to explain those functions in terms that are more general. Information here makes readers understand this controller better. Moreover, when one wants to design PFC pre−regulator beyond the limitation set by the pre−assumed designed values, these pieces of information are beneficial for one to play around with this controller.

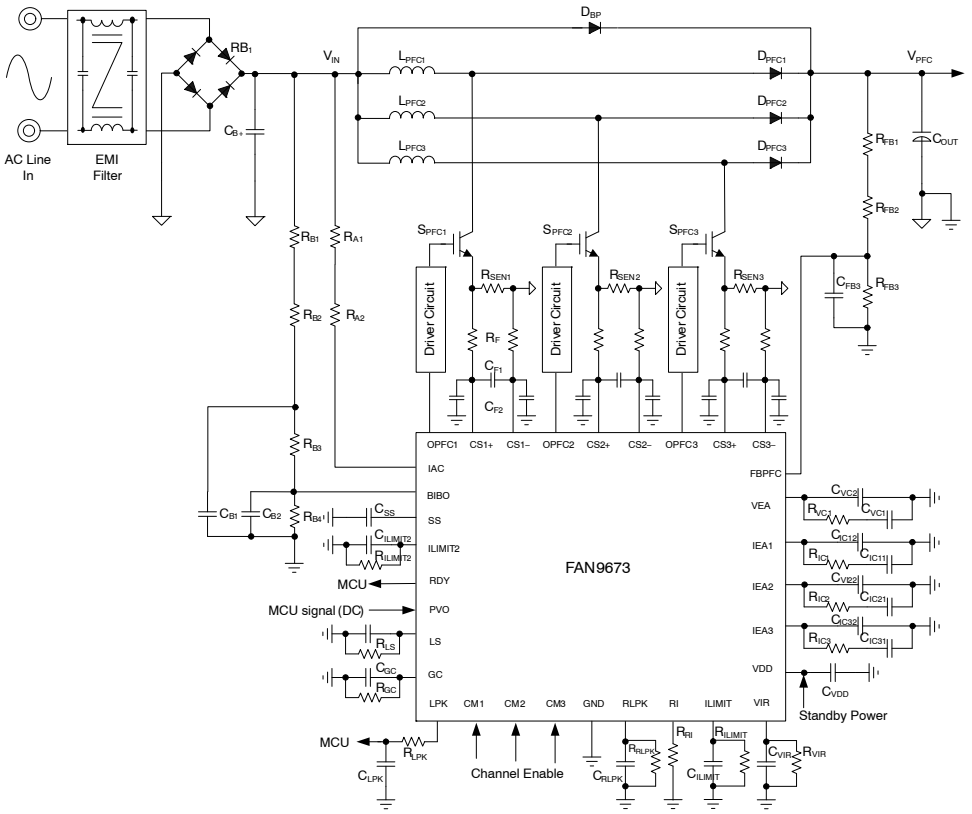

Figure 1. Typical Application Circuit of FAN9673

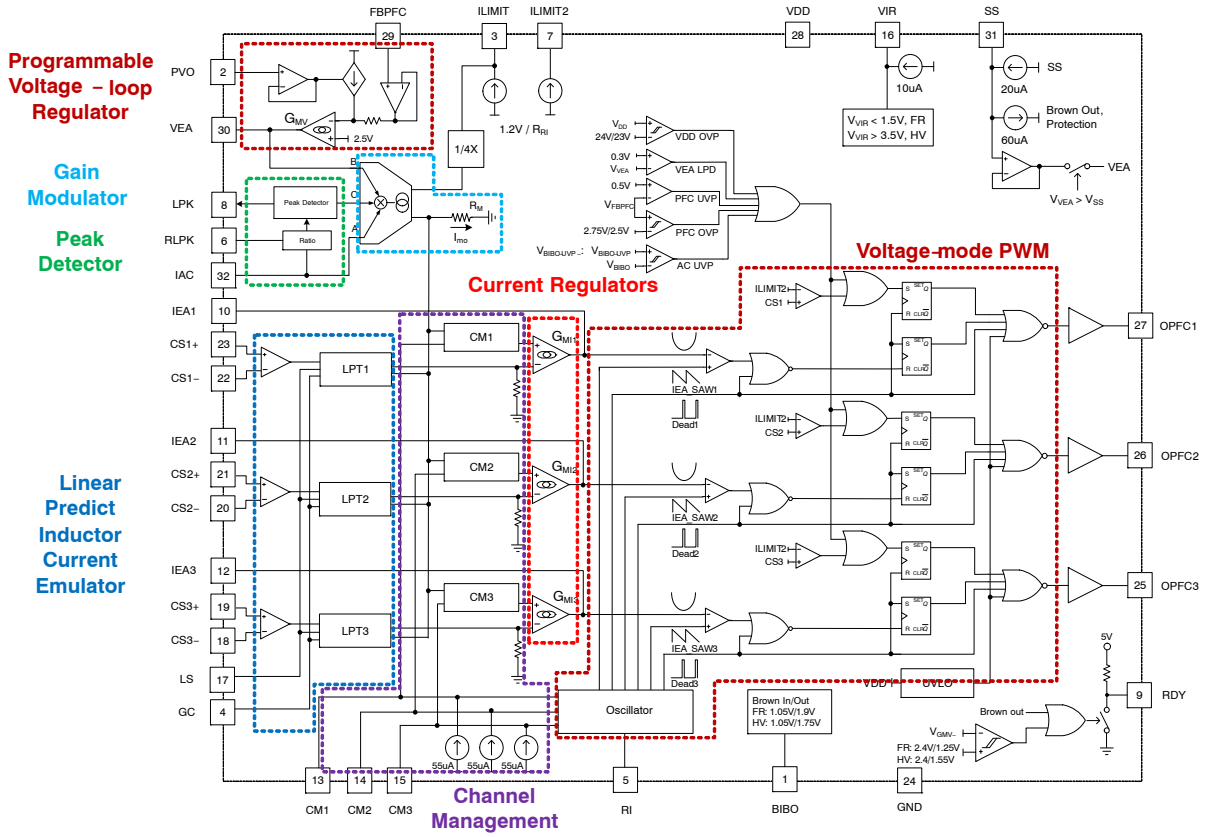

Figure 2. Simplified Block Diagram of FAN967x

Overview of Block Diagram

Figure 2 shows the block diagram of FAN9673. It is the same drawing in the datasheet of FAN9673, except that its functional purposes group related blocks. Block diagram of FAN9672 is almost identical to this one, except it reduces channel number by one.

FAN967x is a multi−channel interleaved pulse−width modulation (PWM) controller, which modulates its duty to make inductor current track input−voltage waveform. The PWM block receives control voltages generated by $G_{MI1\sim3}$. $G_{MI1\sim3}$ are trans−conductance error amplifiers, used to make inductor current of each channel track a current command. These G_{MI} generate signals IEA1~3, serving as control voltage of the PWM block.

Three sets of differential−input CS pins sense inductor currents. Current−sense (CS) signals are then further processed by linear−predict (LPT) blocks, explained later.

An FBPFC pin senses an output voltage of the PFC stage. Another trans−conductance error amplifier G_{MV} takes the FBPFC signal. G_{MV} is used to regulate FBPFC voltage. Some additional elements are inserted between FBPFC and G_{MV} input to change regulation target for the FBPFC other than 2.5 V. G_{MV} generates an error signal VEA, feeding into a gain modulator section.

A gain modulator generates the current command for the G_{MI}. It takes signals that represent the real−time value of input voltage, the peak of input voltage and the VEA. The current command is proportional to the VEA signal. High current−command signal makes high regulation target for inductor currents, which leads to the high input current. As a result, VEA voltage is proportional to the operating wattage condition of the PFC power converter.

Between the gain modulator and the G_{MI} error amplifiers, there are channel−management blocks. This block acts as a gain for reducing current command signal fed into the G_{MI} error amplifiers for managing power in each PFC channel.

Figure 3 illustrates the signal flow of the PFC control mechanism described above. Other blocks in Figure 2 that are not mentioned in this section are peripherals for parameters setting, status indication, and protections.

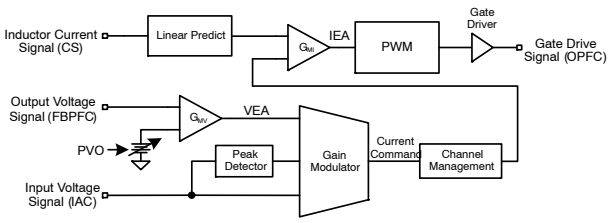

Figure 3. Signal Flow of PFC Control Mechanism

Input Sensing and Peak Detection

FAN967x detects input voltage from IAC pin. IAC pin is a current−mirror input. Its input impedance is much smaller than an external R_{IAC} resistor, making its input current as

$$I_{IAC} = V_{IN}/R_{IAC} \quad \text{(eq. 1)}$$

where V_{IN} is the real−time input voltage. By considering rectified sinusoidal input for the PFC stage, (eq. 1) can be re−write as

$$I_{IAC}(t) = \frac{V_{IN.PEAK}}{R_{IAC}} \cdot |\sin(\omega \cdot t)| \quad \text{(eq. 2)}$$

where ω stands for angular frequency of the ac−input voltage.

An RLPK pin mirrors I_{IAC} as a sourcing current. With a resistor connecting to the RLPK pin, the input−voltage information in a current−signal format, I_{IAC}, becomes a voltage signal, V_{RLPK}.

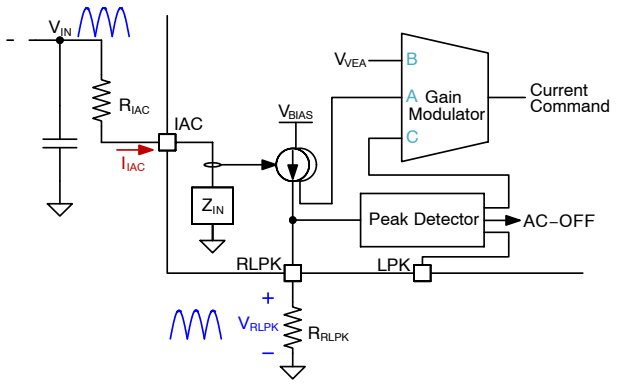

Figure 4. Block of Input Voltage Detection

V_{RLPK} replicates the shape of the input−voltage waveform. A peak detector block processes V_{RLPK} signal to track its cycle−by−cycle peak value. The basic algorithm of peak detector is as depicted in Figure 6. An intermittent signal $V_{PEAK-HOLD}$ traces rising V_{RLPK} and hold the peak value until triggering of a reset event. The reset is triggered when V_{RLPK} keeps lower than $V_{PEAK-HOLD}$*0.95 for a t_{UPDATE} duration. Upon reset is triggered, V_{PEAK} updates with the last $V_{PEAK-HOLD}$ value. This algorithm is designed to update V_{PEAK} at the valley of V_{IN} waveform, so to minimize disturbance of PFC operation due to V_{PEAK} variation. The V_{PEAK} signal is then sent to LPK pin and gain modulator.

When the peak of V_{IN} suddenly increases, another mechanism update V_{PEAK} in a much faster pace by detecting $V_{RLPK} > V_{PEAK} + 0.2$ V, which is also depicted in Figure 6. This mechanism acts only when V_{RLPK} exceeds V_{PEAK} by 0.2 V. However if V_{RLPK} is higher than V_{PEAK} but not that much, V_{PEAK} will not be updated until the criterion of $V_{RLPK} < V_{PEAK-HOLD}$*0.95 is satisfied.

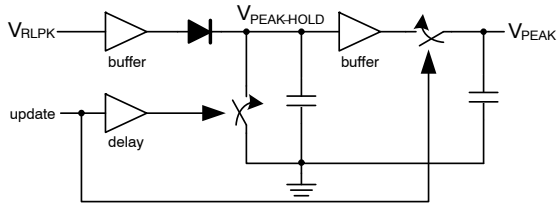

Figure 5. Block of Input Voltage Detection

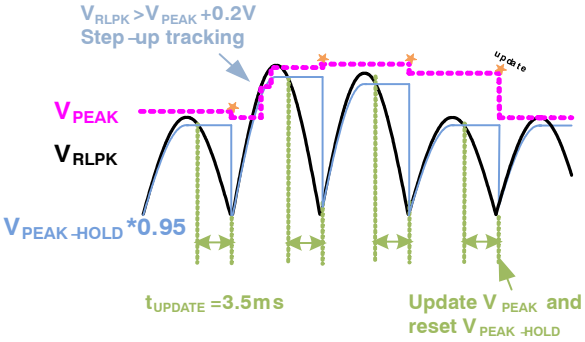

Figure 6. Algorithm of Peak Detector

In an extreme AC−input sag situation, FAN967x blanks updating of V_{PEAK}. This AC−OFF mechanism is as depicted in Figure 7. When V_{RLPK} keeps lower than a V_{AC-OFF} for t_{AC-OFF}, FAN967x triggers AC−OFF. AC−OFF is released when $V_{RLPK} > V_{AC-ON}$ while updating of V_{PEAK} keeps blanking for the following 5 ms. It is worth noting that the IEA signal, which is the control voltage of PWM, is pulled low during the AC−OFF situation.

Timing specification in Figure 6 and Figure 7 are designed values in FAN967x. These values are optimized for typical 50~60 Hz ac input.

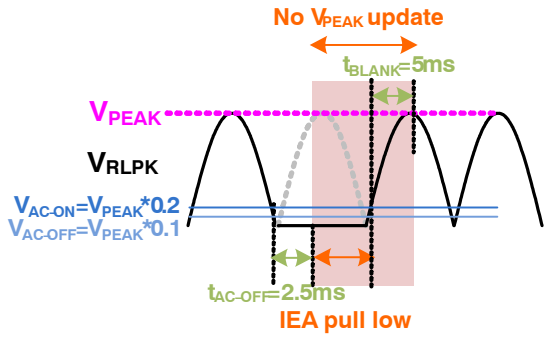

Figure 7. Blanking V_{PEAK} Update During AC−OFF

FAN967x generates the V_{LPK} signal to be utilized by other circuitries, such as a microcontroller unit (MCU) for acquiring input−voltage information. LPK pin can provide a signal to a high input impedance port. LPK pin's output

impedance is around 5 kΩ. Sinking too much of current from LPK pin makes its voltage drop.

There is a known situation that a drop in V_{LPK} signal for a short time can happen. We observed the phenomenon when PFC converter is designed to work in low−power detection mode ($V_{VEA} < V_{VEA-OFF}$), or burst mode, with a high input power. V_{IN} can be a little bit higher when input current (I_{IN}) cuts off. The slightly elevated V_{IN} may make the updating of V_{PEAK} trigger two times during one valley of rectified V_{AC}. That makes V_{PEAK} updated with a wrong value. It recovers within one−fourth of the ac−input period. If LPK signal is used by other circuitry to have protection based on the input voltage detection, consider adding a blanking time more than one−fourth of the ac−input period for a smoother operation.

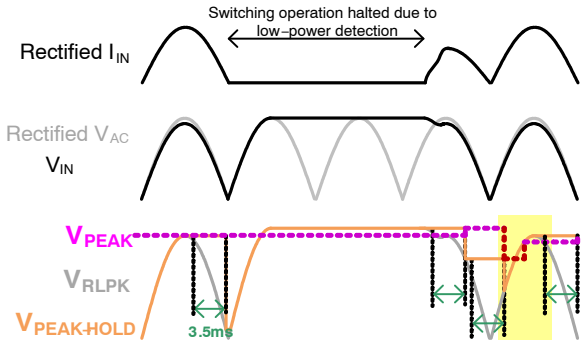

Figure 8. A situation That Makes V_{PEAK} (V_{LPK}) Drop

Linear−Predict Function for Rebuilding Inductor Current

Constant−frequency CCM PFC controls its average inductor current to track input−voltage waveform. CS pin of FAN967x is designed to simplify current−sense circuitry. You can directly put current−sense resistor at the source terminal of power switches of a boost converter. With this connection, the controller gets the inductor current information when the power switch is in ON state. Since controlling a CCM PFC requires average inductor current information, FAN967x implements a linear−predict function for the reconstruction of the inductor current signal.

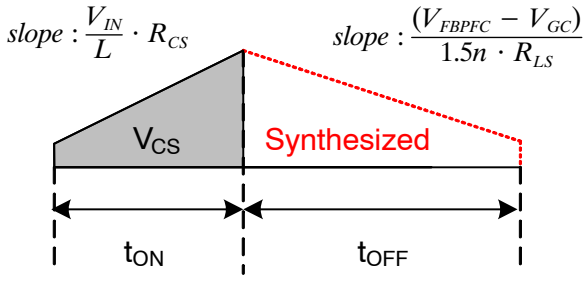

Figure 9. Linear−Predict Function

A linear−predict (LPT) block manipulates V_{CS} before feeding into the G_{MI} error amplifier. The current signal is the same as V_{CS} with OPFC is in on state. When OPFC is off, the LPT block generates a synthesized part of the current signal by discharging a capacitor from the last peak value of V_{CS}.

If the inductor current is sensed by a current−sense resistor R_{CS} all the time, the slope of the sensed signal during t_{OFF} should be

$$\frac{(V_{OUT} - V_{IN}) \cdot R_{CS}}{L} \quad \text{(eq. 3)}$$

In the LPT block, the slope of the synthesized waveform is

$$\frac{(V_{FBPFC} - V_{GC})}{1.5n \cdot R_{LS}} \quad \text{(eq. 4)}$$

V_{FBPFC} represents the output voltage. GC pin is similar to RLPK pin, which gets a sourcing current mirrored from IAC pin. In other words, V_{GC} contains the input−voltage information. By putting a resistor R_{GC} on GC pin, V_{GC}−to−V_{IN} ratio is adjusted to be identical with V_{FBPFC}−to−V_{OUT} ratio. As a result, $(V_{FBPFC} - V_{GC})$ become a replicate of $(V_{OUT} - V_{IN})$. After V_{GC} level being correctly set, R_{LS} is adjusted to make the slope of the synthesized waveform (eq. 3) matched with pseudo sensed inductor current waveform (eq 4). In short, the GC pin is used to set a ratio, making input voltage signal comparable with output voltage signal; and, LS pin is used to set the slope of synthesized signal, mimicking behavior of the actual inductance applied in the boost converter. The description above implies how the design equations of R_{GC} and R_{LS} are derived.

$$R_{GC} = \frac{R_{FB3}}{R_{FB1} + R_{FB2} + R_{FB3}} \cdot \frac{R_{IAC}}{\begin{bmatrix} 1, \text{if } V_{IR} < 1.5 \\ 2, \text{if } V_{IR} > 3.5 \end{bmatrix}} \quad \text{(eq. 5)}$$

$$R_{LS} = \frac{R_{FB3}}{R_{FB1} + R_{FB2} + R_{FB3}} \cdot \frac{L}{R_{CS}} \cdot \frac{1}{1.5n} \quad \text{(eq. 6)}$$

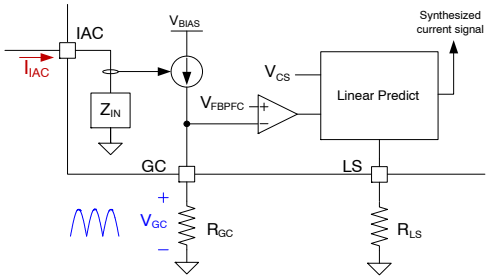

Figure 10. Simplified Block Diagram of Linear−Predict Function

Common−mode and Differential−mode Filter for Current−Sense Signal

Because of multi−channel nature, FAN967x controller is hard to stay close to current−sense (CS) resistors. Long PCB trace between the CS resistors and the controller make the CS signals prone to be noisy. FAN967x takes the current−sense signals as differential−input signals which reject the induced common−mode noise on the PCB trace.

Although differential input rejects common−mode noise inherently, the common−mode voltage on each of the input pin still affects the operation of the controller. A common−mode filter is generally implemented to filter out the common−mode noise. Figure 11. shows a schematic of the common−mode filter. Bandwidth of the common−mode filter is

$$f_{BW-comon} = \frac{1}{2\pi \cdot R_f \cdot C_C} \quad \text{(eq. 7)}$$

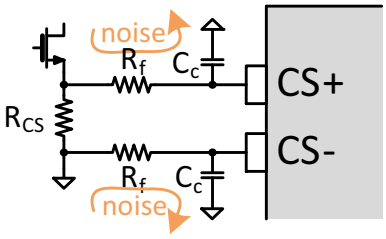

Figure 11. Common−mode Filter for CS Pin

Due to a mismatch between the resistors and capacitors in the common−mode filter, common−mode noise may be filtered differently between CS+ and CS−. As a result, a differential−mode noise appears on the CS signals. To tackle with the differential−mode noise, we add a capacitor to filter out the differential−mode noise.

With the resultant CS filter in Figure 12, which combines common−mode and differential−mode filters, the bandwidth of a low−pass filter for the differential CS signals becomes

$$f_{BW-diff} = \frac{1}{2\pi \cdot 2R_f \cdot \left(C_d + \frac{1}{2} \cdot C_c\right)} \quad \text{(eq. 8)}$$

The bandwidth of the filter should be set based on noise that is generated in actual design result. In a 5 kW reference design for FAN9673 with 40 kHz of switching frequency, we set $f_{BW-common}$ at 154 kHz and $f_{BW-diff}$ at 51.3 kHz.

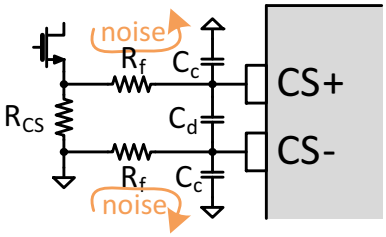

Figure 12. CS Pin Filter

Effect of Input Range Setting

VIR pin of FAN967x sets two different modes that optimize for universal input range and European input range, respectively. This pin sources a constant current. A resistance value connecting between VIR and GND decides the voltage on the VIR pin. The voltage on the VIR pin needs to be set higher than 3.5 V or lower than 1.5 V. Avoid anything in between.

The setting on the VIR pin changes some internal signals of FAN967x, which are collected in Table 1. A K_{RLPK} constant appears in the table. According to the test cases of V_{LPK}, which can be found in electrical characteristics in the datasheet, K_{RLPK} is 2.465.

Table 1. Effects of VIR Setting

V_{VIR}	< 1.5 V	> 3.5 V
Optimized for	Universal−input range (90~264 Vac)	European−input range (180~264 Vac)
Recommended R_{IAC}	6 MΩ	12 MΩ
V_{BIBO} Brown−in Level	1.90 V	1.75 V
V_{BIBO} Brown−out Level	1.05 V	1.05 V
V_{FBPFC} for RDY = HIGH	2.4 V	2.4 V
V_{FBPFC} for RDY = LOW	1.25 V	1.55 V
I_{RLPK}	K_{RLPK}*I_{IAC}	2*K_{RLPK}*I_{IAC}
V_{LPK}	Peak of 2*K_{RLPK}*I_{IAC}*R_{RLPK}	Peak of 4*K_{RLPK}*I_{IAC}*R_{RLPK}
“C” input of gain modulator	Peak of 2*K_{RLPK}*I_{IAC}*R_{RLPK}	Peak of 2*K_{RLPK}*I_{IAC}*R_{RLPK}
I_{GC}	I_{IAC}	2*I_{IAC}

Signals of the Gain Modulator

Gain modulator generates a current command for inductor current to follow. Inductor current of PFC converter should have the same shape of input voltage, be proportional to error signal V_{VEA}, and have magnitude inverse−proportional to the magnitude of the input voltage. In this condition, the current command decreases when the amplitude of input voltage increases without waiting for the output voltage to respond. That is, input power is kept unchanged by a feed−forward control. More, V_{VEA} is ideally decided by power requirement and less related to fluctuation in input voltage.

To realize the characteristics mentioned above, gain modulator is designed to have its output signal proportional to $A \cdot B/C^2$, where A, B and C are its input signals depicted in Figure 13.

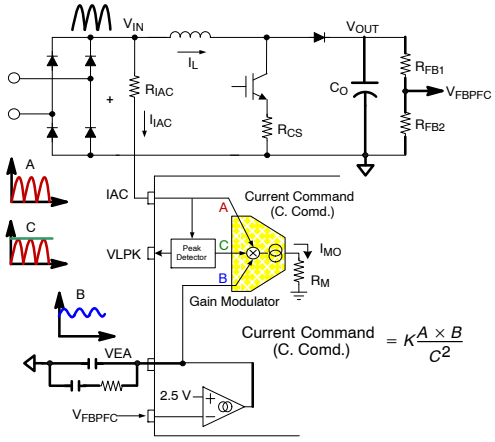

Figure 13. Gain Modulator

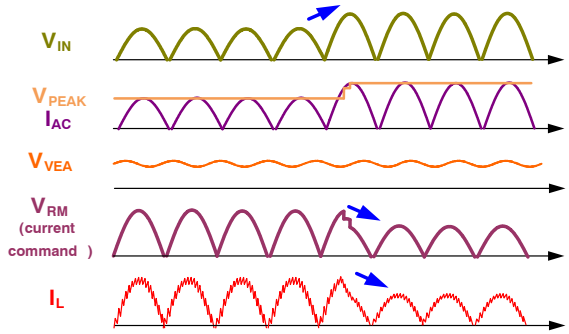

Figure 14. Behavior of Gain Modulator in Line Transient

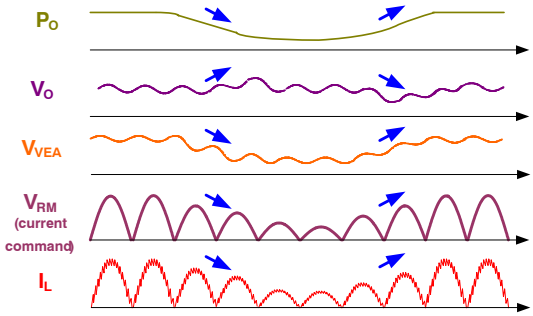

Figure 15. Behavior of Gain Modulator in Load Transient

Figure 13. describes the output of gain modulator as a current signal, which is converted to a voltage signal by a resistor R_M. So, current command is named as V_{RM}, meaning voltage across the R_M resistor.

$$V_{RM} = K \cdot \frac{A \cdot B}{C^2} \cdot R_M \qquad \text{(eq. 9)}$$

Replacing A, B, and C terms in (eq. 9) by its real input signals, V_{RM} can be re−write as

$$V_{RM}(t) = \frac{K_{RM} \cdot I_{IAC.PEAK} \cdot (V_{VEA} - 0.6) \cdot |\sin(\omega \cdot t)|}{(2 \cdot K_{RLPK} \cdot I_{IAC.PEAK} \cdot R_{RLPK})^2} \qquad \text{(eq. 10)}$$

In (eq. 10), a K_{RM} constant replaced $K \cdot R_M$, and $I_{IAC.PEAK}$ represents the peak value of I_{AC} signal in (eq. 2). Electrical characteristics table on the datasheet provides several test cases of V_{RM}. The test cases set R_{RLPK} as 12.4 kΩ, which makes $V_{LPK} = V_{IN.PEAK}/100$ when R_{IAC} is set according to Table 1. More, V_{FBPFC} = 2.25 V makes V_{VEA} be pulled high. Gain modulator reacts to V_{VEA} with a linear range of 0.6 to 5.6 V with a 0.6 V voltage shift. Calculation from those test cases shows that K_{RM} is about 6000. Note that the linear range of V_{RM} is up to 0.8, which may happen in the lowest input voltage condition.

V_{RM} is inverse proportional to $I_{IAC.PEAK}$. When the input voltage increases, $I_{IAC.PEAK}$ increases as well. As a result, V_{RM} reduces to a lower value. Ideally, V_{VEA} should keep unchanged, if only the input voltage changes but the loading is unchanged. In actual implementation, V_{VEA} may still decrease slightly due to propagation delays in control signal, such as gate−driver delay and CS−pin filter delay.

Since V_{CS} tracks the current command V_{RM}, V_{RM} equation and the maximum wattage in the design specification of the PFC converter determine R_{CS} as

$$R_{CS} = \frac{K_{RM} \cdot R_{IAC} \cdot (V_{VEA.MAX} - 0.6)}{8 \cdot K_{RLPK}^2 \cdot R_{RLPK}^2 \cdot P_{MAX}/N_{CH}} \qquad \text{(eq. 11)}$$

where P_{MAX} is specified maximum power of PFC converter, and N_{CH} is the number of channels of the multi−channel PFC converter. $V_{VEA.MAX}$ is a maximum V_{VEA} voltage under P_{MAX} condition. $V_{VEA.MAX}$ is generally set around 4~5 V. Set $V_{VEA.MAX}$ properly by setting R_{CS}, so that the control signals in FAN967x can be high enough to achieve a stable operation.

In a universal−input design, V_{RM} tends to be smaller than when the PFC converter operates in high−line input conditions. As shown in Figure 16, V_{RM} in system set to R_{IAC} = 12 MΩ and V_{VIR} = 5 V for European input range becomes higher than set to R_{IAC} = 6 MΩ and V_{VIR} = 0 V, which has a better signal−to−noise ratio and better usage of its resolution. At the same time, since doubled R_{IAC} make I_{IAC} reduce to half under the same V_{IN} condition, FAN967x doubles I_{RLPK} and I_{GC} so that R_{RLPK} and R_{GC} settings can be the same.

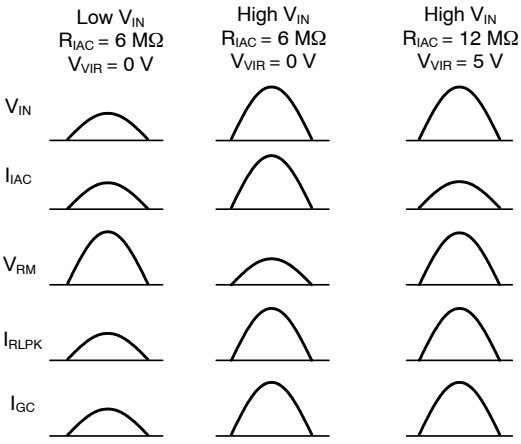

Figure 16. V_{IN} Related Signals under Different VIR and R_{IAC} Setting

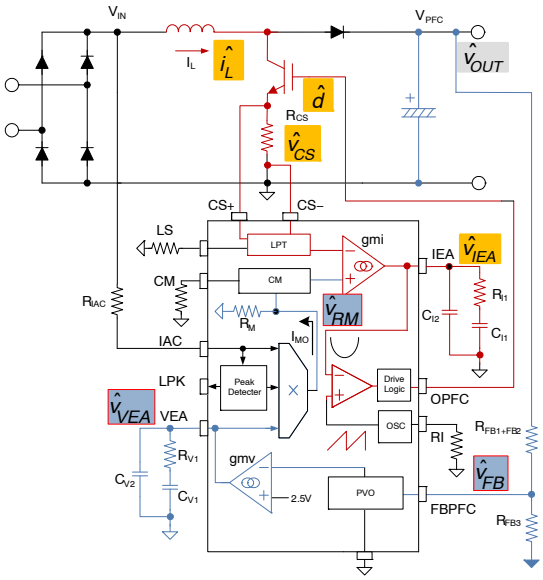

Figure 17. Control Loop of FAN967x

Figure 17 shows a full view of all blocks involved in PFC control. The figure shows only one channel for simplicity. PVO block's effect is to change effective reference voltage for FBPFC, so it does not affect the control signal in small−signal point of view. In full load condition, channel management (CM) block is no more than a unity−gain buffer, so we neglect it in analyzing the control loops.

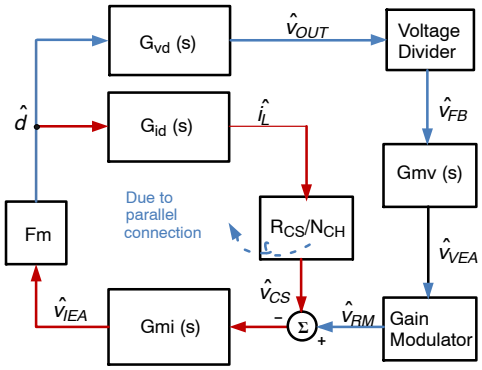

Figure 18. Control Block Diagram of FAN967x

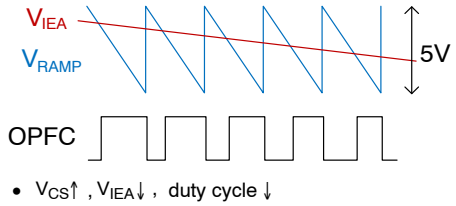

Figure 19. PWM in FAN967x

Current−Tracking Loop

There are two feedback loops in the control block diagram [4], one is for making inductor current track the current command. The gain of this loop is

$$T_I(s) \equiv G_{id}(s) \cdot R_{CS} \cdot G_{mi}(s) \cdot F_m \qquad \text{(eq. 12)}$$

where $G_{id}(s)$ is duty−cycle−to−inductor−current transfer function of boost converter [5], $G_{mi}(s)$ represents G_{MI} error amplifier and setting on IEA pins, and F_m is modulation gain of PWM. As a voltage−mode PWM, modulation gain is the reciprocal of the amplitude of a ramp signal, V_{RAMP}, depicted in Figure 19.

$$F_m = 1/V_{RAMP} \qquad \text{(eq. 13)}$$

$G_{id}(s)$ in [5] is repeated as (eq. 14), where C_{OUT} is capacitance of the output capacitor, r_C is equivalent series resistance of the output capacitor, R_{LOAD} is equivalent resistance of the output loading, L is inductance of power inductor in each channel, and D is duty cycle of OPFC signal. D = (1− V_{IN}/V_{OUT}) By assuming that r_L and r_C are small and R_{LOAD} is large, (eq. 14) can be simplified as (eq. 15).

$$G_{id}(s) \equiv \frac{\hat{i}_L}{d} = \frac{V_{OUT}}{L} \cdot \frac{R_{LOAD} + 2 \cdot r_c}{R_{LOAD} + r_c} \cdot \frac{s + \frac{1}{C \cdot (R_{LOAD}/2 + r_c)}}{s^2 + \left[\frac{C_{OUT}\left[r_L(R_{LOAD}+r_C) + R_{LOAD}r_C(1-D)^2\right] + L}{L \cdot C_{OUT}(R_{LOAD}+r_C)}\right] s + \frac{(1-D)^2 R_{LOAD} + r_L}{L \cdot C_{OUT}(R_{LOAD}+r_C)}} \qquad \text{(eq. 14)}$$

$$G_{id}(s) = \frac{V_{OUT}}{L} \cdot \frac{s}{s^2 + \frac{(1-D)^2}{L \cdot C_{OUT}}} \qquad \text{(eq. 15)}$$

To make inductor track current command well, the bandwidth of the current−tracking loop need to set high enough. When the complex pole formed by L and C_{OUT} is at a frequency much lower than the control bandwidth of $T_I(s)$, we can further simplify $G_{id}(s)$ as

$$G_{id}(s) = \frac{V_{OUT}}{s \cdot L} \qquad \text{(eq. 16)}$$

With (eq. 13) and (eq. 16), (eq. 12) can be simplified as (eq. 17), which is the same as the design equation in application note AN4165/D.

$$T_I(s) = \frac{V_{OUT} \cdot R_{CS}}{s \cdot L \cdot V_{RAMP}} \cdot G_{mi}(s) \qquad \text{(eq. 17)}$$

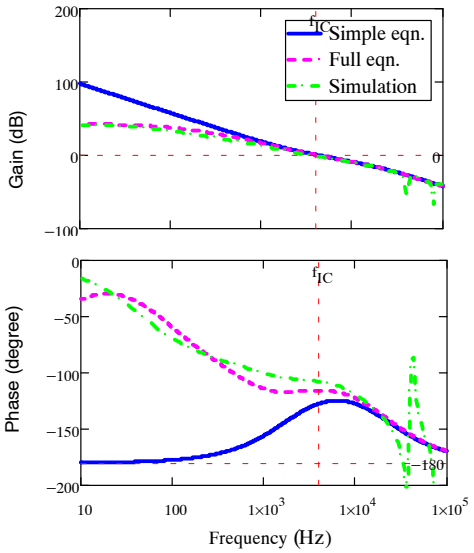

Figure 20. Comparison of $T_I(s)$ Equations

Figure 20 shows comparison data resulted in both simplified (eq. 17), in full (eq. 14), and via simulation. The simplification removes low−frequency components and focus on frequency range around control bandwidth.

Voltage−Regulation Loop

Except for the current−tracking loop, there is another control loop for regulating the output voltage. By breaking the loop at the position of $\ddot{v}_{FB}$ in Figure 18, we can derive the loop gain as (eq. 18), where G_{MOD} is the effective gain of the gain modulator, $G_{vd}(s)$ is duty−cycle−to−output−voltage transfer function of boost converter, V_{FBPFC}/V_{OUT} is the effective gain of a voltage divider for PFC output voltage, and $G_{mv}(s)$ represents G_{MV} error amplifier. $T_I(s)$ in the denominator is divided by N_{CH}. Because all the channels are connected in parallel, so as the current−tracking loop.

Bandwidth of the voltage−regulation loop is generally lower in PFC converters. Within the bandwidth of the voltage−regulation loop, $T_I(s)$ is much larger than one. So, terms in (eq. 18) that relates to the boost power stage and the current−tracking loop can be manipulated as (eq. 19). $G_{vd}(s)$ in [4] is repeated as (eq. 20).

By neglecting r_C and r_L, $G_{id}(s)$ in (eq. 14) can be simplified as (eq. 21). Substituting (eq. 20) and (eq. 21) into (eq. 19) results in (eq. 22). Again, assuming r_C is small and R_{LOAD} is large, we can simplify (eq. 22) as (eq. 23).

G_{MOD} can be derived from (eq. 10) as (eq. 24). Substituting (eq. 11), (eq. 22), and (eq. 24) into (eq. 18), loop gain of the voltage−regulation loop can be written as (eq. 25).

$$\text{Loopgain}(s) = G_{MOD} \cdot \frac{G_{mi(s)} \cdot F_m}{1 + T_I(s)/N_{CH}} \cdot G_{vd}(s) \cdot \frac{V_{FBPFC}}{V_{OUT}} \cdot G_{mv}(s) \qquad \text{(eq. 18)}$$

$$\frac{G_{mi}(s) \cdot F_m}{1 + T_I(s)/N_{CH}} \cdot G_{vd}(s) = \frac{G_{mi}(s) \cdot F_m \cdot G_{vd}(s)}{G_{id}(s) \cdot R_{CS} \cdot G_{mi}(s) \cdot F_m/N_{CH}} = \frac{G_{vd}(s)}{G_{id}(s)} \cdot \frac{N_{CH}}{R_{CS}} \qquad \text{(eq. 19)}$$

$$G_{vd}(s) = \frac{V_{IN}}{L \cdot C_{OUT}} \cdot \frac{(1 + s \cdot C_{OUT} \cdot r_C)\left(1 - \frac{s \cdot L}{(1-D)^2 \cdot R_{LOAD}}\right)}{s^2 + \frac{1}{C_{OUT} \cdot R_{LOAD}} s + \frac{(1-D)^2}{L \cdot C_{OUT}}} \qquad \text{(eq. 20)}$$

$$G_{id}(s) = \frac{V_{OUT}}{L} \cdot \frac{s + \frac{1}{C_{OUT} \cdot (R_{LOAD}/2)}}{s^2 + \frac{1}{C_{OUT} \cdot R_{LOAD}} s + \frac{(1-D)^2}{L \cdot C_{OUT}}} \qquad \text{(eq. 21)}$$

$$\frac{G_{vd}(s)}{G_{id}(s)} \cdot \frac{N_{CH}}{R_{CS}} = \frac{V_{IN}}{V_{OUT} \cdot C_{OUT}} \cdot \frac{(1 + s \cdot C_{OUT} \cdot r_C)\left(1 - \frac{s \cdot L}{(1-D)^2 \cdot R_{LOAD}}\right)}{s + \frac{1}{C_{OUT} \cdot (R_{LOAD}/2)}} \cdot \frac{N_{CH}}{R_{CS}} \qquad \text{(eq. 22)}$$

$$\frac{G_{vd}(s)}{G_{id}(s)} \cdot \frac{N_{CH}}{R_{CS}} = \frac{V_{IN}}{V_{OUT}} \cdot \frac{1}{s \cdot C_{OUT}} \cdot \frac{N_{CH}}{R_{CS}} \qquad \text{(eq. 23)}$$

$$G_{MOD}(t) \equiv \frac{\ddot{v}_{RM}}{\ddot{v}_{VEA}} = \frac{K_{RM} \cdot I_{IAC.PEAK} \cdot |\sin(\omega t)|}{\left(2 \cdot K_{RLPK} \cdot I_{IAC.PEAK} \cdot R_{RLPK}\right)^2} = \frac{K_{RM} \cdot R_{IAC} \cdot V_{IN.PEAK} \cdot |\sin(\omega t)|}{8 K_{RLPK}^2 R_{RLPK}^2 V_{IN.RMS}^2} \qquad \text{(eq. 24)}$$

$$\text{Loopgain}(s) = \frac{(V_{IN.PEAK} \cdot |\sin(\omega t)|)^2}{V_{IN.RMS}^{\ 2}} \cdot \frac{1}{V_{OUT}} \cdot \frac{1}{s \cdot C_{OUT}} \cdot \frac{P_{MAX}}{(V_{VEA.MAX} - 0.6)} \cdot \frac{V_{FBPFC}}{V_{OUT}} \cdot G_{mv}(s) \quad \text{(eq. 25)}$$

$$\text{Loopgain}(s)_{ac-cycle} = \frac{1}{s \cdot C_{OUT}} \cdot \frac{P_{MAX} \cdot I_{OUT}}{(V_{VEA.MAX} - 0.6) \cdot V_{OUT} \cdot I_{OUT}} \cdot \frac{V_{FBPFC}}{V_{OUT}} \cdot G_{mv}(s)$$

$$= \frac{1}{s \cdot C_{OUT}} \cdot \frac{P_{MAX} \cdot I_{OUT}}{(V_{VEA.MAX} - 0.6) \cdot P_{OUT}} \cdot \frac{V_{FBPFC}}{V_{OUT}} \cdot G_{mv}(s) = \frac{1}{s \cdot C_{OUT}} \cdot \frac{K_{MAX} \cdot I_{OUT}}{5} \cdot \frac{2.5}{V_{OUT}} \cdot G_{mv}(s) \quad \text{(eq. 26)}$$

In real application, input voltage is sinusoidal waveform. By averaging (eq. 25) over one period of input voltage, a simplified loop−gain equation can be derived as (eq. 26), where I_{OUT} is rated output current, P_{OUT} is rated output power, P_{MAX} refers to maximum delivered power when $V_{VEA} = V_{VEA.MAX}$, and $K_{MAX} \equiv P_{MAX}/P_{OUT}$. Since V_{VEA} has 5 V of linear range, $V_{VEA.MAX} - 0.6 = 5$.

When programming output voltage (PVO) function is not activated, the control loop regulates V_{FBPFC} to 2.5 V. Thus, (eq. 26) becomes the design equation referred in application note AN4165/D. However, if the R_{CS} value is not determined exactly as indicated by (eq. 11), (eq. 18) combined with (eq. 23) and (eq. 24) can serve as design equation.

The voltage−regulation loop gain is drawn in Figure 21. The simple equation refers to (eq. 23), while the full equation refers to (eq. 22). A computer simulation result is put together for comparison. Although (eq. 22) gives a result that is closer to simulation result, (eq. 23) is reasonable to be used for design purpose.

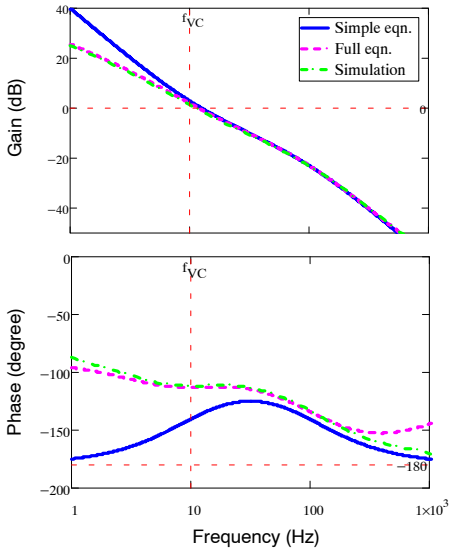

Figure 21. Comparison of Loop−Gain Equations

How Channel Management Works

In a multi−channel PFC converter, to disable some channels according to different load conditions can be beneficial for overall efficiency. FAN967x's CM pins are used to manipulate enabling or disabling of the respective channel. Note that CM1 disables all channels at once.

Two different ways can be used by interfacing with CM pin, as depicted in Figure 22. When using an external circuit to send a logic signal, a logic HIGH and LOW signal controls CM pin voltage to activate or deactivate each channel. In this way, any V_{CM} level in between is not used.

The other is to set a voltage on the CM pin by a resistor based on the maximum sourcing current of the CM pin. This voltage becomes a threshold voltage for V_{VEA} to decide whether a channel should be disabled or enabled. When $V_{VEA} > 55\ \mu A * R_{CM}$, the respective channel is in full operation. Otherwise, FAN967x gradually reduces the ratio of wattage that the channel delivers until it is fully disabled. Also, note that all channels shut down when $V_{VEA} < V_{EA-OFF}$ (0.3 V).

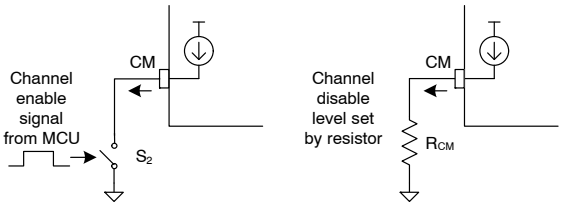

Figure 22. Interfacing CM Pin

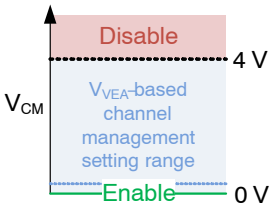

Figure 23. V_{CM} Operating Range

Figure 24 shows the concept of CM−pin behavior. A comparator compares V_{CM} and V_{VEA}, and its output adjusts CM−pin sourcing current and the gain between V_{RM} and G_{MI} error amplifier. The gain and the CM−pin sourcing current changes together, as described in Figure 25. When the CM−pin sourcing current drops to 17.5 μA, which is 31.8% of its maximum value 55 μA, the gain drops to 0% and the respective channel is disabled.

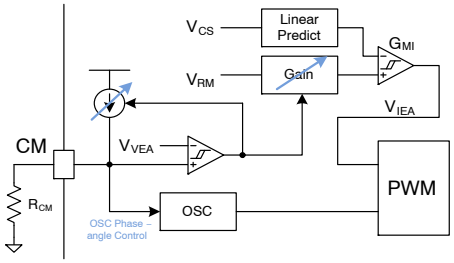

Figure 24. Conceptual Block Diagram of CM Pin

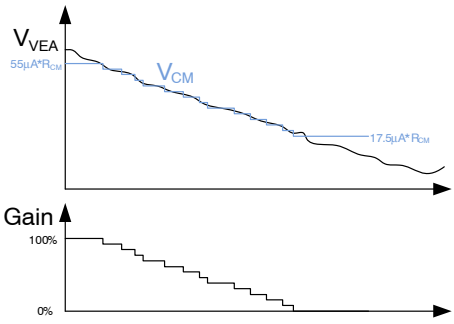

Figure 25. Interaction of V_{VEA} and V_{CM}

Offset in GMI error amplifier

Input offset is a particular non−ideal characteristic in most of the amplifiers. In FAN967x, the design target of the G_{MI} error amplifier is to have zero input−offset voltage. By trimming during IC production, the offset voltage of the G_{MI} error amplifier of the first channel is very close to zero. For the other channels, assuming V_{OS} ranges from −20 to 20 mV is reasonable due to production variation.

V_{OS} of the G_{MI} error amplifier distorts the shape of the inductor current, which means that total harmonic distortion (THD) can be affected, in light−load conditions. When V_{OS} is with a negative value, the average inductor current goes lower due to negatively shifted current command (see V_{CS-B} in Figure 27). Around the valley of the rectified input−voltage signal, the current command becomes zero. When V_{OS} is positive, the average inductor current goes higher (see V_{CS-C} in Figure 27). Around the valley of the rectified input−voltage signal, the input voltage is zero while the current command is above zero. Both conditions make the shape of the input current distorted.

Effect of V_{OS} on THD is minor in heavy−load conditions. In light−load conditions, its effect becomes much remarkable. Our experience is that when offset is negative, THD measurement result tends to be higher (worse), while higher−order harmonics have lower energy (better), and vice versa.

Another effect of the offset is current imbalance across channels in light−load condition. If we connect all CM pin to ground, all channel should be in full operation. They should deliver the same amount of power. However, in light load condition, such as $V_{VEA} \approx 1$ V and high input voltage, the amplitude of the current command is not too much larger than the possible offset voltage. The offset voltage becomes prominent to the current command, which makes delivered power of each channel be not identical. Some channels may even not operate since their valid current command is smaller than the negative offset voltage, which means the channel current will be regulated to zero.

To overcome the uncertainty by the offset voltage of the G_{MI} error amplifier, we recommend adding gradually operating channel number according to output power by using channel−management function. Reduced channel number in light load condition forces the required current command signal to be higher. So, it alleviates the effect of the offset voltage.

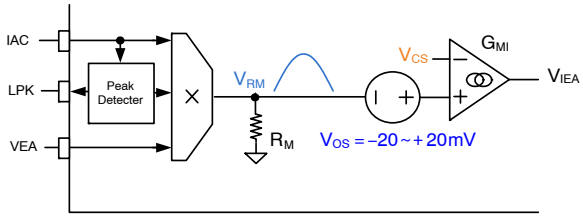

Figure 26. Input Offset of G_{MI} Error Amplifier

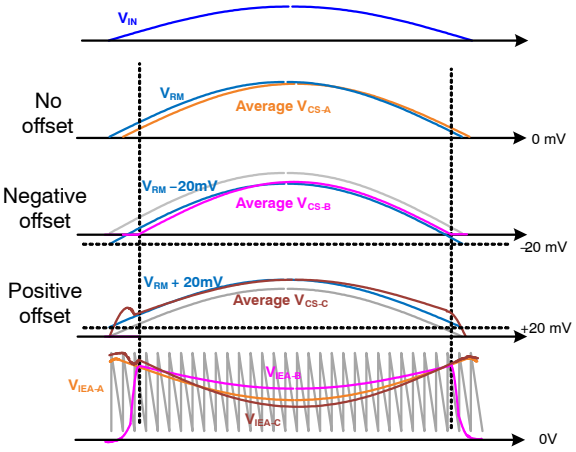

Figure 27. Effect of V_{RM} Offset to Average V_{CS}

Protections

FAN967x has lots of built−in protections, covering faults on input voltage, output voltage, over current, and improper IC operating conditions.

ILIMIT2, GC, and RLPK pins have pin−open protection. $V_{ILIMIT2-OPEN}$, $V_{GC-OPEN}$, and $V_{RLPK-OPEN}$ are related parameters for pin−open protection. ILIMIT1 pin does not have the same open−circuit protection as ILIMIT2. ILIMIT1 sets a threshold voltage of V_{RM}, which already has internal highest value of 0.8 V. Since there is a highest V_{RM}, an open−circuit protection for ILIMIT1 is not necessary.

When protection is triggered, FAN967x shuts down its OPFC and IEA signals. Soft start resets as well. FAN967x resumes operation when fault condition is cleared.

Table 2. Collection of Protections in FAN967x

Category	Protections	Triggering condition
Input voltage	Brown in/out	Start operating when input voltage is high enough.
	Sag	Input voltage drops for a while.
	AC−OFF	Input−voltage signal (IAC) is missing or too low.
Output voltage	FBPFC UVP	Output voltage is too low or FBPFC pin open.
	FBPFC OVP	Output voltage is too high.
Over current	ILIMIT1	Limit current command $V_{RM.}$
	ILIMIT2	Pulse−by−pulse current limiting for CS.
IC operating conndition	VEA−OFF	Low−power detection a.k.a. burst mode.
	VDD−UVLO	Supply voltage is not high enough.
	VDD−OVP	Supply voltage is too high.
	OTP	Chip junction temperature is too high.
	ILIMIT2 open	ILIMIT2 pin is opened.
	GC open	GC pin is opened.
	RLPK open	RLPK pin is opened.

References

[1] FAN9672, Two−Channel Interleaved CCM PFC Controller, Data Sheet https://www.onsemi.com/pub/Collateral/FAN9672−D.PDF

[2] FAN9673, Three−Channel Interleaved CCM PFC Controller, Data Sheet https://www.onsemi.com/pub/Collateral/FAN9673−D.PDF

[3] AN4165/D, Design Guideline for a 5−kW 3−Channel Interleaved CCM PFC Using FAN9673 https://www.onsemi.com/pub/Collateral/AN4165−D.PDF

[4] R. B. Ridley, B. H. Cho and F. C. Y. Lee, ”Analysis and interpretation of loop gains of multiloop−controlled switching regulators (power supply circuits),” in *IEEE Transactions on Power Electronics*, vol. 3, no. 4, pp. 489−498, Oct. 1988.

[5] B. Bryant and M. K. Kazimierczuk, ”Small−signal duty cycle to inductor current transfer function for boost PWM DC−DC converter in continuous conduction mode,” *2004 IEEE International Symposium on Circuits and Systems (IEEE Cat. No.04CH37512)*, 2004, pp. V−856−V−859 Vol.5.

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