Standard Logic ICs as Essential Building Blocks in AI Systems

Why Interoperability Logic Determines Whether High-Performance AI Accelerators Actually Work Together on a Board

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Introduction

AI training and inference equipment is built around core compute devices – GPUs, TPUs, and custom accelerator ASICs – that are selected almost entirely for raw performance, power efficiency, and latency rather than for how easily they interoperate with the rest of the system. These devices are fabricated on advanced process nodes optimized for compute density and power efficiency, which typically limits their native I/O to low core voltages that are incompatible with the higher-voltage control, memory, and sensor buses found elsewhere on the board.

Bridging that gap is the job of standard logic: gates, level translators, buffers, flip-flops, shift registers, I/O expanders, and signal switches. These are the devices that let systems engineers actually connect state-of-the-art accelerators, memory controllers, sensors, and management processors into one working board – without redesigning the accelerator itself.

The System Integration Challenge

Once a GPU, TPU, or accelerator ASIC is selected for compute performance, the system design team inherits a set of interoperability problems that standard logic is specifically built to solve:

- Signal interoperability across mismatched I/O voltage levels between accelerator cores, memory, and control-plane devices.
- Signal conditioning and buffering to preserve edge rates and drive strength across connectors, mezzanine cards, and long board traces.
- Control logic implementation for reset sequencing, interrupt handling, and board-level state machines.
- System signal optimization using shift registers, flip-flops, and small-scale logic (including ALU-class functions) to reduce pin count and synchronize clock domains.
- Signal flexibility through I/O expansion, giving designers additional GPIO and bus capacity without consuming scarce microcontroller pins.

Figure 1 illustrates how these functions appear on a representative AI accelerator baseboard, and Figure 2 shows the same pattern at AI Data Center rack level where standard logic is one of the core elements of system support circuitry.

onsemi Logic Portfolio Advantages

onsemi's standard logic portfolio spans AC, ACT, HC, HCT, LCX, LVX, VHC, and VHCT families, with operation up to 140 Mbps and supply voltage ranges from 0.9 V to 18 V across the line, giving designers the range needed to match accelerator, memory, and sensor domains from a single supplier rather than stitching together parts from several vendors.

The newer Treo platform, built on a proprietary 65 nm process, extends this further: Treo-based level translators such as the T30LMXT3V4T245 support data rates up to 400 Mbps, reducing design complexity and power consumption on high-speed protocols like SPI.

For AI system designers, the practical value of a broad, single-vendor logic portfolio shows up in four places:

- Enabling system performance targets by matching translator speed and drive strength to the accelerator's native signaling rather than forcing a compromise in terms of performance.
- Meeting power, size, and thermal objectives with small-footprint, low-Icc logic instead of over-specified general-purpose parts.
- Simplifying the coordination of signals from disparate components – GPUs, TPUs, processors, sensors, and memory controllers – by sourcing the level translation, buffering, and expansion functions from one logic family set.
- Reducing sourcing risk: **onsemi** is a top global suppliers of logic devices, and both **onsemi** and its distribution partners publish cross-reference tools mapping equivalent logic families across suppliers, which lets designers qualify a multi-source strategy without redesigning the board.

Table 1 maps common logic functions to representative **onsemi** devices and to the AI equipment application cases where each is typically used.

For more information about **onsemi**'s logic portfolio, please visit the **onsemi** logic landing page.

Reference Architectures

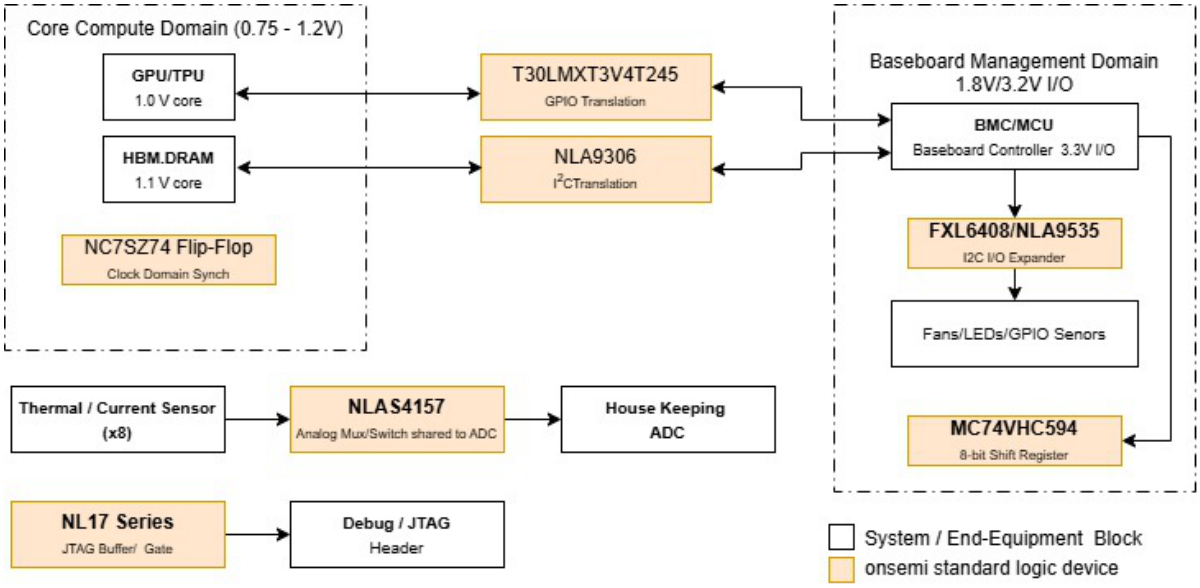

Figure 1. AI Accelerator Baseboard Signal Interoperability Architecture

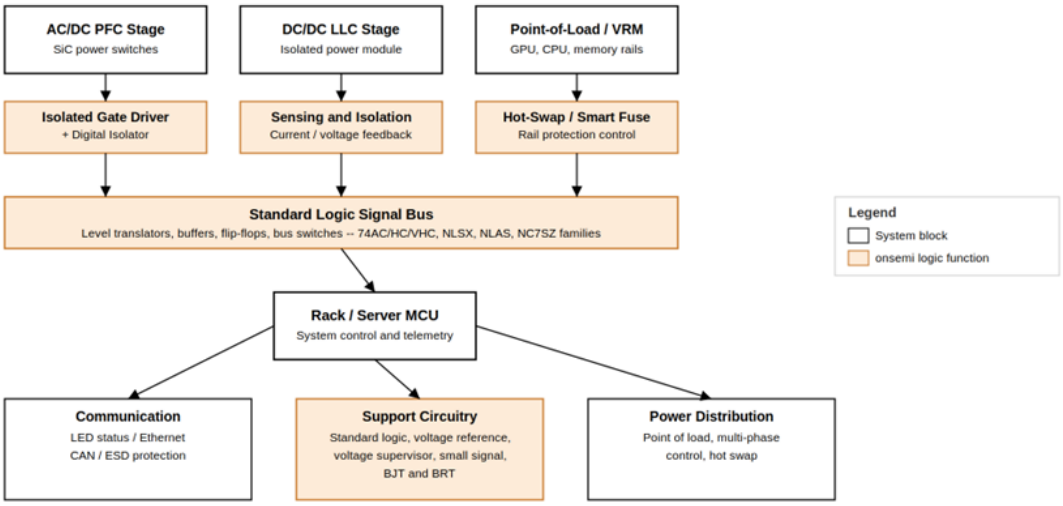

Figure 2. Standard Logic Within the AI Server Power and Control Signal Chain Flow

Table 1. STANDARD LOGIC FUNCTIONS AND AI EQUIPMENT APPLICATION CASES

Logic Function	Representative onsemi Devices	AI Equipment Application Case
Gate Logic (buffers, inverters, AND/OR/ NAND/NOR/XOR)	74AC/ACT/HC/HCT/LCX/VHC/ VHCT families; MC74HC1G04	General-purpose control-signal buffering and combination between MCU, sensors, and accelerator support circuitry; clean translation of enable, reset, and interrupt lines.
Level Translation	NLSV1T244; FXLH1T45; NLA9306; T30LMXT3V4T245 / T30LMXT3V4T244 (Treo platform)	Bridging 0.8−1.2 V GPU/TPU/ASIC core I/O to the 1.8−3.3 V domains of BMC/MCU, flash, and sensor buses, preserving signal integrity at data rates up to 400 Mbps.
I/O Expanders	NLA9555 (16−bit I2C); NLA9535 (16−bit, low power, I2C); FXL6408 (8−bit I2C GPIO)	Adding GPIO capacity for fan control, status LEDs, presence-detect, and board-ID straps without consuming scarce MCU pins on densely populated accelerator baseboards.

Table 1. STANDARD LOGIC FUNCTIONS AND AI EQUIPMENT APPLICATION CASES (continued)

Logic Function	Representative onsemi Devices	AI Equipment Application Case
Signal / Bus Switches	T30LMSW3B3125, T30LMSW3B3126	Routing thermal, current, and voltage-sense analog signals to a shared housekeeping ADC channel; isolating or re-tasking shared buses during board tests and debug.
Flip-Flops and Latches	NC7SZ74; MC74AC273; 74VHC74	Clock-domain synchronization between memory/accelerator clocks and management-plane logic; status latching for fault capture and power-sequencing state machines.
Signal Muxes (SPI/ GPIO)	T30LMSW3B3257, T30LMSW3B3253	Multiplexing and voltage-bridging multiple SPI sensor and EEPROM segments (temperature, power, memory SPD) onto a single BMC controller bus.
Shift Registers	MC74VHC594	Serial-to-parallel expansion for status-LED banks, fan-fault indicators, and slot-ID encoding, reducing MCU pin count and PCB routing congestion.
Buffers and Bus Transceivers	74LVX4245	Bidirectional, dual-supply data-bus buffering between accelerator management buses and baseboard controllers across mixed 1.65−5.5 V mezzanine connectors.

REVISION HISTORY

Revision	Description of Changes	Date
0	Initial document release.	9/15/2026

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
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