Smart Low Power Idle Mode in Zonal eFuses

AND90413/D

Introduction and Scope

One of the advantages of a Software Defined Vehicle is the ability to add/program new features to different performance and functional aspects over time via software updates. It is anticipated that these Over-the-Air (OTA) updates cannot always occur during normal vehicle operation, and therefore, it is desired that software updates be carried out during a vehicle's key-off, or in some cases, a parked state. In addition, there are certain loads such as keyless entry modules, security and alarm control sensors etc. that are required to be powered on during key-off state. This means subsets of zonal clusters will need to remain powered while consuming as low a system leakage as possible so as not to cause excessive battery drain. This can be a challenging task from the perspective of eFuse IC providing power to these clusters. Since any current consumed for the operation of the IC will be considered "leakage" from a system perspective, it is imperative to reduce the overall operational leakage and to devise a dedicated mode that offers reduced leakage for powering on key-off and park-mode loads.

Naturally, while inactive (i.e. eFuse is "open", not conducting aka in "sleep mode"), low quiescent currents are desired for all eFuses present on board inside a vehicle. But when an eFuse is activated, it typically consumes a nominal operating current to support diagnostic and control functions. Therefore, for zonal applications, it is desired to be able to add a special state for such "light loads" where control functionality is still available while having other protections and diagnostics consume no charge. To this end, **onsemi**'s eFuse devices include a dedicated low power Idle mode specifically for zonal applications, which allows the output stage to be switched ON while significantly minimizing the ground operating current.

This application note provides details on operational aspects of this low power Idle mode. The sections below will present the key requirements, figures of merit, entry/exit criteria and will compare different design implementations towards that end. Different design aspects centric to **onsemi** eFuses will also be discussed together with corroborating bench measurement results. Discussion on other smart switch/eFuse features besides Idle mode is outside the scope of this document and respective application notes should be referred for any details on those features.

Idle Mode Control

The requirement to enable Idle Mode is primarily governed by the Zonal MCU. Depending on the requirements in a specific "drive cycle", the MCU may chose to enable/disable the mode altogether. **onsemi**'s direct drive eFuses employ a dual-purpose Idle Flag pin (Refer section *Idle Flag* in this document) to control this mode and consequently device's response to load transitions during a drive cycle. For devices with communication protocols such as SPI, Idle mode can be controlled and configured via software register settings.

Entry into Idle Mode

Once enabled, eFuses are generally ON for extended durations and Zonal MCU, in such applications, can go to sleep/reduced operating mode (if not polling actively through watchdog). The load transitions in such case should dictate entry into Idle mode. The loads in this case are mostly ECU/ sub-system modules and are capable of triggering load transitions based on end-node desired response without the interference of Zonal MCU. Because the application microcontroller may be limited in its control and configuration capability in this state, it is anticipated for the eFuse to continuously monitor load current and be able to enter the low power mode autonomously based on internally set load thresholds. Further, since the purpose of this mode is only to support software updates, or a minimum functionality, the load levels are usually significantly lower than those in normal operation. Idle load thresholds are in the range of 1%~5% of nominal load dependent on application (Refer specific product datasheets for Idle mode load thresholds) and they are active without any intervention from microcontroller. The thresholds are carefully designed to avoid, on one hand, inadvertent operation in Idle mode in case of certain load step-down transients that are expected in the application, while on the other hand, should also ensure operation in Idle mode when load spikes occur because of periodic microcontroller polling. Caution must be exercised in managing such load transients, especially, when driving at lower than rated steady state loads. It may also be desired to have a configurable Idle load threshold to serve varying load requirements across applications. **onsemi** zonal eFuses with SPI offer an adjustability in Idle thresholds thereby offering an enhanced configurability in the steady state operating load of the device without worrying about the load transients.

In other cases, entry into Idle mode can also be "dictated" by Zonal MCU when it is driving software updates and it can command the eFuse to go into Idle mode. Even in this case, eFuse should only go into Idle mode once load current is below Idle threshold to preclude a situation where the load is being actively driven without full protections and diagnostics available, potentially causing a safety hazard. The load current supported during software updates must be sufficiently lower than the Idle entry load threshold of the

selected eFuse in the application. Besides the load current, other conditions such as the output stage actively toggling during inrush, or supply voltage below the desired range should also be considered before making a decision to enter Idle mode and disable internal protection circuits.

The time to enter Idle mode after observing the required load transition or receiving an MCU command usually depends on device's ability to disengage its internal biases & controls safely and while following a well-defined internal state machine/ hand-shaking sequence before finally entering this mode. This is critical because there could be events such as overload transitions, supply dips or short circuits etc. during this handshake and the device must not enter Idle mode in such a scenario. The waveform in Figure 1 below depicts this scenario in NCV84003G. At the first (downward) load step, the routine and handshake to enter Idle mode starts. However, the second (upward) load step causes the routine to be abandoned and consequently the Idle flag stays low. While there are no stringent requirements on Idle mode "entry time", **onsemi** eFuses usually enter this mode in a few hundreds of microseconds (Refer specific product datasheets).

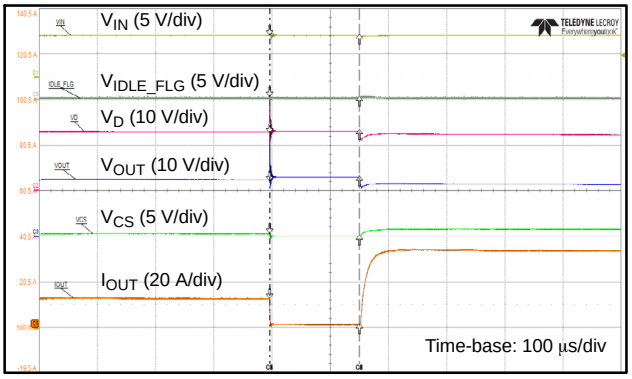


Figure 1. Response to Overload Events during Idle Entry Routine in NCV84003G

Operation in Idle Mode

When operating in Idle mode, the most critical performance parameter is the operating current in this mode. This is the current consumed by the IC to support Idle device operation, i.e., any current that flows through the GND or other I/O terminals, not including the load current, is considered as "operational leakage" from a system standpoint and is termed as Idle operating current. Since there could be multiple eFuses in a zonal cluster, this operational leakage needs to be low to minimize the overall "system spend" and reduce the battery drain during this mode.

The conceptual schematic below depicts the operational principle for this mode.

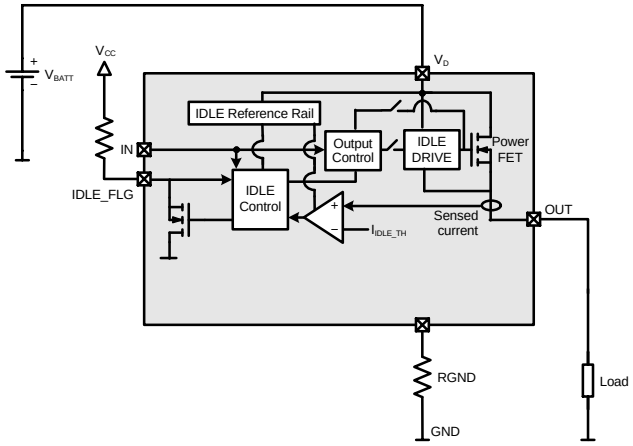


Figure 2. Idle Operation Conceptual Schematic

While in this mode, the internal bias rails are designed to minimize operational leakage and output control is provided through a dedicated Idle drive. Since the load current levels are low in this mode, the conduction loss, or R_{ON} requirements can be relaxed in lieu of reduced leakage. The possible implementations of Idle drive, therefore, may include but are not limited to, a parallel bypass switch, or a smaller DMOS (output Power FET), or a feebly driven DMOS to power loads. Either of these approaches are aimed at reducing or eliminating the charge pump/over-drive consumption current associated with the DMOS and have their associated concerns and trade-offs.

While a parallel bypass switch (likely a PFET in parallel to the power stage) can offer reduced leakage levels by eliminating the need of charge pump drive in Idle mode, it may add significantly to die area as most PFETs available on BCD technologies are not area efficient. Further, the conduction losses may be worse because of the inefficient bypass transistors. The overall package size, system cost impact and the required output voltage levels in this mode must be considered before selecting a solution for zonal system design. Further, when integrating advanced features such as SPI control, failsafe diagnosis etc., it is imperative to minimize the leakage associated with these internal blocks.

In addition, the various Idle drive architectures differ not only in the levels of conduction losses, or operating consumption but also in the supported mode transition and their ability to swiftly exit to normal mode in case of overcurrent transients. For instance, Idle drives with parallel pass-transistors may be challenged in supporting nominal application loads greater than Idle exit threshold (since most such pass devices saturate early and need to be oversized for handling higher loads) and in handshaking with the power DMOS in case of overload transients. A feebly driven

DMOS with a higher transconductance (than the PFET) can deliver the required load but needs to be protected and safely shut down in time before the load-current overshoots beyond the internal protection limits and potentially overstress the die. Likelihood of short circuit and nominal load transients should also be considered before selecting a particular solution.

As described before, the majority of the “Smart” protection and diagnostic features are disengaged in this mode with the exception of a few. Some of these are discussed below.

IDLE Flag

Since the integrated diagnosis is not available in this mode, it is intuitive to provide a dedicated signal that acknowledges transitions in and out of Idle mode. Most solutions in this regard consist of an open-drain Idle flag pin (Refer Figure 2) that informs the microcontroller of operation in Idle mode. SDV applications that are designed for key-off software updates should have the Idle pin connected to the zonal MCU to monitor and verify that the IC is operating in IDLE mode. The pin, when supplied with an external logic supply, is actively pulled down/switched off and pulled up depending on the mode of operation (the signal should be monitored, in general, after any startup blanking time as provided in the datasheet). The flag output is particularly important in providing the microcontroller with information on high current transients while operating in Idle mode. Further, devices, such as NCV84003G, offer a feature to enable/disable Idle mode based on the state of IDLE flag pin at startup, thereby utilizing this pin as a dual purpose I/O. When using the part for applications that do not require low power mode, users may wish to disable Idle mode while still using other fuse-centric capabilities of the IC such as I2t protection. To disable Idle mode, the flag pin can be tied via a resistor to ground on the PCB. When the device exits from sleep mode at startup, the flag pin is queried internally to confirm the state of the pin. If the pin is grounded, Idle mode is disabled for the cycle (until the chip goes to sleep again). If the pin is supplied via a pull-up resistor, Idle mode is enabled for the cycle, and device is able to transition to Idle mode provided other conditions such as load and supply thresholds are met. Waveform below as measured on NCV84003G represents the Idle blanking delay timing. As the device turns on from sleep mode (V_{IN} = V_{CS_EN}), the state of Idle flag, which in this case is pulled up to 5 V using a 10 kΩ resistor, is scanned during blank period. Idle mode is therefore enabled and device transitions into Idle mode (as depicted by Idle flag subsequently transitioning Lo → Hi) once other conditions for Idle entry are met (Refer to product datasheets for the specific condition set for Idle mode entry and exit).

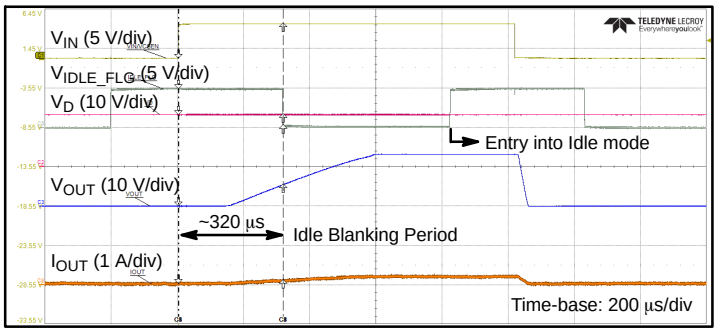


Figure 3. Dual Purpose Idle Flag I/O− Blanking

For SPI enabled devices, the availability of this dedicated pin becomes all the more important as communication interface is likely disabled in this mode. Further, while designing multi-channel devices with Idle mode, it should be noted that maximum benefit in the form of reduced leakage is derived if all channels are driven in Idle synchronously with a common flag indication pin. For specifications on flag pin and its functionality, refer to the respective product datasheets.

Digital Input Latch

Since the output stage is required to be enabled prior to entry into Idle mode, an operation in Idle mode would imply that the logic input pin is required to be driven high all the time by zonal MCU. Such a requirement will not only increase the system level current consumption but would also entail the MCU to stay “awake” in this key-off mode. To preclude this scenario, **onsemi** eFuses such as NCV84003G offer a smart latch at the logic IN pin that remembers the last state of the IN pin under certain conditions and lets the zonal MCU to float/tri-state its logic output used to drive eFuse’s IN pin, thereby allowing the MCU to transition to sleep mode. Refer to respective product datasheet for further details on the latch operation, and the required condition set.

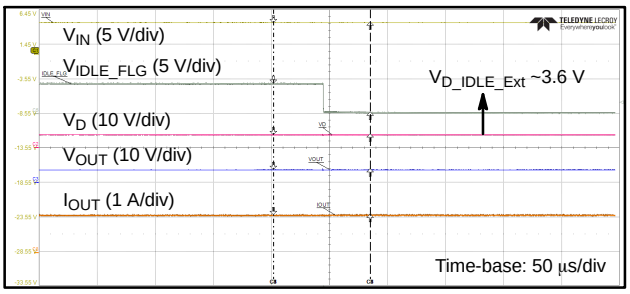
Current Monitoring

An internal current monitoring mechanism is required to be active in Idle mode to facilitate autonomous transitions to normal mode in case of load activation or overload transients such as due to short circuit. A key challenge in designing this current monitoring is the trade-off between the desired accuracy around thresholds and the operational leakage in Idle mode. Since the current consumption needs

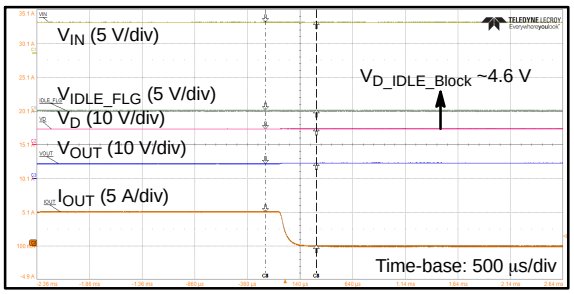
to be minimized in this mode, the comparators designed are often not as precise as those in normal mode and often suffer from headroom/hysteresis issues. While this may not be critical in case of overload transients, where the applied load step eventually settles to a much higher current level, it may be crucial for load steps that settle close to Idle exit thresholds and the decision to exit the mode becomes critical. Such load steps may be inflicted due to inadvertent/partial load turn-on's (application fault) or due to nominal load being too close to Idle exit threshold. For this purpose, it is re-iterated to select the eFuses carefully while ensuring that nominal application load current levels are well-above the Idle exit threshold including the specified tolerances. Further, any load spikes caused by polling during software updates should be contained below the exit threshold to avoid an un-necessary exit to normal mode and wake-up of the MCU through Idle Flag. Finally, the stability of the device close to the exit threshold, i.e., the decision to exit or stay in Idle mode is yet another performance metric to be considered. The device should not keep oscillating between Idle and normal modes due to hysteresis challenges close to the threshold. **onsemi** eFuses incorporate an internal OTP routine to ensure tight accuracies around the Idle load thresholds. The comparators are designed to avoid any oscillatory behavior as cited above.

Supply Voltage Monitoring

Besides current monitoring, another key aspect of operation in Idle mode is the supply voltage monitoring. The mode, in general, is designed for operation in nominally specified supply voltage range to support software updates and key off operation. While on the higher side of supply voltage, the natural over-voltage protection through integrated clamps is still available, the operation at extremely low battery voltages becomes critical to manage to avoid any inadvertent device response. Once again, the headroom of the internal blocks observes a trade-off against the operational leakage as low headroom circuitry often consumes a higher operation current. Further, the bias rail and the bandgaps deployed in this mode can also potentially de-stabilize at low battery voltages. To circumvent a faulty response from the device at low supply voltage levels, **onsemi** eFuses incorporate a voltage detection mechanism that triggers an exit from Idle mode to normal mode if the supply voltage drops below a defined threshold. At the same time, if operating in normal mode, an entry into Idle mode is also blocked if the supply voltage drops below the defined blocking threshold. Using NCV84003G as an example, Figure 4a) describes Idle mode exit behavior where the device exits Idle mode at low supply voltage while Figure 4b) describes Idle mode blocking response where the device prohibits entry into Idle mode even though load current is reduced. Refer to respective product datasheets on these exit and blocking supply voltage thresholds. Such a design ensures that device exhibits well-defined behavior in terms of output levels, internal detections and response to overload in case of Idle mode operation.



a)



b)

Figure 4. a) Idle Mode Exit at Low Supply Voltage
b) Idle Mode Blocking at Low Supply Voltage

Exit from Idle Mode

If a software update in key-off mode is complete, the zonal MCU should be able to invoke an exit from Idle mode using logic IN pin, or SPI commands. The device will exit to sleep/normal mode accordingly. In another case, exit from Idle mode can be because of load transitions. As explained before, certain load transitions are because of load activation. To exemplify, this could happen in scenarios where the user adjusts the seat position, presses the brakes etc. during such updates. A worst case example could be a possible crash (triggered by another vehicle) and the need to active airbag ECU/squib loads, or other secondary restraint mechanisms. In all such examples, the load transitions to nominal levels, and a drop/loss of output voltage may imply a compromise or loss in the required functionality respectively. As stated before, different design implementations for Idle drive have their merits and short-comings. In the aforementioned scenario, a parallel PFET may be required to be shut down before the power DMOS can be activated to avoid extended operation in saturation and associated die overstress. Similarly, a smaller (or sectioned) DMOS may also be required to be briefly shut down to avoid potential damage at heavy loads. The selection of zonal eFuse must consider the required time to exit to normal mode with power DMOS fully ON as well as any allowance for drop/loss of output voltage depending on

application criticality. The waveform below, as collected on NCV84003G, depicts that the device is able to safely exit to normal mode when presented with a load step in a period close to 15 µs. The output voltage, as can be observed, does not show a significant drop. Refer to product datasheets for detailed timing specifications.

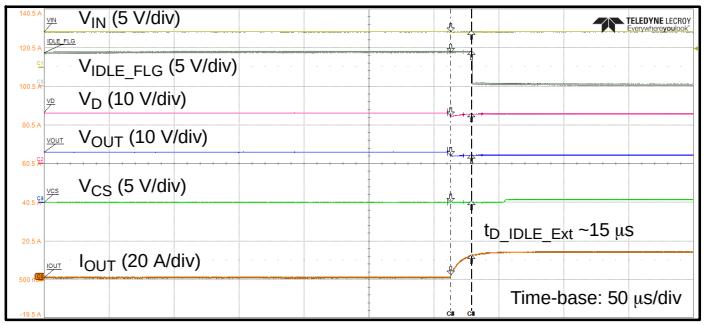
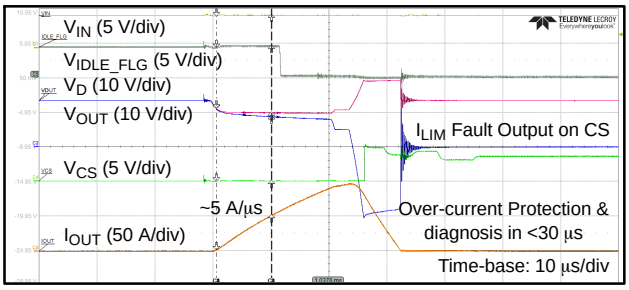
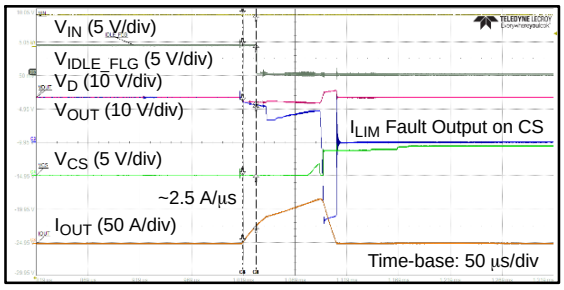


Figure 5. Idle Mode to Normal Mode Response and Transition Time

An exit from Idle mode can also be triggered in case of overload transients such as due to short circuit. This is under the assumption that a physical short circuit at load, cable, or module level may still happen while the device is operating in Idle mode. It is very important that the device safely exits Idle mode, thereby activating all the protection and diagnostics and be able to shut down the power stage if an over-current / over-load fault is triggered. In this regard, the transition time to exit Idle mode and engage protection circuits is extremely critical. Further, any short circuit applied must be within the limits specified, if any, in the datasheet. For short circuit load steps with ramp rates faster than the datasheet recommendations, the peak transient current levels can exceed the device capability and potentially overstress the die because of high power dissipation levels. The waveforms below represent scenarios where short circuit is applied to NCV84006G in Idle mode at different load current ramp rates with output impedance according to terminal and load short circuit (per AECQ100-012) respectively. Both events cause the device to exit to normal mode, engage over-current protection as well as provide diagnostic reporting on CS output. The corresponding peak current overshoots are also reported on these waveforms.



a)



b)

Figure 6. Idle Mode to Short Circuit Protection Response in NCV84006G in Case of a) Terminal Short Circuit, and b) Load Short Circuit per AECQ100-012 for V_D = 13.5 V

Summary

To summarize, this application note elaborates critical performance aspects associated with the lower power Idle mode in zonal eFuses. Different implementation options, their design challenges and selection criteria in the application have also been discussed to assist the system designer in selecting and integrating the right eFuse meeting the specific application needs. Some key features as relevant to Idle mode functionality in **onsemi** eFuses are also presented in this application note.

REVISION HISTORY

Revision	Description of Changes	Date
0	Initial document release.	3/26/2026

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

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