Enabling AI Accelerators with onsemi Voltage Level Translation

AND90408/D

Introduction

Artificial-intelligence (AI) capabilities are increasingly embedded across end-equipment—both at the edge and in the cloud—to deliver new functionality and user experiences. Realizing these capabilities on device or via cloud infrastructure requires adoption of the latest processor technologies, including high-performance CPUs, FPGAs, and—critically—GPUs that provide massive parallelism and high memory bandwidth for training and inference workloads. Operating these devices at aggressive, low core voltages is often essential to meeting thermal and power budgets while achieving target performance. However, low core voltages limit the I/O levels that can be supported, creating control and low-speed interface mismatches when connecting processors to peripheral subsystems. Voltage level translation devices are a key enabler for AI accelerator cards: they allow heterogeneous components to interoperate at the I/O level while each device continues to operate at its optimal core voltage, preserving performance, efficiency, and form-factor. This is particularly important for GPUs, which must run at very low core voltages, yet still communicate over a variety of control and serial interfaces to memory, sensors, and management controllers. Simple, scalable level translators resolve these I/O disparities without forcing compromises in system power, timing margins, or layout complexity (see Figure 1).

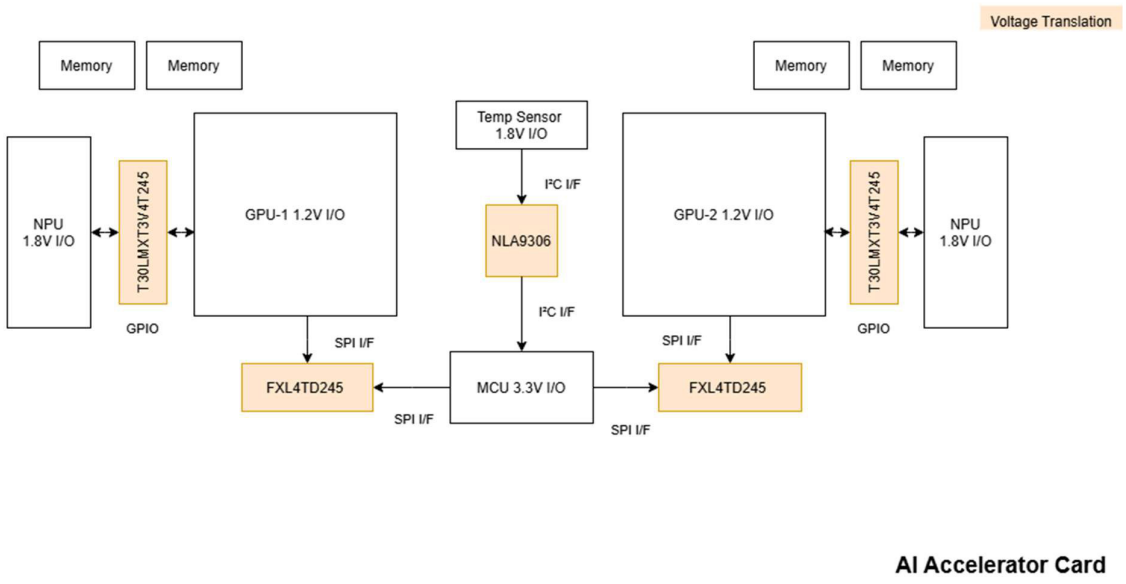

Figure 1. Translation Usage in AI Acceleration Cards

Voltage Level Translation

Integrated level-shifting solutions are available in a broad range of I/O families, bit widths, data-rate classes, drive strengths, and packages. **onsemi**'s level-translation portfolio spans auto-directional, direction-controlled, and fixed-direction devices to address nearly any control-interface requirement encountered in high-performance compute and AI accelerator designs. Options are offered across industrial and automotive with coverage for common interfaces—GPIO, SPI, I^2C, SMBus, MDIO, UART, JTAG, I^2S, PCM, and SDIO and more—over wide voltage ranges (from <1 V up to 5.5 V), enabling clean, reliable crossings between low-voltage GPU/CPU domains and higher-voltage peripherals (see Table 1). These translators help maintain signal integrity, interface timing, and system robustness while simplifying board-level design and scalability across product variants. **onsemi**'s latest Treo process-based level translators, such as the T30LMXT3V4T245, goes far beyond traditional level translators in terms of power efficiency. Treo based translators offer power dissipation levels that are almost 90% lower than competing solutions while offering industry leading data rates and current drive. For additional details on the breadth of **onsemi** solutions, please visit onsemi's level–translation landing page at onsemi.com.

Table 1. RECOMMENDED TRANSLATOR BY INTERFACE

Interface	Up to 3.6 V	Up to 5.5 V
FET Replacement	FXLP34 / NL3V1T244	MC74VHC1G126
1 Bit GPIO / Clock Signal	FXLA101 / NL3V1T244	MC74VHC1G126
2 Bit GPIO	FXL2T245 / NL5X4002	NL5X4002
2-Pin JTAG / UART	FXL2T245	NL5X4002
I^2C / MDIO / SMBus	NLA9306 / FXMA2102 / NL5X4002	NLA9306 / FXMA2102 / NL5X4002
4 Bit GPIO	T30LMXT3V4T245 / FXMAR2104	FXMAR2104
UART	T30LMXT3V4T245 / FXMAR2104	FXMAR2104
SPI	FXL4TD245 / FXLA0104	FXMAR2104
JTAG	FXLA0104 / FXMAR2104	FXMAR2104
I^2S / PCM	FXMAR2104	FXMAR2104
Quad-SPI	FXL2SD106	NA
SIM	FXLP4555	NA
8 Bit GPIO	FXL4245 / FXLH42245	74LVX4245 / 74LVX3245

REVISION HISTORY

Revision	Description of Changes	Date
0	Initial document release.	2/9/2026

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
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