EliteSiC JFET Based High Voltage Hot-Swap Application

AND90399/D

Introduction

Hot-Swap control/controller is used for safely inserting power supplies to a live system, without causing high inrush current which may corrupt or damage the bus system. Hot-Swap controller also provides protection against short circuit and overvoltage/undervoltage situations. Essentially, it enables “Hot-Swapping” where the power supplies can be swapped while the system bus is powered on.

Existing Hot-Swap controllers are designed for low voltage applications with voltage up to 100 V. Suitable solution is required when the high voltage (400 V to 800 V) system is necessary to meet the higher power demands by applications such as data center for AI computing. Figure 1 shows one example of the system topology.

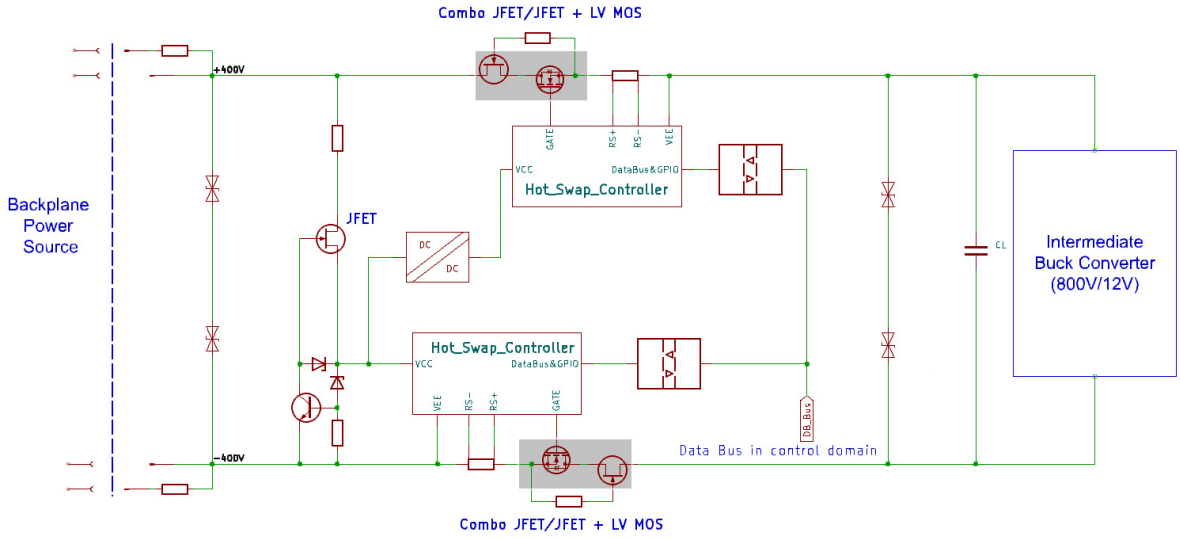

Figure 1. Simplified Block Diagram

This AN will focus on **onsemi** EliteSiC Combo JFET for Hot-Swap applications, including advantages, working mode description, design practices and test results, etc.

EliteSiC JFET Based Device

JFET is the simplest Field Effect Transistor (FET) device with direct drain to source current path. This simple structure gives the lowest possible on-resistance, and there is no gate charge traps or surface current which affects reliability. Figure 2 shows the structure of JFET. JFET is a normally-on device which means without negative gate bias applied, the device is on. To switch or keep it off, the negative voltage (lower than its threshold voltage) is needed.

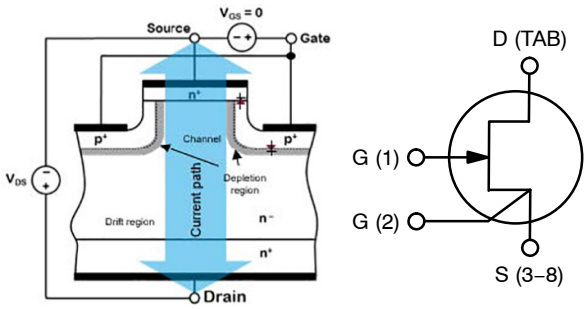

Figure 2. JFET Structure (Left: Structure, Right: Symbol)

onsemi provides two types of normally off devices based on SiC JFET:

- CJFET (Cascode JFET), Silicon Carbide (SiC) JFETs
- Combo JFET, Silicon Carbide (SiC) Combo JFETs

CJFET utilizes a cascode configuration with a low-voltage MOSFET and a JFET. The MOSFET acts as a switch for the JFET's source, while the JFET's gate is connected to the MOSFET's source. The circuit diagram and symbol for this configuration can be found in Figure 3.

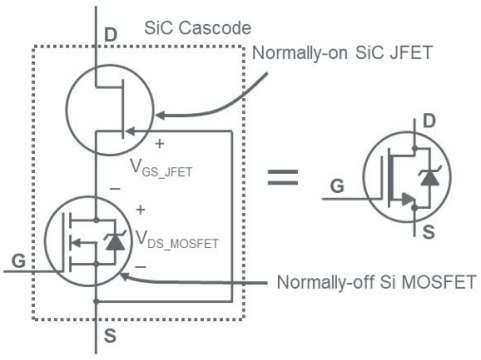

Figure 3. CJFET Structure

When the gate-to-source voltage (VGS) of a low-voltage MOSFET is above its threshold voltage, the MOSFET turns on. While JFET source is connected to the MOSFET Drain and its gate connected to the MOSFET source, it is turned on due to VGS_JFET exceeding its threshold. Conversely, when the MOSFET VGS is low (and it's off), the external voltage applied to the CJFET will increase the MOSFET's VDS until it exceeds the JFET's threshold voltage, turning the JFET off and enabling the CJFET to block high voltage. CJFET is mainly for high frequency switching mode applications.

A Combo JFET is similar to the cascode configuration of CJFET, but with the crucial distinction that the JFET's gate is externally accessible. This external access to the JFET's gate provides several advantages, including:

- Reduced on-resistance with overdrive
- Increase stability for linear mode control
- Adjustable switching speed for reducing overshoot and easily paralleling
- The ability to monitor junction temperature

For circuit protection applications like hot swap, linear mode stability and adjustable switching speed are critical. This is why Combo JFETs are recommended for hot swap applications. Figure 4 shows the symbol of Combo JFET.

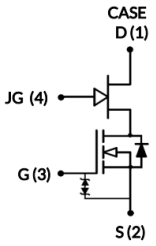

Figure 4. Combo JFET Symbol

Details refer to UM70113 – JFET and Combo JFET User Guide

Advantages of Combo JFET for Hot-Swap Applications

Low Rds(on):

The low on-resistance minimizes voltage drop and power dissipation during normal operation, when power FET is fully on. JFET based devices have lower Rsp than MOSFET devices, below figure shows the reason and tested RdsA between different technologies.

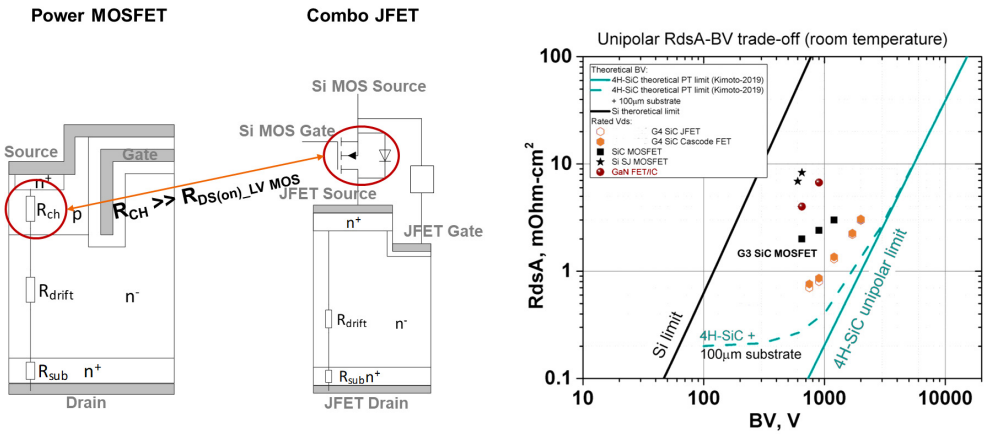

Figure 5. Structure and RdsA Comparison Between JFET and MOSFET

Strong Safe Operation Area (SOA)

During hot swapping, the voltage across the power FET is fully DC link bus voltage initially and decreases to zero voltage when DC link capacitors are fully charged. To maintain the junction temperature of power FET within specification, the charging current is typically very low compared to its normal operation current. This operation can cause thermal instability issues for modern power FET.

The thermal stability is defined by how big the positive temperature coefficient area is on transfer curves. Below figure shows an example of transfer curves of 1200 V/7 mΩ JFET and MOSFET. It is clearly shown that the SiC JFET has relatively smaller PTC area than SiC MOSFET.

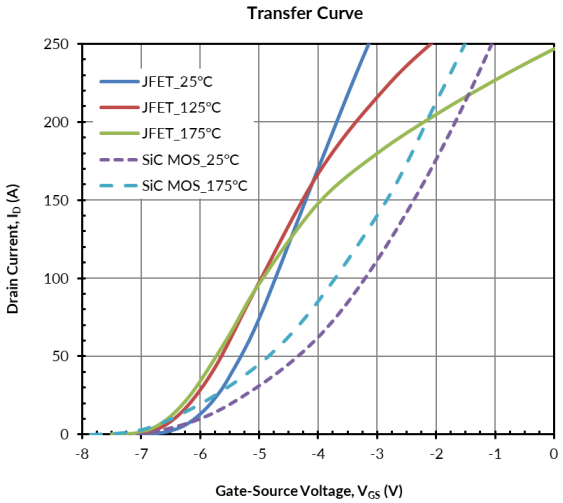

Figure 6. Transfer Curve of SiC JFET and SiC MOSFET

Current Limiting

The hot swap power FETs need to limit the current for safety of system and itself. There are two current limiting scenarios for hot swap applications: startup (DC link capacitors pre-charging) and over current protection (OCP). Figure 7 shows the working conditions for startup and OCP current limiting.

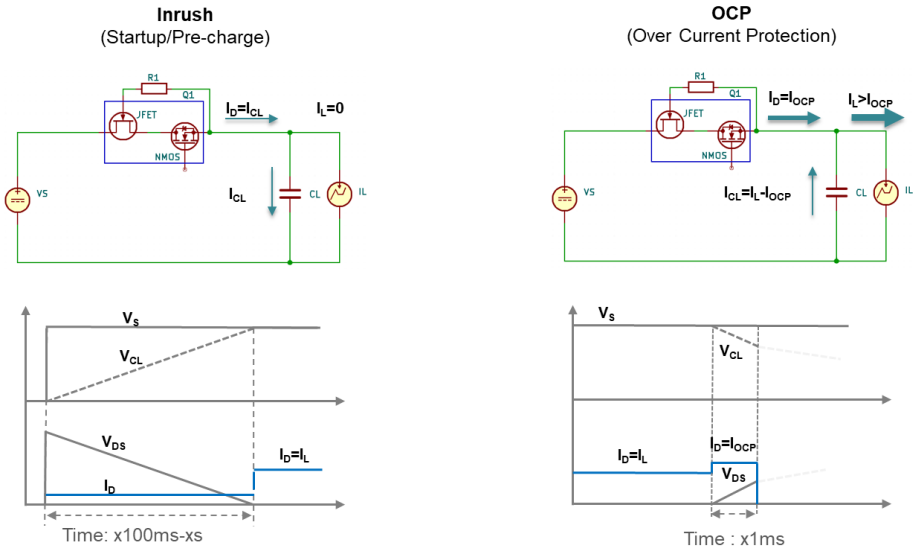

Figure 7. Startup Inrush Current and Over Current Protection

Combo JFETs can work in current limiting (Linear mode) stability, they have been tested with hot swap controllers for both 400 V and 800 V systems. Figure 8 illustrates the working principles of Combo JFETs for linear mode operations during startup and OCP.

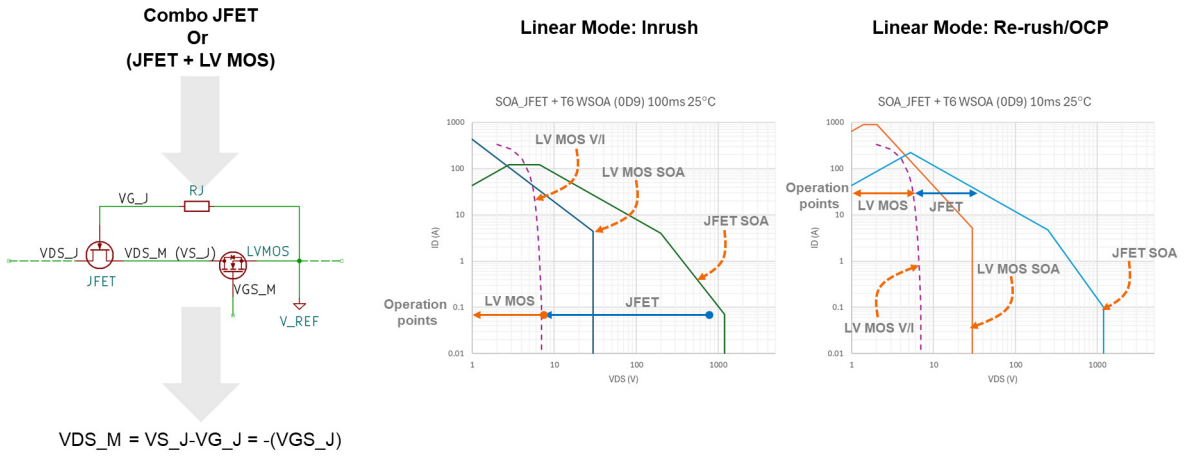

Figure 8. Combo JFET Working Principles During Startup and OCP

Gate Drive Voltage Compatibility

Most of the hot swap controller gate bias voltage is between 10 V to 12 V, the gate drive voltage of the power semiconductor needs to be compatible with hot swap controllers. Thanks to the low voltage silicone MOSFET gate input, the Combo JFET has universal gate compatibility with all hot swap controllers. Figure 9 shows that 10 V–15 V gate voltage can turn the Combo JFET fully on.

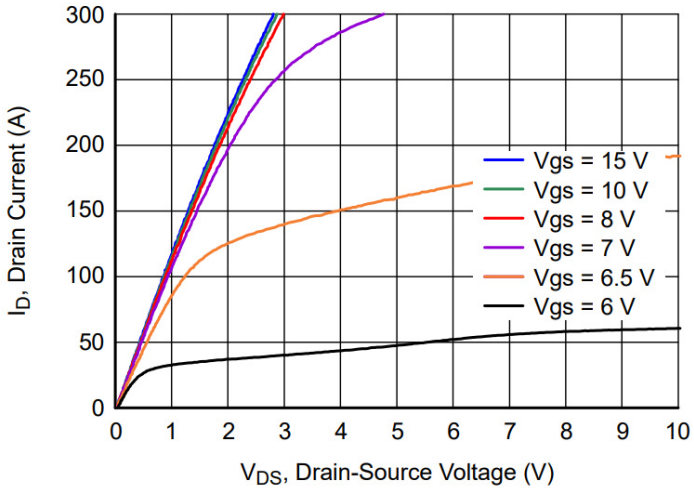

Figure 9. Combo JFET Typical Output V/I Curves with Different Gate Voltage (Example of 1200 V/9 mΩ Device)

Hot Swap Control Method

Hot Swap controller senses the current output and input/output voltage for controlling, please refer to the controller for detail. In this AN, we will discuss the inrush control methods, because the inrush or startup stage is more stressful for the power device.

There are two typical ways to limit the inrush current, one is dv/dt control/mode, and the other one is active current limiting.

dv/dt Control with External Cgd

A constant output voltage ramp rate (dv/dt) can control the inrush current value, and the limited current level is defined by:

$$I_{Inrush} = C_{load} \times \frac{dv}{dt} \qquad \text{(eq. 1)}$$

Power FET's dv/dt is controlled by constant gate drive current when the gate to source voltage is at threshold level.

This constant gate drive current control power FET dv/dt through Cgd, follows:

$$I_{GATE} = C_{gd} \times \frac{dv}{dt} \quad \text{(eq. 2)}$$

Based on (eq. 1) and (eq. 2) the inrush current is defined eq. 3.

$$I_{Inrush} = I_{GATE} \times \frac{C_{load}}{C_{gd}} \quad \text{(eq. 3)}$$

Hot Swap controller provides constant gate drive current at μA level (5 μA – 20 μA). External Cgd may be needed to keep inrush current is within power FET SOA for different load capacitance levels.

A discrete solution is shown in Figure 10 and simulated results in Figure 11. Cascode structure is demonstrated here, Q1 is SiC JFET and Q2 is low voltage MOSFET. **onsemi** provides separate JFET and LV MOSFET, or Combo JFET which two dices into one package.

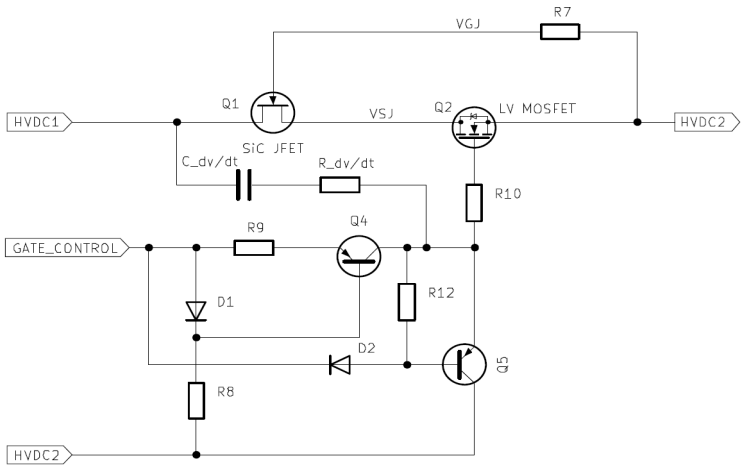

Figure 10. Discrete dv/dt Control Schematic

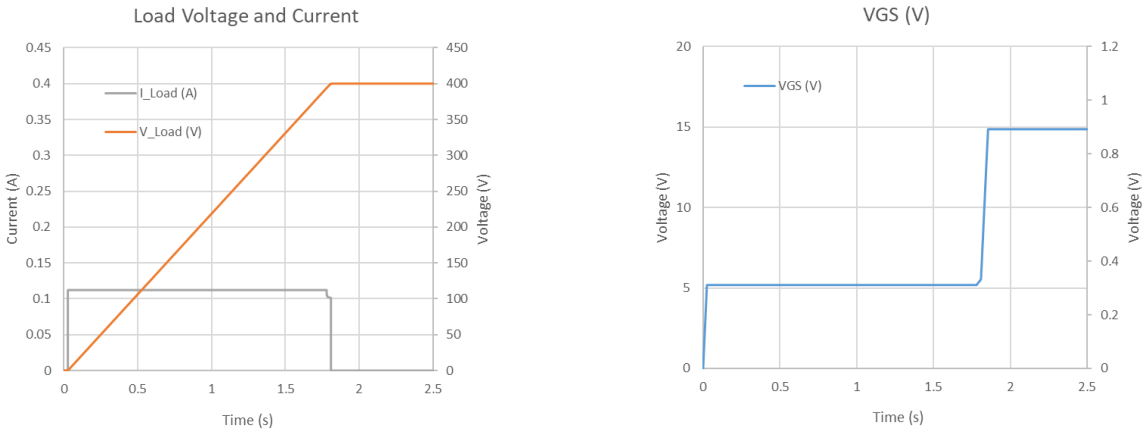

Figure 11. dv/dt Control Simulation Result

Continuous Current Close Loop Mode

The controller senses the load current; this sensed current is feedback to the constant current control loop and is compared with current setting. The difference between the sensed current and set current value is amplified to drive the power FET gate. Certain level of external Cgd between drain of JFET and gate of LV MOSFET is still needed to stabilize the control.

A discrete design is shown in Figure 12 to show the principle of current close loop control.

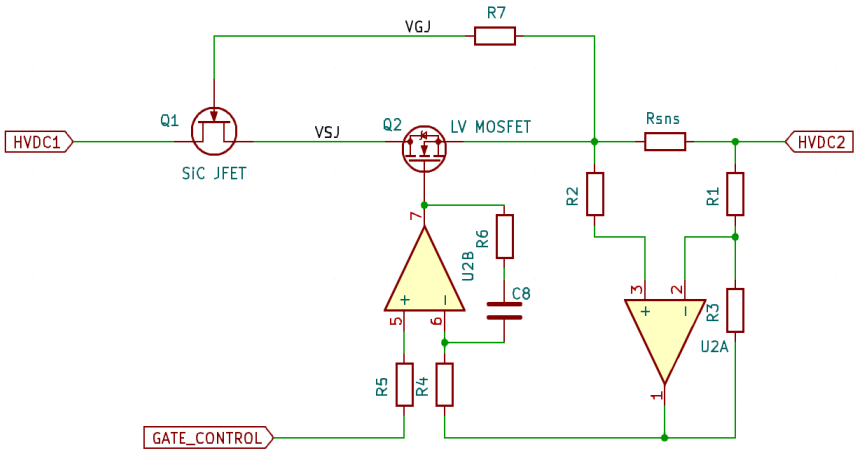

Figure 12. Current Close Loop Control Block Diagram

Discontinuous Current Close Loop Mode

Current close loop control needs enough current sensing resolution to control the current accurately, so there is minimum controllable current level. If the minimum controllable current level is higher than the SOA capability, the discontinues mode (boost mode) method can be used. Discontinues mode means the current is at minimum controllable level with certain pulse length (within SOA), with certain cool down time between two active current pulses. This method balances current control resolution and SOA limits.

Design Practices

Thermal Capability

The maximum allowed power loss to keep the junction temperature within specification is determined by the thermal impedance and ambient temperature (eq. 4).

$$P_{D(MAX)} = \frac{\left[T_{J(MAX)} - T_A\right]}{Z_{JA}} \qquad \text{(eq. 4)}$$

Z_{JA} in eq. 4 is the impedance from device junction to ambient. Thermal stack is illustrated by Figure 13. The thermal impedance from junction to case (Z_{JC}) is characterized and shown on datasheets with curves of different pulse durations. The thermal impedance from case to ambience (Z_{CA}) should be characterized by the application designer.

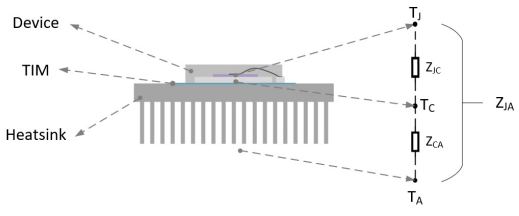

Figure 13. Thermal Impedance

RC thermal model (Foster or Cauer) is equivalent representation of thermal impedance of power FET, to support the calculation or simulation used within SPICE simulator. The Foster model is provided on SiC Combo JFET. Figure 14 shows the thermal transient curves and foster RC network.

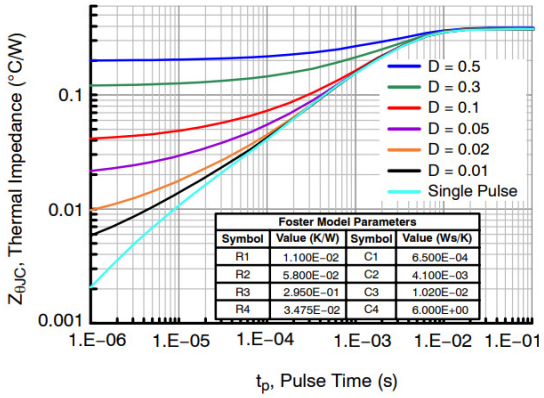

Figure 14. UG4SC075009K4S Thermal Impedance

Figure 15 indicates junction temperature simulation with thermal models including case to ambient. Ploss is the current source in simulator to represent the instantaneous power loss of power FET and TA is a voltage source that represents ambient temperature.

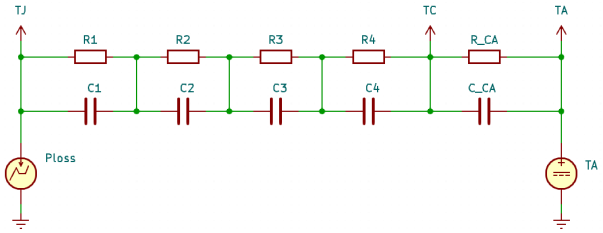

Figure 15. Thermal Model (Foster)

Case to ambient thermal resistance and capacitance impact the junction temperature, SPICE simulations are conducted to show this based on UG4SC075009K4S and conditions in Table 1.

Table 1.

Item	Value	Unit	Note
VDC	400	V	DC input value
Cload	300	μF	Load capacitance
I_Charge	0.15	A	Charge current (constant during pre-charge)
TA	45	°C	Ambient temperature

Simulation (Figure 16) shows the junction temperature during startup current limiting operation based on UG4SC075009K4S under certain case to ambient thermal impedance (Rth_CA = 5 K/W and Cth_CA = 0.1 Ws/K).

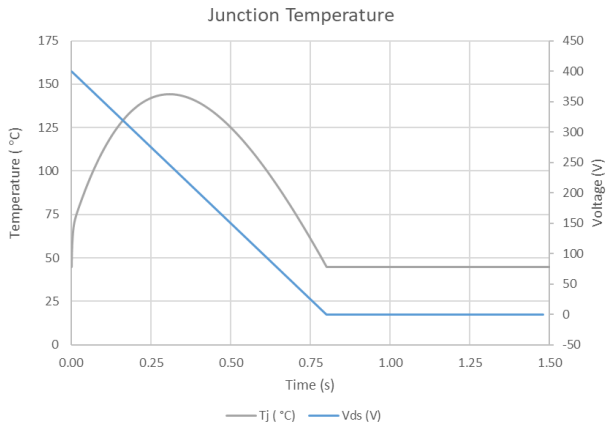

Figure 16. Junction Temperature Simulation Result

Figure 17 shows the simulation results, with different case-to-ambient thermal resistance and capacitance. From this simulation results, the tolerance to thermal resistance is high (from 5 K/W to 20 K/W) when the thermal capacitance is high enough (>0.2 Ws/K) during startup.

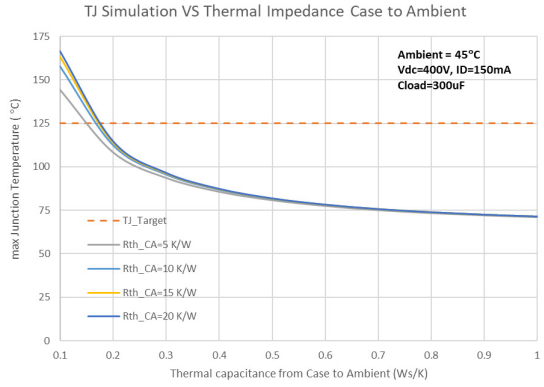

Figure 17. Tj Simulation Results with Different Case-to-ambient Thermal Impedances

The thermal resistance of heatsink is determined by air flow for given design and the thermal capacitance can be calculated with (eq. 5):

$$C_{th\_heatsink} = V \times \varrho \times C_p \qquad \text{(eq. 5)}$$

V is Volume (m^3)

ϱ is Density (kg/m^2, 2700 kg/m^2 for Aluminum)

C_p is Heat capacity (J/kg.K, 904J/kg.K for Aluminum)

The thermal interface material (TIM) is considered as part of the Z_{CA}, the actual thermal impedance should be measured by testing.

Thermal Stability

The SOA curve of power FET may show the idealized curves of drain source voltage (VDS) and drain current (ID) with different pulse width and case temperature.

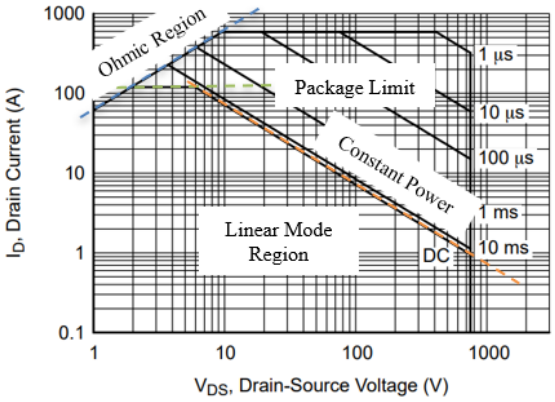

Figure 18. SOA Curves – Constant Power Line

There are basically two different operation modes when power FET is conducting:

- Ohmic Region: the V_{DS} value follows the rule of I_D x Rds(on).
- Linear mode Region: the V_{DS} value is independent with I_D, the V_{DS} is determined by external circuit and I_D is controlled by V_{GS} ($I_D = k \times (V_{GS} - V_{TH})^2$.

With the same current level, when power devices work in linear mode, its power loss is significantly higher than when it works in ohmic mode. Power FET for inrush current limiting will enter linear mode for relatively long time compared to its thermal transient time. This is why the pre-charge current is typically small, must be within the SOA according to the ambient and thermal capability, especially the thermal capacitance discussed previously.

However, actual parts may show different behavior in the zone when V_{DS} is high, and current on actual SOA is smaller compared with constant power lines. This phenomenon is called “Spirito Effect”, causes by hot spot develops locally.

The transfer curve of power FET shows the drain current (I_D) as a function of the gate to source voltage (V_{GS}) at a given junction temperature and drain to source voltage (V_{DS}). Figure 18 shows the typical transfer curve of **onsemi** Gen 4 SiC JFET. There is a cross over point between two curves at different junction temperatures. At this point, the drain current will not change when the junction temperature changes, meaning the temperature coefficient is zero (ZTC). Below this point, hot spot can be developed because of the drain current becoming higher when the junction temperature increases. A hotter area on the chip focuses more on current that causes further heating and possibly failure from thermal runaway in a localized area. AND90317 – SiC JFET in Active Mode Applications shows the instability analysis method based on transfer curves and thermal transient.

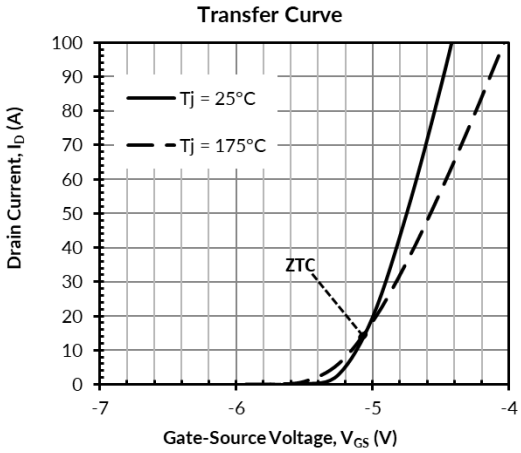

Figure 19. SiC JFET Transfer Curve

Thermal runaway happens when power loss increases more than the power can be thermally dissipated.

$$\frac{\partial P_{loss}(t)}{\partial T_J(t)} \le \frac{\partial P_{\theta}(t)}{\partial T_J(t)} \qquad \text{(eq. 6)}$$

With $P_{loss}(t) = i_D(t) \times V_{DS}(t)$ and $\partial T_J(t) = \partial P_{\theta}(t) \times Z_{\theta}(t)$, the condition of thermal stability can be:

$$\frac{\partial i_D(t)}{\partial T_J(t)} \le \frac{1}{Z_{\theta}(t) \times V_{DS}(t)} \qquad \text{(eq. 7)}$$

For hot swap application, all parameters change, with different junction temperature, time or voltage. So, verification by testing actual design is more trustworthy than theoretical analysis based on eq. 6 and 7.

Test Result

Combo JFET (UG4SC075011K4S) is tested with a hot swap controller for charging 330 μF capacitor to 400 V, with 160 mA charging current the time to fully charge is 800 ms.

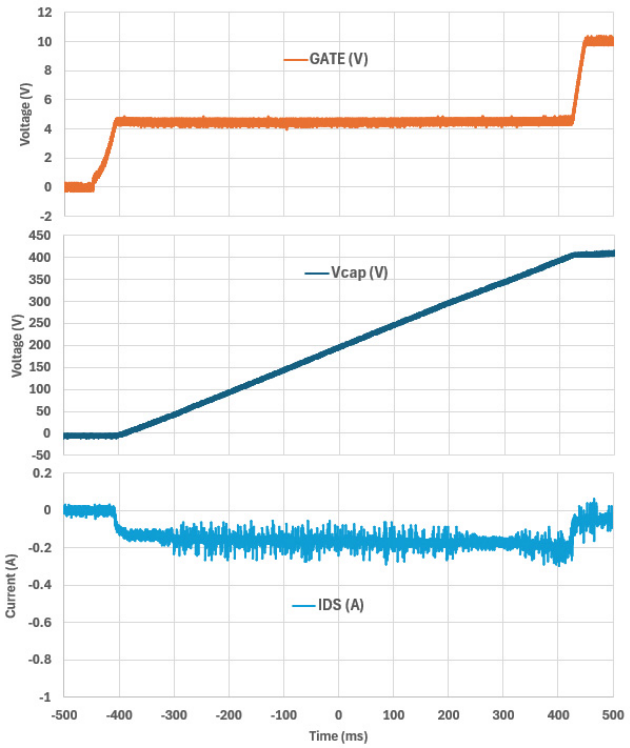

Figure 20. Hot Swap Startup Test Result

References

Refer to AND90317 – SiC JFET in Active Mode Applications for details.

REVISION HISTORY

Revision	Description of Changes	Date
0	Initial document release.	12/10/2025

ADDITIONAL INFORMATION

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