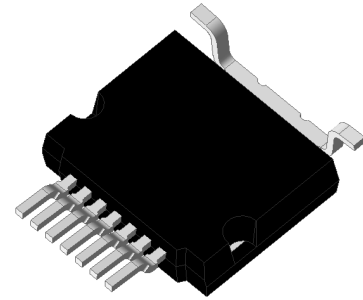


T2PAK: Top-Side Cooled Package Designed for Automotive and Industrial High Voltage Applications

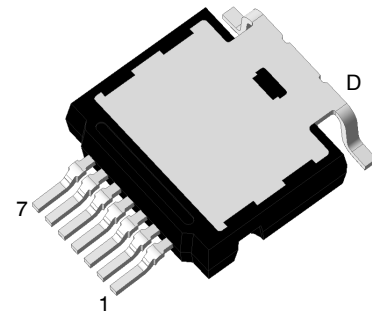
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Introduction

To enhance its advanced power package portfolio, **onsemi** has introduced the T2PAK and BPAK, top-side cooled packages designed to meet stringent standards for automotive and industrial high-voltage (HV) applications. Unlike bottom-side cooling packages like D2PAK and TOLL, which require power extraction through the printed circuit board, the T2PAK and BPAK utilize top-side cooling. This design ensures direct thermal contact with the heatsink, significantly improving thermal performance. With its top-side cooling and leadless design, T2PAK minimizes stray inductance by eliminating long leads and enabling tighter current loops than D2PAK or TO packages. This results in improved switching behavior, reduced voltage overshoot, and better EMC performance – making T2PAK a strong choice for compact, high-efficiency power designs. This advancement allows for higher power density, addressing the evolving needs of high-performance applications. **onsemi**'s initial offerings in this new type of package include eight Elite-SiC Silicon-Carbide MOSFETs.



a) Bottom View



b) Top View

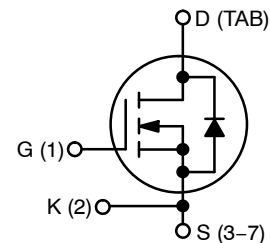
Figure 1. T2PAK Package Views
Table 1. onsemi T2PAK AUTOMOTIVE QUALIFIED PRODUCT

Technology	650 V	950 V / 900 V
M3S	NVT2012N065M3S	NVT2011N095M3S (950 V)
	NVT2016N065M3S	
	NVT2023N065M3S	
M2	NVT2012N065M2	NVT2016N090M2 (900 V)

Table 2. onsemi T2PAK INDUSTRIAL QUALIFIED PRODUCT

Technology	650 V
M3S	NTT2012N065M3S
	NTT2016N065M3S
	NTT2023N065M3S

This application note aims to guide hardware design engineers working on automotive on-board chargers, HV DC/DC systems, and industrial SMPS in mounting these packages and leveraging the thermal properties of the T2PAK. The application note is organized as follows: [T2PAK Package Details](#) describe the T2PAK package specifications. [Soldering Considerations](#) discuss key aspects for reliable electrical connections. [Moisture Sensitivity Level](#) addresses device handling and storage. [Device Mounting](#) provides guidelines for optimal device mounting practices.


Figure 2. Pin-Out for SiC MOSFET T2PAK

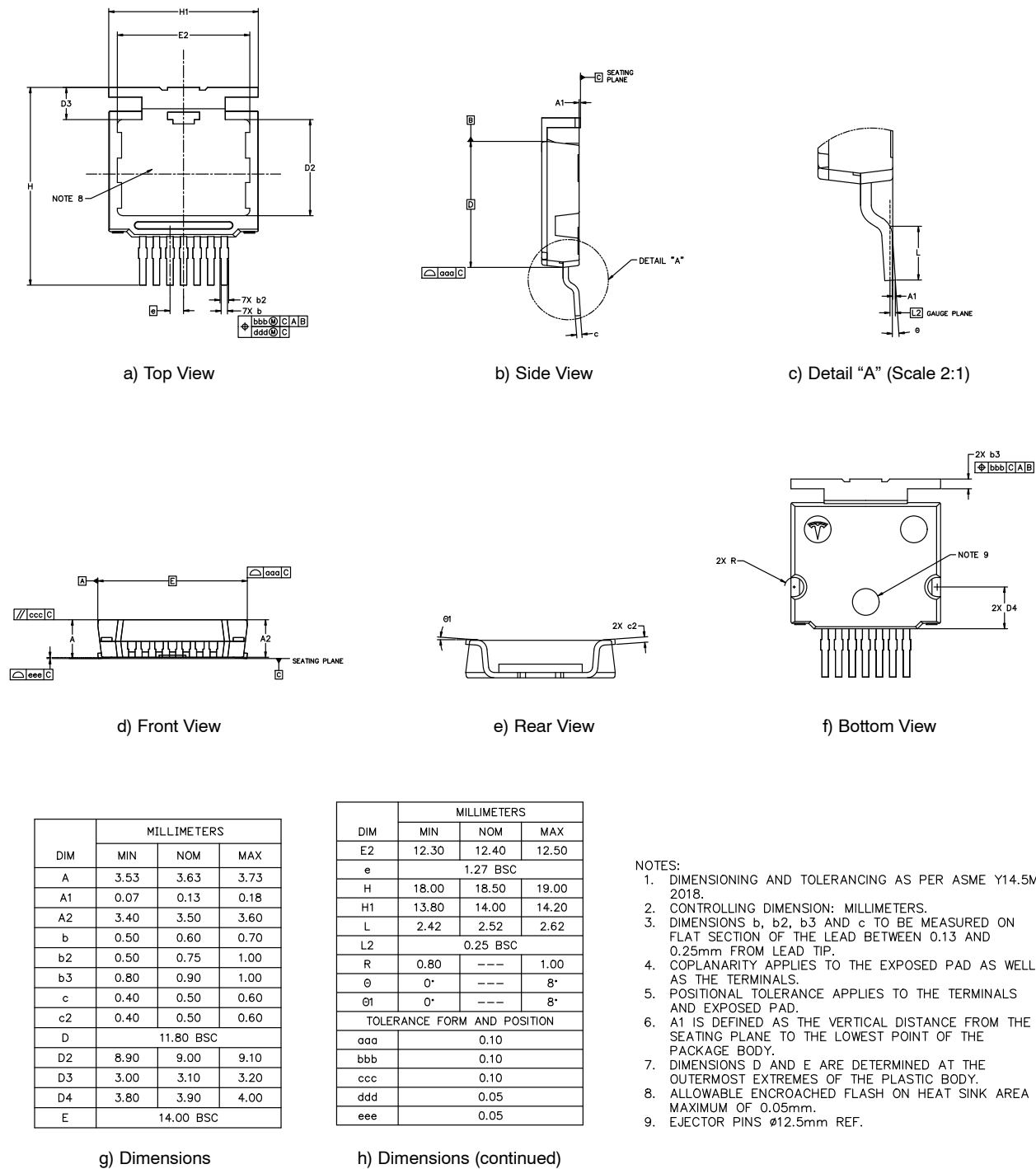


Figure 3. T2PAK Package Mechanical Outline

[Commutation Loop Suggestions](#) discusses commutation loop consideration for T2PAK device. [Thermal Performance](#) analyzes thermal performance, essential for maintaining device integrity under operational conditions before the app note is concluded. Figure 1a shows package

bottom view and package Figure 1b shows package top view. Pin configuration is shown in Figure 2. Pin Figure 1b shows the pin location as: Pin 1 is gate; Pin 2 is Kelvin and Pin 3–7 is source. In Figure 1b Drain tab is marked with D.

T2PAK Package Details

Figure 3 shows the details of the package outline for T2PAK. Sub-figure a presents the top view, while Figure b shows the side view. Detail A (Figure 3c) illustrates the pin dimensions from the side view, complemented by the front view (Figure 3d) and rear view (Figure 3e) and Figure 3f depicts the bottom view. Figure 3g and Figure 3h contain all relevant dimensions associated with Figure 3. The body of the package is approximately 11.80 mm x 14.00 mm x 3.63 mm (D x E x A), while the plan view dimensions inclusive of the leads are 18.50 mm x 14 mm (H x H1).

The T2PAK and D2PAK (TO-263) packages are both high-power surface-mount solutions designed for efficient thermal management in compact PCB layouts. While they share similar electrical footprints, their thermal architecture differs significantly. The D2PAK is a bottom-side cooled package, relying on the exposed drain pad to transfer heat into the PCB copper and through thermal vias to internal or backside copper planes. In contrast, the T2PAK introduces a top-side cooling feature via an integrated through-hole tab, which allows direct attachment to an external heatsink or metal chassis. This top-side thermal path provides a more efficient and controlled heat dissipation mechanism, especially in applications where PCB thermal capacity is limited or where forced air cooling is available on the component side.

This architectural difference translates into measurable thermal performance gains. For a 32 mΩ device, the T2PAK achieves a junction-to-case thermal resistance of 0.7 °C/W, slightly better than the 0.75 °C/W of the D2PAK. The advantage becomes more pronounced in lower-resistance, higher-current devices: a 12 mΩ T2PAK device offers 0.3 °C/W, compared to 0.35 °C/W for its D2PAK counterpart. These improvements are largely attributed to the T2PAK's ability to offload heat directly to a heatsink, bypassing the thermal limitations of the PCB. As a result, T2PAK is particularly well-suited for thermally constrained designs or environments requiring enhanced thermal headroom, such as automotive power modules, industrial drives, and high-efficiency DC-DC converters.

The recommended PCB landing pattern for T2PAK is shown in Figure 5. Pin numbering shown in the package top view picture, pin 1 on the lower right corner being the gate, with pin 2 is the kelvin source pin to provide a reference potential for the driver, and pins 3 through 7 provide the source connections. Drain connection is made via the large extended drain tabs, which are common with the exposed drain pad in the center of the top side of the package, which is the main heat sink interface area.

Soldering Considerations

The surface mount board layout is a crucial aspect of the overall design. It is essential that the footprint for the semiconductor packages is accurately sized to ensure a proper solder connection interface between the board and the package. When the pad geometry is correct, the packages will self-align during the solder reflow process. Figure 4

illustrates the recommended landing pattern for T2PAK. The leads of T2PAK devices are tin-plated with Pb-free finishes, which guarantee excellent solderability on PCB pads.

For optimal thermal and mechanical reliability during soldering, T2PAK devices should always be preheated prior to reflow. Preheating minimizes thermal shock and reduces stress on the package, especially given the high thermal mass of power semiconductors. According to **onsemi**'s soldering guidelines [2], the temperature difference between the preheat and peak soldering stages should not exceed 100 °C, and the maximum temperature gradient during transition should be limited to 5 °C/s. Additionally, the soldering temperature should not exceed 260 °C for more than 10 seconds. Gradual cooling after soldering is recommended to prevent latent mechanical failures due to rapid thermal contraction. These practices are essential for maintaining junction integrity and long-term reliability in T2PAK-mounted assemblies.

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed to minimize the thermal stress to which the devices are subjected.

- Preheat the device.
- The temperature difference between the preheat and soldering should be 100 °C or less. Soldering a device without preheating can cause excessive thermal shock and stress, which can result in damage to the device.
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings 260 °C. When using infrared heating with the reflow soldering method, the difference should be a maximum of 10 °C.
- The soldering temperature and time should not exceed 245 °C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5 °C/s or less.

The T2PAK is intended to be mounted onto PCB board using the reflow soldering process. The package follows the IPC/JEDEC J-STD-020E [1] reflow profile. The reader is also directed to **onsemi** application note SOLDERRM [2], which provides the reflow profile as illustrated in Figure 5.

T2PAK packages are compatible with both Sn-Pb (tin-lead) and Pb-Free (lead-free) soldering processes, each requiring distinct thermal profiles. Sn-Pb assembly uses eutectic solder alloys with a lower melting point of 183 °C, while Pb-Free assembly – typically using SAC305 alloy – requires a higher liquidus temperature of 217 °C and peak reflow temperatures up to 245 °C. As per soldering guidelines, both processes recommend a preheat range (T_{smin} to T_{smax}) of 100–150 °C for Sn-Pb and 150–200 °C for Pb-Free, with a soak time of 60–120 seconds. The ramp-up rate should not exceed 3 °C/s, and time above

liquidus should be maintained between 60–150 seconds. Peak body temperature for T2PAK should reach 245 °C, with a dwell time of 30 seconds within 5 °C of peak. Ramp-down should be controlled at 6 °C/s, and the total time from ambient to peak should not exceed 6 minutes. Proper preheating and thermal control are essential, especially for Pb-Free processes, to minimize thermal stress and ensure reliable solder joints.

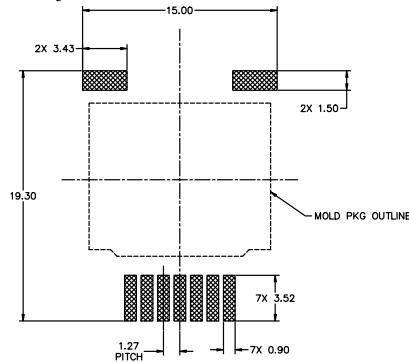


Figure 4. Recommended PCB Landing Pattern

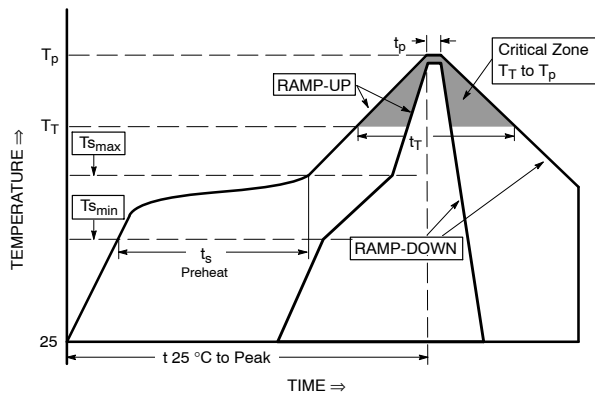


Figure 5. Pb-Free Solder Heating Profile [2]

Table 3. CLASSIFICATION REFLOW PROFILE PER [2]

Profile Feature	Sn-Pb Assy	Pb-Free Assy
Temperature Min (T_{smin})/°C	100	150
Temperature Max (T_{smax})/°C	150	200
Time (t_s) from T_{smin} to T_{smax} /s	60–120	60–120
Ramp-up Rate (T_L to T_P)/°C/s	3	3
Liquidus Temperature (T_L)/°C	183	217
Time (t_L) Maintained above T_L /s	60–150	60–150
Peak T2PAK Body Temperature (T_P)/°C	245	245
Time (t_P) within 5 °C of Specified Classification Temperature (T_C)/s	30	30
Ramp-down Rate (T_P to T_L), °C/s	6	6
Maximum Time from 25 °C to Peak Temperature, Min	6 (max)	6 (max)

Table 3 provides recommended values for various stages of the reflow process. While this profile may vary among soldering systems, it serves as a reliable starting point and should be adjusted based on factors such as PCB board size and thickness, component density, types of components, solder paste used, and the type of board or substrate material. Developing a soldering profile should begin with the recommended profile from the solder paste manufacturer, ensuring that temperature and time limits for all components on the assembly are adhered to. Various types of reflow soldering equipment, including infrared (IR), forced convection, and vapor phase, are available. Forced convection ovens are particularly suitable for power electronics designs due to their even heating distribution across PCB boards, leading to uniform heat distribution to the components on the board. If components must be placed on both sides of the PCB, the T2PAK device should be mounted last because the wetting force will not hold the T2PAK device during the second reflow. For reworking PCB components, localized reflow is recommended instead of a second reflow [2].

The following notes apply to Table 3 [2]:

- All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), TP shall be within ± 2 K of the live-bug TP and still meet the TC requirements, otherwise, the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperatures, refer to JEP140 [3] for recommended thermocouple use.
- Reflow profiles in this document are for classification or preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table 1. For example, if TC is 260 °C and time t_P is 30 seconds, this means the following for the supplier and the user.
 - ♦ For a supplier: The peak temperature must be at least 260 °C. The time above 255 °C must be at least 30 seconds.
 - ♦ For a user: The peak temperature must not exceed 260 °C. The time above 255 °C must not exceed 30 seconds.
- All components in the test load shall meet the classification profile requirements.
- SMD packages classified to a given moisture sensitivity level by using Procedures or Criteria defined within any previous version of J-STD-020, JESD22-A112 (rescinded), IPC-SM-786 (rescinded) do not need to be reclassified to the current revision unless a change in classification level or a higher peak classification temperature is desired.
- SMD: Wave soldering is not recommended.

Moisture Sensitivity Level

In accordance with JEDEC J-STD-033 and J-STD-020 standards, T2PAK products are classified as Moisture Sensitivity Level 1 (MSL1). As a result, they do not require dry packing and have no defined floor life limitations under standard ambient conditions, simplifying storage and handling requirements.

Device Mounting

To achieve optimal performance, top-side cooling devices, in addition to the specified soldering mounting profile, require a high-performance thermal connection to cold plates or heatsinks. While the thermal resistance junction-to-case ($R_{\theta JC}$) is a quantity dependent on chip size, thickness, die attach, and copper lead frame, and is well-controlled and declared in the datasheet, the overall thermal behavior still strongly relies on the stack-up connecting the exposed pad to the heatsink. Achieving a high-performance thermal connection involves the choice of interface materials, typically referred to as thermal interface material (TIM). The selection of suitable TIM and the implementation of an accurate and repeatable dispensing process are key factors in achieving optimal thermal performance, ensuring reliability at both the device and board levels, and enhancing the safety of electrical insulation. Three options have been studied to propose an effective approach in this regard and to demonstrate the process of evaluating interfaces.

Liquid Gap Filler (Figure 6)

The relatively low viscosity of most liquid gap fillers (Figure 6) makes them an excellent choice for conforming to the line of contact between the exposed pad and the heatsink. The thickness and final shape of the TIM are controlled primarily by the pressure applied between the heatsink and the package itself (pressure applied by the PCB). To maintain a controlled thickness, the distance between the heatsink and PCB is often regulated using standoff systems, such as screws or spring-loaded pins. A few crucial aspects must be carefully weighed when using liquid gap fillers:

1. TIM Material Properties

- Evaluation and validation of the insulation properties of the TIM material is critical. The gap filler serves as the sole insulation between the package tab (high voltage) and the heatsink (ground). The minimum thickness to support such voltage, depending on the material, may range from 500 μm to 1 mm.
- While the thermal conductivity of commercially available liquid gap fillers spans from 1.6 W/(m·K) to 9 W/(m·K), the suggested test value by **onsemi** is higher than 5 W/(m·K)

2. Optimal Dispensing

- Over dispensing TIM to ensure optimal insulation will come at the expense of thermal performance. Refer to data reported in the thermal simulation and thermal testing sections for more details.

3. Shrinkage During Curing

- It is important to acknowledge that the gap filler material may experience shrinkage during the necessary curing process.

Balancing these aspects is essential for achieving the desired electrical insulation while maintaining optimal thermal performance.

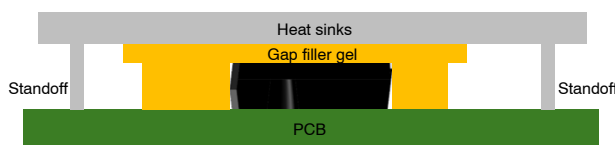


Figure 6. Liquid Gap Filler

Pre-Formed Gap Filler Pad (Figure 7)

Preformed gap filler pads offer an alternative solution. In this context, thickness control is granted by design. However, the overall mounting cost can potentially increase, and critical aspects in controlling the distance between the heatsink and PCB may become more challenging: the pre-cut thermal pad, while providing consistency in thickness, will not conform as well to its surroundings due to its predetermined shape.

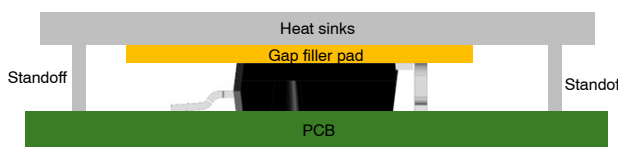


Figure 7. Pre-Formed Gap Filler Pad

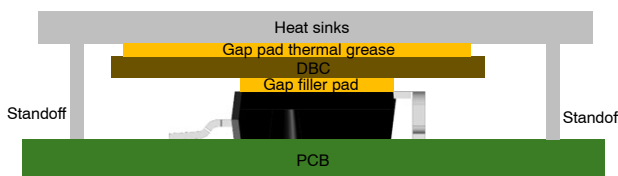


Figure 8. Ceramic Insulator

Ceramic Type Insulators (Figure 8)

Materials like Al_2O_3 or ALN can be introduced into the stack to provide stable and reliable insulation, especially when combined with a thinner layer of liquid gap filler ranging from 250–500 μm . While this thermal stack is often seen as the most reliable insulation, it does incur a significant cost without offering substantial benefits in terms of thermal conductivity when compared to Option 1.

Commutation Loop Suggestions

The commutation loop is a critical consideration in hardware design, especially in high-speed switching applications. Minimizing parasitic inductance within this loop directly contributes to reduced switching losses and improved overall system efficiency.

Top-cooled packages, such as the T2PAK, offer a distinct advantage over bottom-cooled models in this regard. Their thermal design allows for more flexible electrical routing, enabling a more compact and optimized commutation loop.

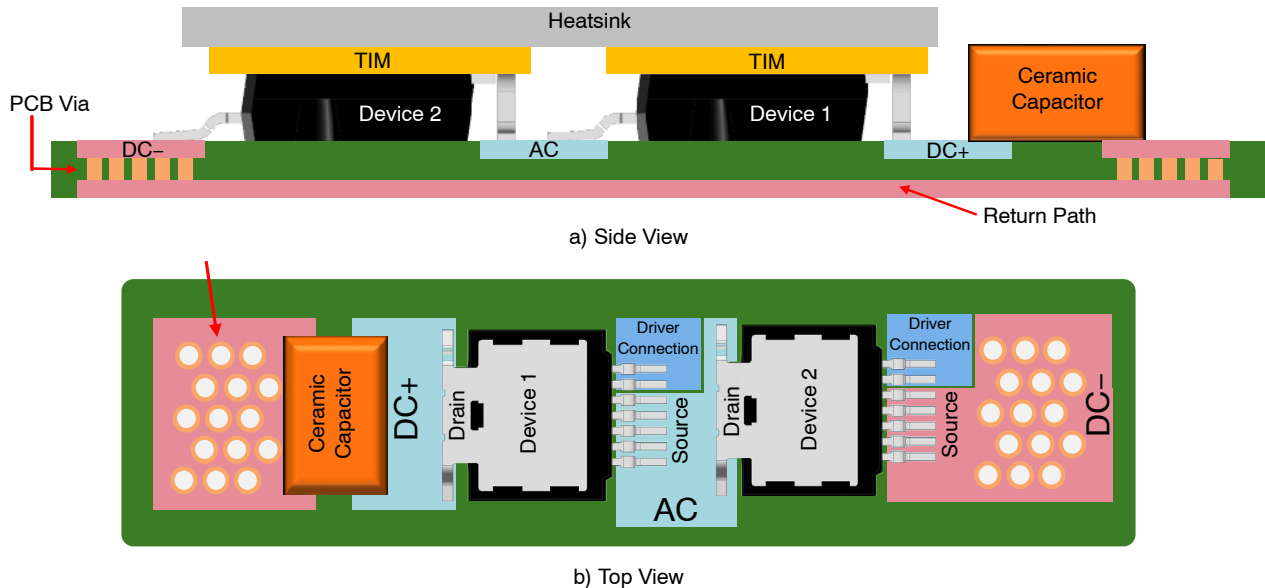


Figure 9. Commutation Loop Suggestion in Hardware Design

As illustrated in Figure 9, a half-bridge configuration can be achieved by placing two T2PAK devices side-by-side:

- DC+ is connected to the drain of Device 1.
- The source of Device 1 connects to the drain of Device 2.
- The source of Device 2 then connects to DC-.

To complete the commutation loop, the return path can be routed through the bottom layer of the PCB, running parallel to the top-mounted devices. Vias are used to interconnect the top and bottom layers, forming a compact loop geometry. This arrangement promotes magnetic flux cancellation, which significantly reduces parasitic induction. In our Double Pulse Test (DPT) setup, this configuration achieved a loop inductance of just 9 nH, validating the effectiveness of the layout.

In contrast, bottom-cooled packages rely on the PCB's bottom copper layer for thermal dissipation, which restricts its use for electrical routing. This constraint makes it difficult to implement a compact commutation loop, often resulting in longer trace paths and higher parasitic inductance. Since the bottom layer must be dedicated to heat sinking – typically through thermal vias and large copper areas – routing the return path in close proximity to the power loop becomes impractical. This leads to less effective flux cancellation and higher loop inductance, which can negatively impact switching performance.

Thermal Performance

Top cooled packages in general provide improved thermal performance relative to traditional SMD parts due to the ability to extract heat directly from the exposed metal pad (drain for MOSFETs, collector for IGBTs, cathode for rectifiers), without the thermal resistance of the intervening PCB material as is the case with bottom cool packages. As mentioned above, to gain maximum cooling benefit care must be taken in the design of the thermal system in which the power device operates.

The T2PAK package, with its top-side cooling capability, offers a distinct thermal advantage by enabling direct contact with heatsinks or cold plates, by passing the limitations of PCB-based heat transfer seen in bottom-cooled SMD packages like TO-263-7. Research based on converters [7] has shown that integrating a copper heat spreader on top of the device can reduce TIM thermal resistance from 0.85 K/W to 0.05 K/W, significantly lowering device temperatures and nearly doubling power handling capability. Similarly, studies on SiC SMDs [8] demonstrated that replacing thermal vias with solid copper pedestals increased heat dissipation from 13.2 W to 36.4 W, highlighting the importance of minimizing thermal bottlenecks. While these solutions are effective in reducing the thermal resistance of the PCB, they are expensive as additional manufacturing steps are required. In contrast, the top-cooled T2PAK package allows heat dissipation directly

through the top of the device such that no additional costly manufacturing steps are required. These findings reinforce the effectiveness of T2PAK's thermal design, where optimized TIM compression, mechanical clamping, and optional heat spreaders can be leveraged to achieve low $R_{th(jf)}$ and high thermal efficiency in compact, high-power applications.

Test Setup and Methodology

The device under test (DUT) is an NVT2016N065M3S SiC MOSFET, which is directly mounted onto a cold plate using a T-Global TG-A6200 [6] thermal gap pad. This TIM has a thermal conductivity of 6.2 W/m-K and a thickness of 1 mm, ensuring efficient heat transfer between the device and the cold plate.

To enable accurate junction temperature measurement, the MOSFET package was laser-decapitated, exposing silicon die. A thermocouple was then affixed directly onto the die surface to capture real-time temperature data. After sensor placement, the package was resealed using MG Chemicals 832HT-A [5], a high-temperature epoxy, to maintain mechanical integrity and thermal behavior.

- Figure 10a illustrates the attachment of a K-type thermocouple to the exposed die surface.
- Figure 10b shows the complete assembly of the DUT on the cold plate, including the TIM layer.

Accurate torque application is critical, as it directly influences the contact pressure and, consequently, the thermal resistance of the interface. 0.3 Nm of torque is applied to achieve efficient heat transfer.

The cold plate is actively cooled using a 50/50 water-ethylene glycol (WEG) mixture, circulated at a flow rate of 6.0 LPM and maintained at a constant temperature of 20 °C. To generate heat within the device, the body diode of the SiC MOSFET is forward-biased. A 20 A current source is used to conduct current through the diode, and the corresponding voltage drop (V_{SD}) is measured. The product of current and voltage provides power dissipation, which is used to calculate junction-to-case thermal resistance by analyzing the temperature rise from the die to the cold plate.

Instrumentation and Measurement:

- Current Source: Keysight E36234 (20 A)
- Voltage and Temperature Measurement: Keithley DMM6500
- Temperature Sensors: TEWA TTS-5KC3-BZ NTC thermistors (5 k Ω , B = 3977 K), selected for their high sensitivity and electrical isolation

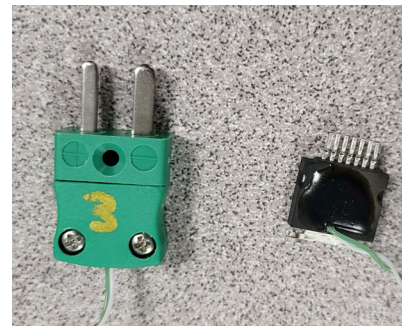
Measured Results

The T2PAK package, with a die area of 11.9 mm², demonstrated excellent thermal performance. At a torque setting of 0.3 Nm, the thermal resistance from junction to case ($R_{th(jf)}$) is measured at 1.06 K/W, with a tolerance of ± 0.08 K/W. When the torque is increased to 0.35 Nm, the

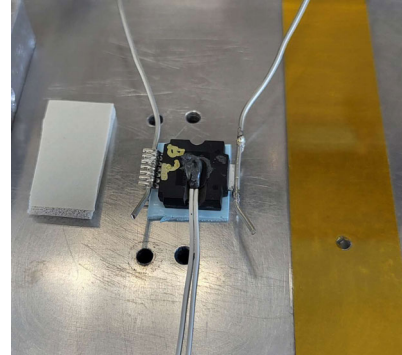
thermal resistance decreases to 0.93 K/W, also with a tolerance of ± 0.08 K/W. This indicates that higher torque settings improve thermal contact, thereby reducing thermal resistance.

These results highlight the strong correlation between mechanical clamping force and thermal resistance. The increase in torque from 0.3 Nm to 0.35 Nm resulted in a 12% improvement in $R_{th(jf)}$, primarily due to better TIM compression and reduced thermal contact resistance.

Although the TG-A6200 TIM maintains stable thermal conductivity under pressure, its thickness significantly decreases with compression. This reduction in thickness directly improves thermal transfer by minimizing the thermal path between the device and the cold plate. The study confirmed that even small increases in torque can lead to meaningful improvements in thermal performance.



a) DUT with thermistor attached



b) Measurement setup

Figure 10. Experimental Test Setup

The T2PAK package offers a compelling thermal solution for high-power applications. The T2PAK package demonstrates excellent thermal performance, outperforming the BPAK package despite a smaller die area. Its larger tab area and compatibility with high clamping forces make it ideal for thermally demanding applications. When paired with a high-performance TIM and properly controlled torque, T2PAK consistently delivers low $R_{th(jf)}$ values, making it ideal for thermally constrained designs. This study reinforces the importance of mechanical design, material selection, and measurement accuracy in achieving optimal thermal performance.

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REVISION HISTORY

Revision	Description of Changes	Date
0	Initial document release.	11/24/2025
1	Update of the Introduction paragraph on the front page.	12/17/2025

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