Electrical Safety Product Self-Test Ground Fault Circuit Interrupter (ST GFCI) Controller Application Note (NCS37021)

AND90381/D

Introduction

This application note provides practical guidelines for designing with the ST GFCI controller series. A GFCI is a device that disconnects the AC load supply voltage when a leakage current to earth ground is detected. This leakage current can be a current through the human body that is accidentally touching an electrical circuit. These controllers are intended to detect ground-fault (GF) and ground-neutral fault (GNF) in residential, commercial, and industrial AC power systems.

Description

The NCS37021 is designed to support UL 943 compliant signal processing for GFCI applications with integrated Self-Test functionality. While we provide robust tools and support, the final implementation and validation should be performed by the customer to ensure it meets specific requirements and standards. The device integrates a flexible power supply (including a 12 V shunt, two 3.3 V internal series regulators and 1.8 internal regulator), GF and GNF detection circuits. Self-Test is monitored at start-up and then every minute. Push To Test (PTT) function allows to disconnect load contact when it is enabled.

Features

- Meets UL943 Self-Test GFCI Requirements
- 4.0−12 V Operation. (120−480 V AC Mains with the Appropriate Series Impedance)
- Wide Operating Temperature Range from −40 °C to 95 °C
- Low Quiescent Current
- Optimized Solenoid Deployment (Coil is not Energized Near the AC Mains Zero Crossings)
- Power Supply Monitor that Verifies Full Diode Bridge Operation
- Tiered GF Trip Times that Increase Immunity to Noise
- Under-voltage Detection that Allows for Increased Operation at Lower AC Input Voltages
- Intelligent Sensing Differentiating Ground Fault versus Ground Neutral Fault (Prevent Nuisance Tripping)
- 16 Pin QFN Package
- This is a Pb-Free Device

Typical Applications

- GFCI Receptacles
- Load Panel GFCI Breakers
- In-line GFCI Circuits (Power Cords)

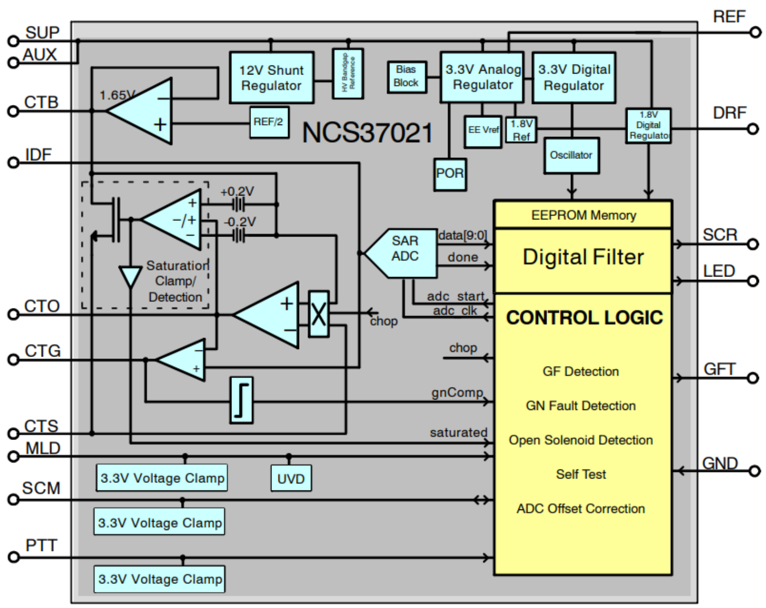

Figure 1. NCS37021 Simplified Block Diagram

Table 1. PIN DESCRIPTION DESCRIPTION

Pin #	Name	Pin Description
1	CTG	Ground Neutral current transformer stimulus
2	SCM	Test input for SCR functionality
3	CTB	Differential current transformer bias voltage
4	CTS	Differential current input
5	CTO	Differential current to voltage output
6	IDF	Differential low pass filter/ADC input
7	REF	3.3 V Internal reference voltage
8	GND	Electronics ground
9	PTT	Reference current bias input Push to Test
10	MLD	Mains level/under voltage detector
11	AUX	Auxiliary power supply input
12	SUP	Power supply input
13	DRF	1.8 V Internal reference voltage
14	LED	End of life LED drive
15	GFT	Differential self-test output signal
16	SCR	SCR gate drive signal

NCS37021 APPLICATION INFORMATION

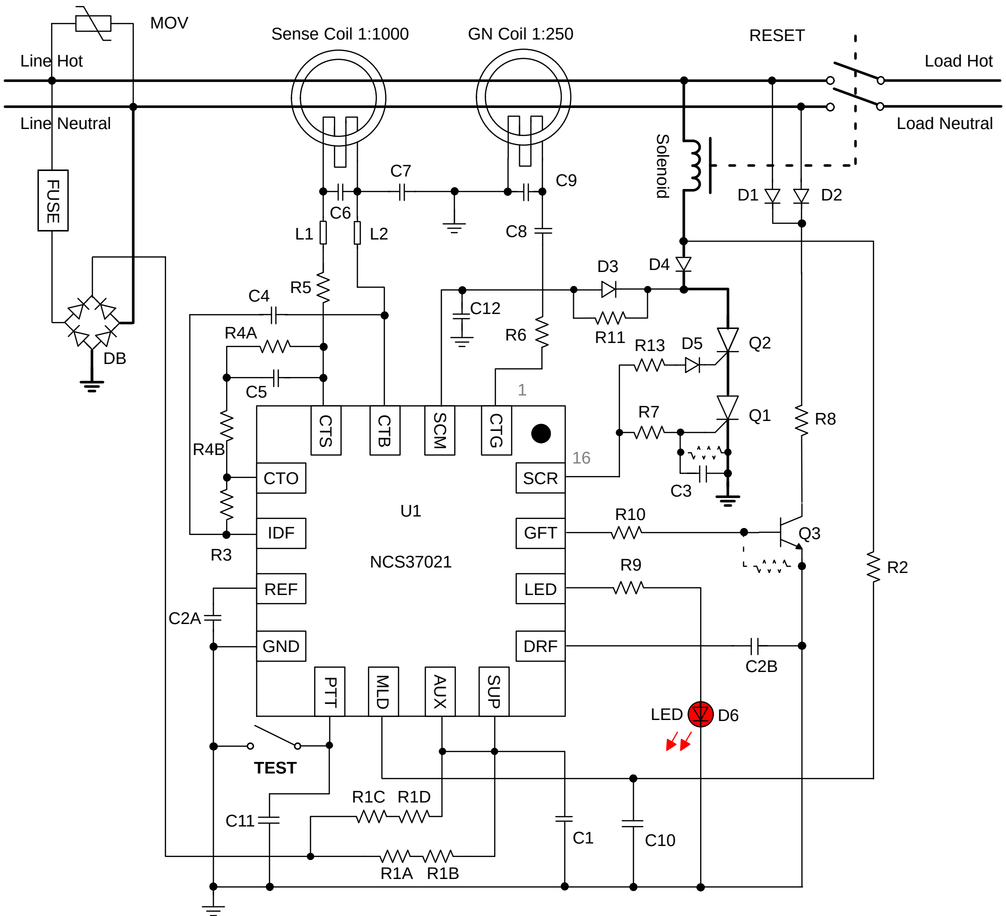

Figure 2. GFCI Receptacle Application Diagram

Table 2. RECOMMENDED EXTERNAL COMPONENTS

Component Type	Instance	Value	Note
SCR	Q1, Q2	–	
NPN	Q3	–	MMBT6517LT1-D
Diode Bridge	DB	–	
Diode	D1, D2, D3, D4, D5	–	1N4007
LED	D6	–	LED for self-test failure
Capacitor	C1	1 μF	SUP pin holding capacitor
Capacitor	C2A, C2B	1 μF	Internal 3.3 V and 1.8 V reference filter cap
Capacitor	C3	100 nF	SCR gate filter capacitor
Capacitor	C4	56 nF	Anti-aliasing filter (140 Hz corner frequency)
Capacitor	C5	2.2 nF	High frequency filter
Capacitor	C6	33 nF	Differential current filter capacitor
Capacitor	C7	1 nF	CTB bias filter
Capacitor	C8	10 nF	Ground Neutral CT resonance capacitor (Set the CTG GN Trip Frequency approximately 4 kHz)
Capacitor	C9	120 pF	Ground Neutral CT AC coupler
Capacitor	C10, C11, C12	100 pF	Ground noise filter
Resistor	R1A, R1B, R1C, R1D	25 kΩ	Current limit resistors
Resistor	R2	1 MΩ	MLD current limit/under voltage attenuator
Resistor	R3	20 kΩ	Differential filter resistor
Resistor	R4A	36 kΩ	Precision resistor (1%), Differential burden/CT low pass filter
Resistor	R4B	50 Ω	CT low pass filter
Resistor	R5	370 Ω	Differential burden resistor, 1% tolerance
Resistor	R6	0−10 Ω	Sets the GN sensitivity
Resistor	R7, R13	4.7 kΩ	Sets the SCR gate current
Resistor	R8	15 kΩ	Controls the self-test current in the Q3
Resistor	R9	3.3 kΩ	LED current limiter resistor
Resistor	R10	10 kΩ	Sets the current in the base of Q3
Resistor	R11	1 MΩ	Current limit resistor for SCM
Inductor	L1, L2	1 k @ 100 MHz	CIM05U102, CT RF filter
Current Transformer	CT1	1000	Differential current transformer
Current Transformer	CT2	250	GN current transformer

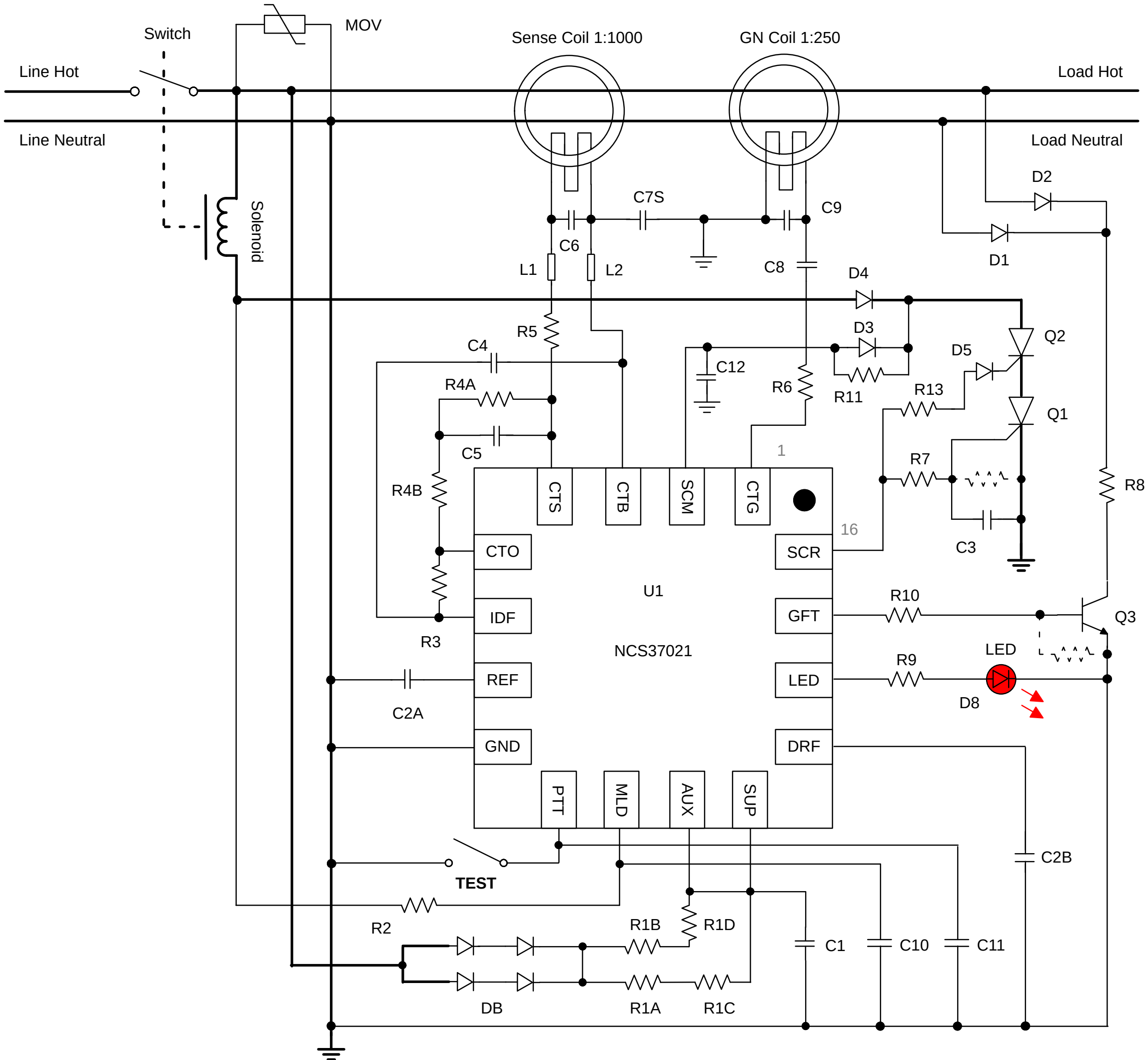

Figure 3. Circuit Breaker Application Diagram (Half Bridge Supply)

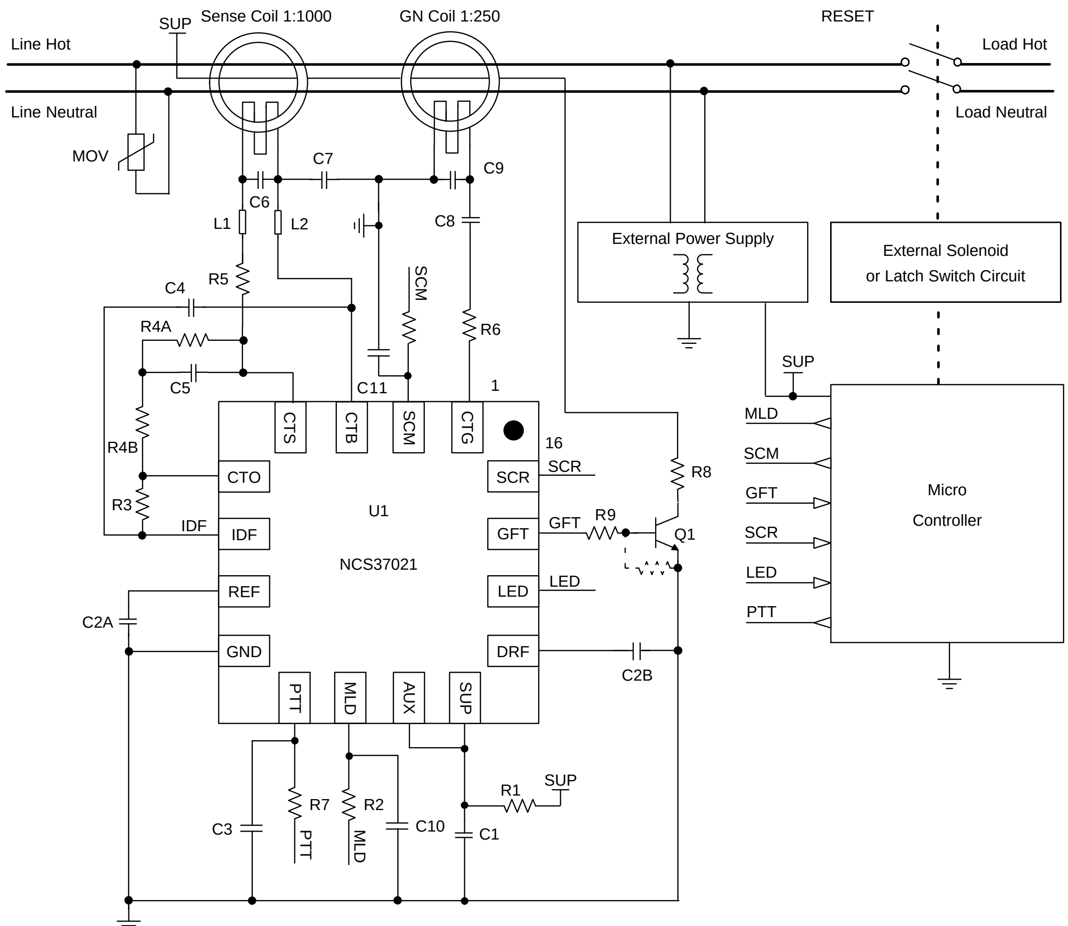

Figure 4. GFI Application Diagram with Microcontroller

- MLD: It is recommended to add RC filter to remove glitches/noises from MCU. Additionally, The MLD pin should be synchronized to the LINE phase.
- SCM: It is recommended to add RC filter to remove glitches/noises from MCU. The SCM pin needs to pre-bias during the Self-Test.
- GFT: Active High during Self-Test.
- SCR: Active High for SCR signal.
- LED: Active High for LED signal.
- PTT: The PTT pin has a 50 kΩ pull up resistor internally. To enable the PTT function, the voltage should go below 1.2 Volts.

*For further information and detailed setup support, please contact **onsemi** applications team.*

Principle of Ground Fault Detection

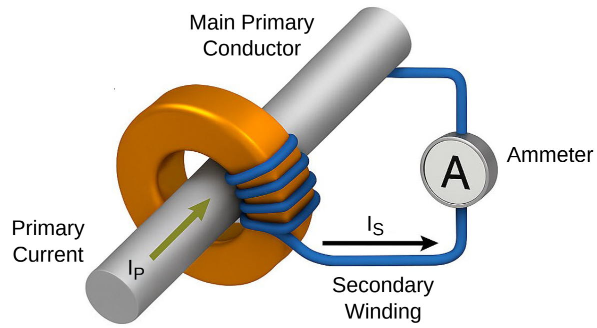

Figure 5. Operating Principle of Secondary Current Generation in a Current Transformer

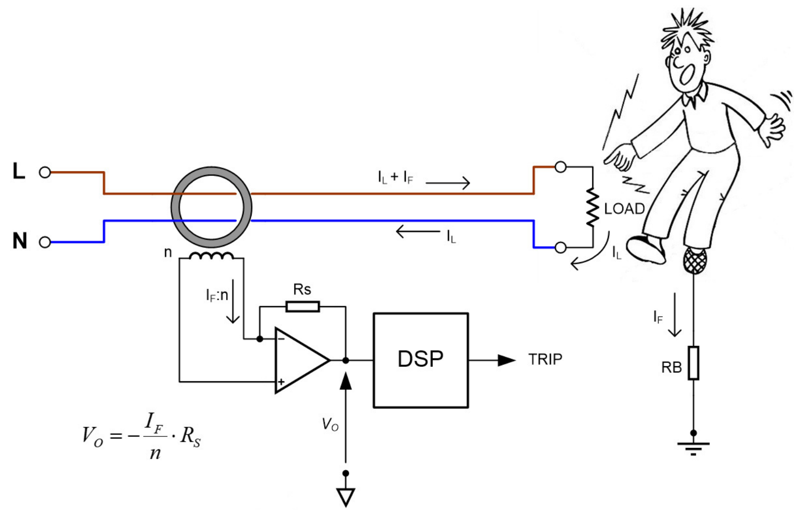

Figure 6. Simplified Diagram of the Ground Fault Detection

Under normal operating conditions, the current flowing through the Line and returning to Neutral are equal. As a result, the net current passing through the current transformer (CT) is zero, meaning no differential current (ground fault current) is detected.

However, when a ground fault occurs, such as when current leaks to the ground, the return current through the Neutral is no longer equal to the Line current. This creates an imbalance between the Line and Neutral currents.

Due to this imbalance, the current transformer (CT) generates a magnetic field proportional to the current. This magnetic field induces a secondary current in the CT according to its turns ratio. The sensing circuit detects this differential current, which indicates the presence of a ground fault. Thus, the CT plays a key role in identifying ground faults by converting the imbalance into a measurable signal, as illustrated in Figures 5 and 6.

To successfully detect ground fault current, the design of the current transformer (CT) is particularly important, especially regarding the selection of core materials and the number of turns. Permalloy is generally recommended as the core material for ground fault (GF) coils, with turns ratio between 800 and 1000 to accurately sense the ground fault current signal on the secondary side while CT is operating within the linear region of its B-H curve. Further characterization will be necessary in the final application. Additionally, a ferrite core is recommended for ground neutral (GN) coils, with turns ratio of 250.

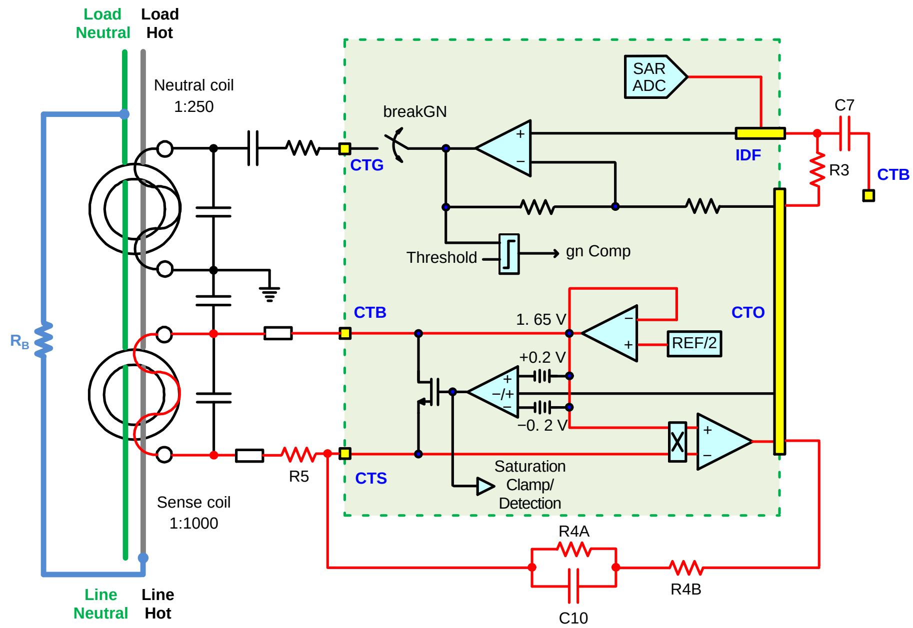

Figure 7. Ground Fault Detection Signal Paths Diagram

In the Figure 7, the ground fault current is detected with 1:1000 Sense coil in the similar method of conventional GFCI controllers. The NCS37021 detects the ground fault currents by secondary currents that is converted to the voltage variation on the CTO pin, and this CTO pin voltage is the input of the IDF pin that is used for ADC input. The secondary currents are produced by primary currents, ground fault currents with respect to turns ratio. In the system, the sensing accuracy of the CT is required to detect the ground fault currents within the range.

The Sense coil is DC biased approximately 1.65 V, which is the Mid-point of ADC input within total available dynamic range, which is from 0 V to 3.3 V. For example, if there are no ground fault currents, the CTB, CTS, CTO, and IDF pin are quiet, which is 1.65 V. To reduce the offset error, the chopping frequency is integrated in internal logic.

Once the NCS37021 detects the ground fault currents, the IDF pin voltage will fluctuate within the ADC dynamic range with respect to the ground fault currents frequency, 60 Hz. If the ground fault currents are over the trip threshold for >8.35 ms within AC mains period, the internal SCR driver logic enabled, then the SCR pin will be enabled to trip the GFCI device.

This ground fault trip threshold can be calculated as following equation:

$$I_{diff} = \frac{0.160 \times CT_1 \times \left(R_{CT1} + R5 + 2\pi f_{AC} \times L_{CT1}\right)}{R_{4A} \times \left(R_{CT1} + 2\pi f_{AC} \times L_{CT1}\right)} \qquad \text{(eq. 1)}$$

Where:

CT_1 is Turns ratio of differential CT

R_{CT1} is DC winding resistance of differential CT

f_{AC} is AC mains frequency

L_{CT1} is Inductance of differential CT

* Note that the equation above is for an ideal CT. In practice, the GF threshold can be ±20% different and should be empirically set. To ensure accuracy in CT performance, careful attention must be paid to the CT design. This includes selecting core materials, optimizing the number of turns, and ensuring consistent performance across corners. Achieving this level of precision may require collaboration with experienced CT manufacturers who have a proven track record in producing reliable components for RCD & GFCI applications.

In the NCS37021, the different levels of response time to enable the SCR driver logic based on the amount of the ground fault currents as follows:

6 mA to 15 mA ≤ 135 ms
15 mA to 30 mA ≤ 70 ms
over 30 mA ≤ 20 ms

If very high ground fault currents occur, the secondary side current produces large currents, which increase the voltage across the CT. And Internal logic is monitoring the voltage between the CTB and CTS pins. If it is greater than approximately 230 mV, and if this state remains greater than approximately 1.4 ms, the SCR driver logic will be immediately enabled.

The other external components including R4B, C10, R3, and C7 are incorporated to facilitate signal filtering and conditioning.

Ch1: IDF, Ch2: SCR, Ch3: MLD, Ch4: REF

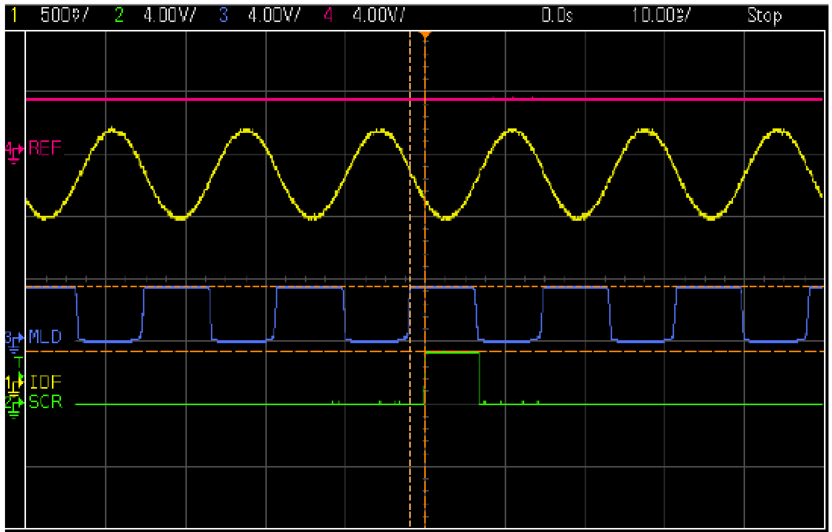

Figure 8. Ground Fault Detection Waveform

Principle of Grounded Neutral Fault Detection (UL 943 Requirement)

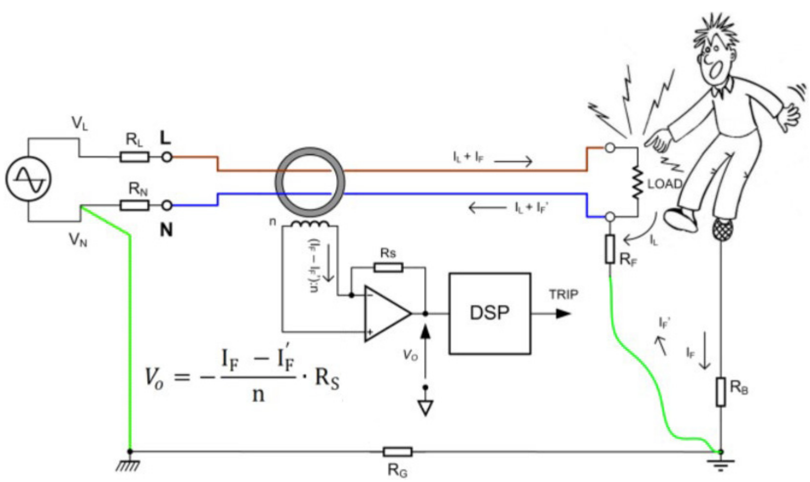

Figure 9. Simplified Diagram of the Grounded Neutral Fault Detection

To comply with UL 943 requirements, GFCI must detect grounded neutral faults. The grounded neutral fault will occur when the Neutral wire is unintentionally connected to the earth ground. This condition can disrupt the GFCI's ability to detect actual ground faults, potentially allowing dangerous leakage currents to go unnoticed and the GFCI differential detection circuitry will not see the fault and will not trip as intended.

To address this, UL 943 requires GFCI to include a grounded neutral detection circuit that enables it to trip if such a fault is present. This ensures that the GFCI cannot operate in an unsafe condition where it might fail to protect against electric shock.

This requirement enhances user safety by ensuring that the GFCI remains effective even when the Neutral is improperly connected to the earth ground in the application, as illustrated in Figure 9.

Understanding and Applying for Grounded Neutral Fault Detection Using NCS37021)

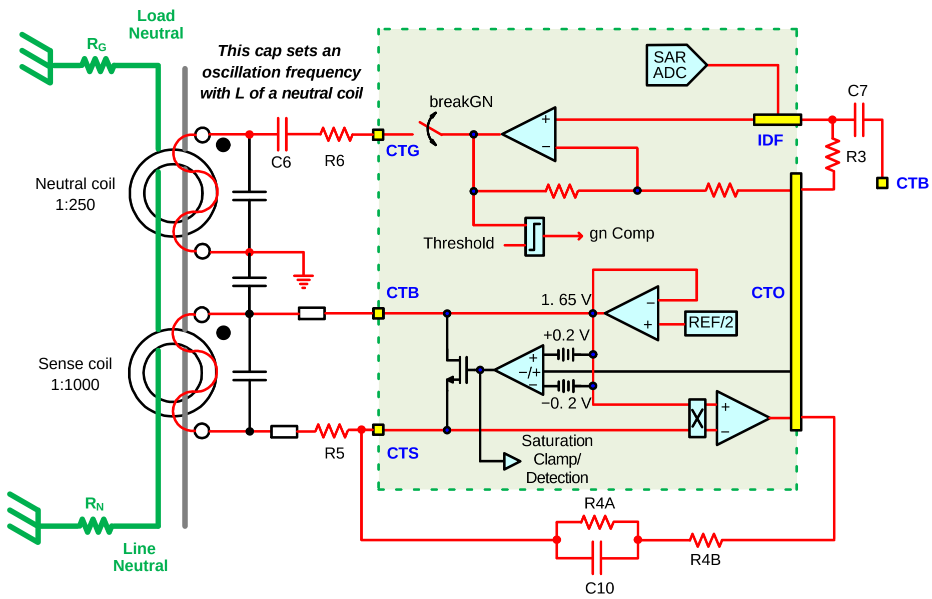

Figure 10. Grounded Neutral Fault Detection Signal Paths Diagram

The grounded neutral fault detection is also the same philosophy for conventional GFCI controllers. The grounded neutral fault detection is accomplished by the addition of the Neutral coil (GN coil) to generate “Dormant Oscillator” circuit. Once GN fault occurs in the loop, both Sense coil and Neutral coil are magnetically coupled, enabling energy transfer between the coils. This signal is processed within the IC through two amplifiers. To ensure stable oscillation, it is important that the loop gain is sufficiently high enough when the phase shift is 0 degrees.

For further support, please contact the **onsemi** team.

The sensitivity of the GN detection can be changed by C6 and R6. Also, to successfully detect the GN fault, this frequency needs to be between 2 kHz to 7 kHz. The GN oscillation frequency can be calculated by following equation:

$$f_{GN} = \frac{1}{2\pi\sqrt{L_{GN\ Coil} \times C_6}} \quad \text{(eq. 2)}$$

Where:

$L_{GN\ Coil}$ is Inductance of GN CT

The CTG pin voltage is continuously monitored to detect the GN fault by internal logic. When the GN oscillation frequency at the CTG pin occur and the voltage of this oscillation is above 1.95 V, the internal logic will be disabled the GN amplifier to break the loop, which will stop the oscillation at the CTG pin. During this time, if the oscillation is less than 1 kHz, this indicates the potential GN fault. Therefore, the GN amplifier will be enabled again. After three times of completing this cycle, the SCR driver logic will be enabled. This intelligent GN detection algorithm enables advanced sensing that differentiates between ground faults and true grounded neutral faults. By accurately distinguishing these scenarios, it reduces the risk of nuisance tripping, enhancing system reliability and operational stability. During the Power-Up, the GN amplifier will be powered down for the first approximately 70 ms.

Ch1: CTG, Ch2: SCR, Ch3: MLD, Ch4: REF

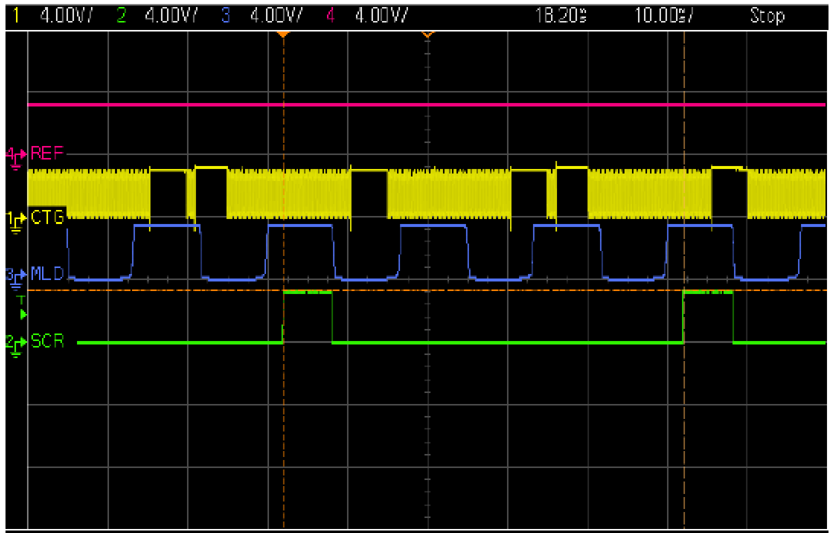

Figure 11. Grounded Neutral Fault Detection Waveform

Understanding the Functionality of Self-Test (ST)

In the NCS37021, the intelligent Self-Test (same as auto-monitoring) function is inbuilt with digital logic which allows the GFCI application to have the capability for compliance with UL 943 requirements.

In every ST cycle, the internal digital logic tests both the ability to respond the ground fault current testing and to monitor the switching semiconductor supplying the trip solenoid (SCR Self-Test).

When the device Power-Up, the first ST cycle will occur at 1 second after Power-Up. Once the first ST passes, the periodic ST will occur every 1 minute. During the ST cycle the GFT pin will be enabled at the positive MLD phase for approximately 16 ms and the CT current (set at 8 mA RMS, R8) will be verified for positive or negative MLD phase. During the next negative half cycle, at the beginning of the cycle the SCR's anode voltage will be pre-biased by the SCM pin to approximately 3.3 volts which will be verified by internal logic. The SCR will then be enabled and the SCR's anode voltage will be monitored by the SCM pin.

If the anode voltage goes below approximately 2.1 volts, the SCR will be disabled after at least 250 μs verification check and the ST logic will register a passing ST cycle. If a ST cycle fails due to a low GF detection, the LED blinking logic will be enabled. After a self-test failure, the testing frequency is accelerated to a faster interval 12 MLD. If seven consecutive ST cycles fail the SCR will be enabled. If a ST cycle passes before any of the 7 consecutive ST cycle counter, the ST logic will be reset, and a ST cycle will occur in 1 minute.

Ch1: SCM, Ch2: SCR, Ch3: MLD, Ch4: GFT

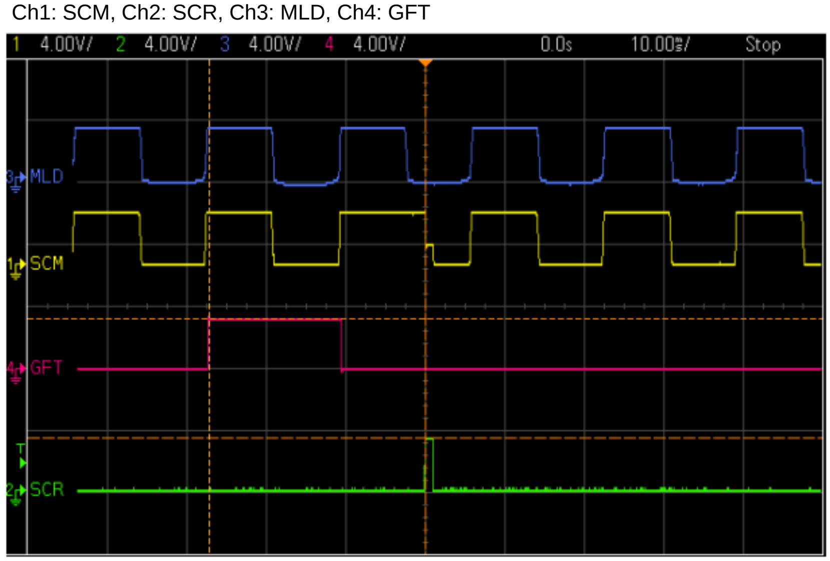

Figure 12. Self-Test Waveform at Steady State

Ch1: LED, Ch2: GFT, Ch3: SCR, Ch4: REF

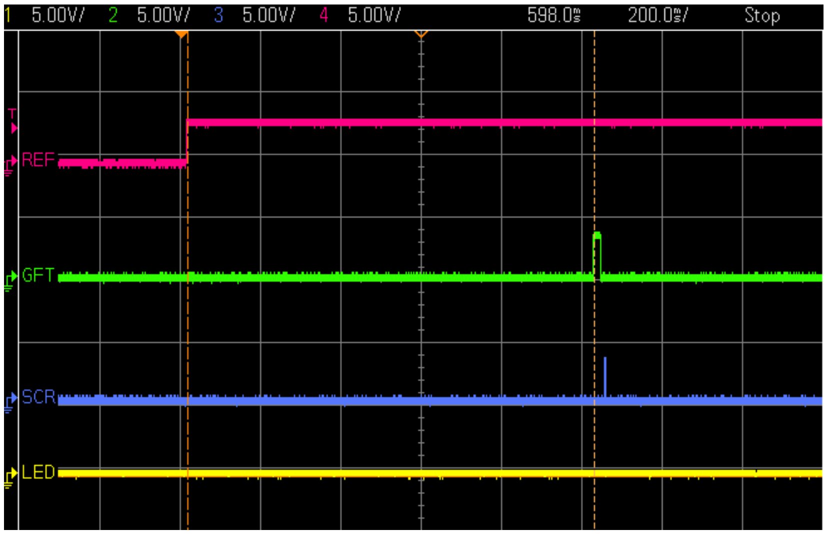

Figure 13. Self-Test Waveform at Power-Up − ST Occur in One Second

Understanding the Functionality of Push-To-Test (PTT)

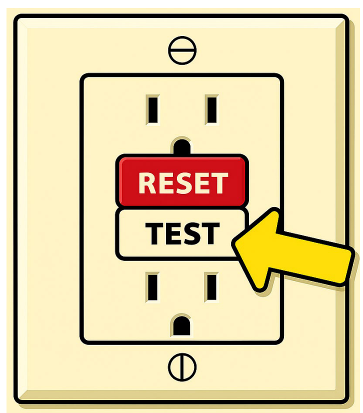

Figure 14. Typical Test Button Integration in GFCI Application

The Push-To-Test (PTT) is a function which does one-time self-test when it is pulled low. This feature can be utilizing as the features to do a “manual” test like one in a GFCI receptacles or breakers, that provides a benefit of not adding a wire into a CT to generate a fault currents.

When the PTT pin is enabled for greater than 16 ms a ST cycle will be enabled. During this ST cycle, the GFT pin goes high for one AC mains cycle to generate a ground fault current, which set by R8. If the ST cycle passes, the SCR will be enabled and the LED will blink once (for breakers, the LED can blink until power down). If the ST cycle fails, the LED will keep blinking, and SCR will not be fired. The PTT pin has an internal 50 kΩ pull up resistor. This pin is a CMOS input with hysteresis. To enable the PTT function, the input voltage should go below 1.2 volt.

Ch1: SCM, Ch2: SCR, Ch3: MLD, Ch4: PTT

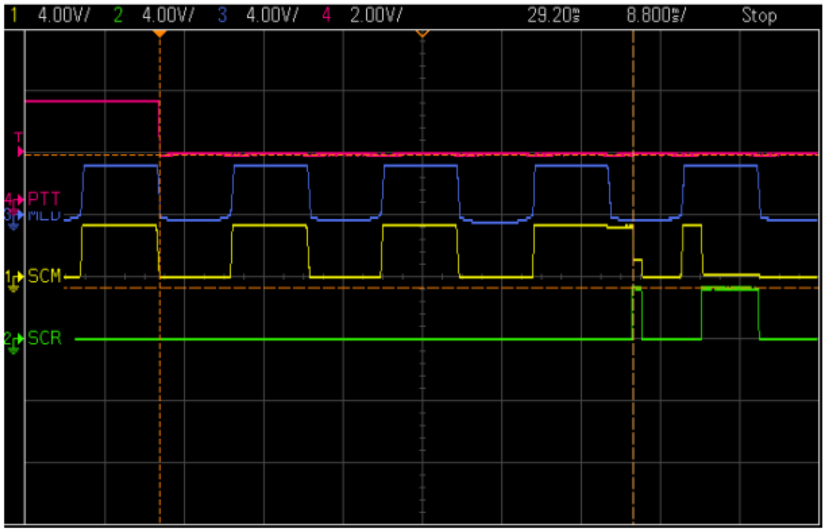

Figure 15. PTT Self-Test

Ch1: LED, Ch2: GFT, Ch3: MLD, Ch4: PTT

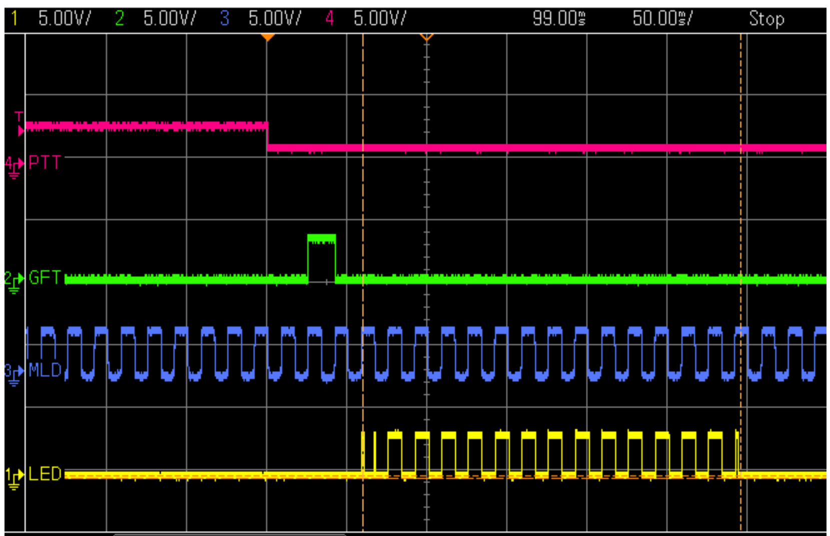

Figure 16. PTT Self Test and LED

REVISION HISTORY

Revision	Description of Changes	Date
0	Initial document version release.	9/18/2025

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales