Capacitive Load Charging in Zonal eFuses

AND90379/D

Introduction and Scope

The introduction to power distribution in a zonal architecture, and its advantages and challenges have been presented in detail in the applications note AND90348/D – Smart Power Distribution in Zonal Architecture. Further, the note also highlighted power switches/eFuses as a key component of zonal architecture and described the key standout features desired in these switches that specifically relate to their operation in zonal systems. This application note provides details on one of those feature sets – namely, capacitive load charging capability. The sections below will present the requirement for a dedicated mode to charge capacitive loads and will compare different design implementations towards that end. The design methodology in **onsemi** eFuses as well as impact of application set up on device performance will also be discussed together with corroborating bench measurement results. Discussion on other smart switch/eFuse features besides capacitive charging is outside the scope of this document and respective application notes should be referred for any details on those features.

Capacitive Load (CL) Mode

Application Use Cases

In conventional domain applications, inrush requiring loads as observed by SmartFETs primarily constitute lighting (incandescent filament bulbs, or LED clusters), heating (such as seat heaters, airbag squibs etc.), power window and HVAC fan motors, audio systems with amplifiers as well as ADAS units. Since most of these applications require a sudden surge of power at startup – such as to heat the filament in a bulb, or to overcome the motor inertia, a capacitor in parallel with the load can help stabilize the output voltage of the high side switch in case of load transients. With the advent of zonal architecture, where Smart Switches replace mechanical fuses, several electronic control units and sub-modules in the zonal cluster would be required to be supplied via these switches. Most of these control units/modules, including those operating in key-off mode, have a bulk or a reserve capacitor at their input to reduce supply interruptions and to keep the modules powered during high current transients and supply loss/drop. The capacitor values can range from a few 10's of μF's to a few mF's. Since these capacitors are required to be charged via smart switches/eFuses, capacitive load charging becomes a central aspect of eFuses in a zonal architecture. The figure below depicts different topologies in which such capacitive loads are being driven in the zonal application. **onsemi**'s portfolio of high-side Smart Switches/eFuses targeting zonal applications have an integrated capacitive load mode to enable the charging of these bulk capacitors.

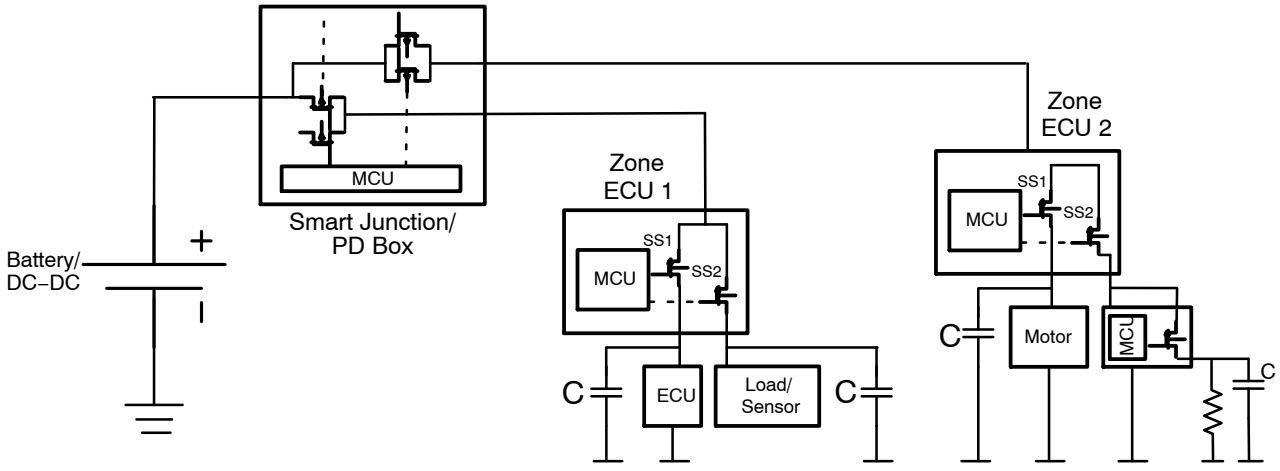

Figure 1. Capacitive Loads in Zonal Architecture

Key Design Considerations

When addressing capacitive load charging, several design implications need to be considered. Some of these include the maximum allowed current in the application, the desired time to charge the capacitive load, the available supply voltage, the output cable impedance, and finally the power dissipation across the output stage of the switching IC. Further, the overall system cost, PCB area consumption and overheads also need to be considered in designing a solution to charge capacitive loads. Very often, there are trade-offs when attempting to optimize each aspect as will be described below.

Managing Peak Inrush Current

The primary challenge when powering capacitive loads is to manage the inrush requirement of the load. Depending on the value of capacitor and external conditions, the current during inrush phase can reach fairly high levels, in some cases, even triggering the internal overcurrent detection threshold causing the device to shut down as will be explained. Since a fuse replacement Smart Switch is expected to latch-off the output stage in case of overcurrent detection (due to the possibility of a short circuit), the absence of a retry strategy post shutdown can prevent the capacitor from getting charged. Further, since many of such e-fuses will have multiple loads connected to their output, activation of internal over-current protection followed by a shutdown of the output stage can cause unexpected transients, or complete loss of power in different "load-legs". Even if the over-current detection shutdown is not invoked, extremely high currents during inrush may potentially damage the PCB traces, or harness connectors. In case of such repetitive capacitive load turn-on events, the transient thermal overstress inflicted on the device can potentially compromise its lifetime and long-term reliability.

Figure 2 below depicts such inrush profiles under two use-cases while charging a 3.9 mF capacitive load to 13.5 V with NCV84003G without using the integrated capacitive charging mode. In Figure 2(a), the overcurrent detection threshold was configured to reduce the peak current observed in the application (Refer to product data sheet for details on overcurrent threshold adjustment). The inrush at turn-on resulted in device shutting down the output stage without completely energizing the load. In the second case, where the internal overcurrent shutdown is set to default, even though the capacitive load is fully charged, the load levels can reach close to 100 A or even higher (depending on external conditions) during inrush. This response is depicted in Figure 2(b).

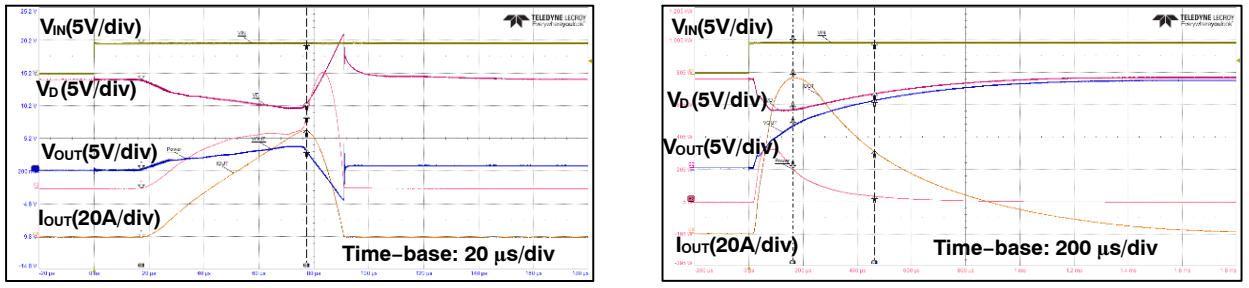

Figure 2. Capacitive Load Inrush Profile Examples With a) Reduced Overcurrent Detection b) Default Overcurrent Detection

Avoiding Supply Voltage Drops

In addition to the thermal overstress observed by the die (as explained above), a huge spike in output current can also lead to the supply voltage dropping, thereby making it challenging for the device to operate, especially during cold cranking conditions. A typical 14 gage harness, as an example, can add up to 10 mΩ line resistance per meter, which excludes any output impedance that the supply or DC/DC regulator can exhibit. Depending on cable length, the available voltage at the input supply of the Smart Switch can drop by 1~2 V at peak current levels of ~100A or more. At low starting battery voltages, this drop can be sufficient to affect the parametric performance of the device – such as internal bandgaps and references, overcurrent trip thresholds, current sense output etc. Prolonged drops in the supply voltage can also cause longer supply recovery times, thereby delaying the charge build-up in the capacitor. In addition, since the same supply is powering other loads in the application, a reduction in supply voltage during inrush could also imply a compromised performance or even loss of functionality (in cases of under-voltage shutdown) served by those other loads. The situation is exacerbated especially while operating at low battery voltages (such as inrush during cold cranking) to begin with. It is, therefore, imperative to limit these high current excursions during the inrush phase of the capacitive charging.

Soft-Start Implementation

The general guiding principle of reducing high current excursions during inrush phase can be implemented through various design approaches. The most intuitive of these approaches is output ramp slew rate reduction. The switching IC uses active circuitry deploying current sources to charge and discharge the gate of the output stage. The rate at which the gate charge accumulates or dissipates consequently sets the output voltage slew rates. Such active regulation of the output slew rate control is necessary for SmartFETs not just to improve the EMC performance of the system but also allow a "soft-start" in applications that have specific inrush requirements. The load dependent dynamic slew rate adjustment in NCV84003G is presented in examples below where the increase in load current from 5 A (Figure 3(a)) to 40 A (Figure 3(b)) causes a dynamic reduction in turn on profile and slew rate while charging the output voltage to 13.5 V.

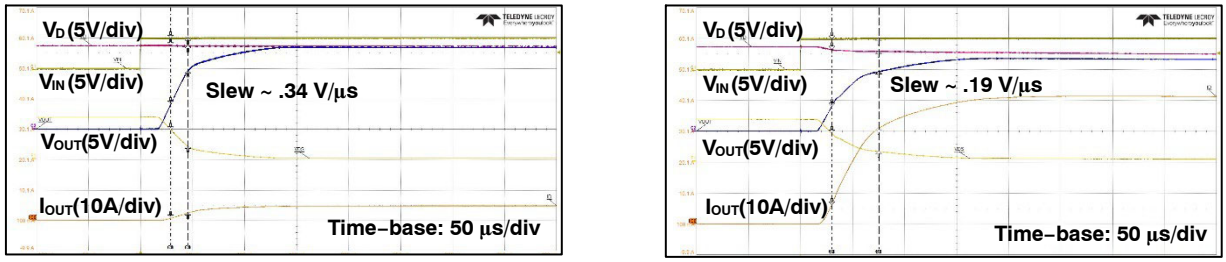

Figure 3. Active Slew Control Mechanism in NCV84003G at a) I_{OUT} = 5 A and b) I_{OUT} = 40 A

The described approach can be furthered by "folding back" on the base slew rate while charging capacitive loads in addition to the load dependent slew rate adjustment. Such a reduction in output slew rate in the form of a dedicated capacitive charging mode allows a gradual turn on of the Smart Switch output voltage. A slower dv/dt at the output node, in turn, limits the inrush current with the relationship described below:

I = C*dv/dt, where C is the known fixed capacitor to be charged, I is the current during inrush and dv/dt is the slew rate of the voltage that the capacitor is required to be charged to.

The waveforms below depict a 220 µF capacitive load being charged to 13.5 V with two different slew rates. The output ramp in the waveform to the right is about 10x slower than that on the left waveform. The inrush profile with a reduced slew exhibits lower current excursions and the consequent drop in supply voltage is also low.

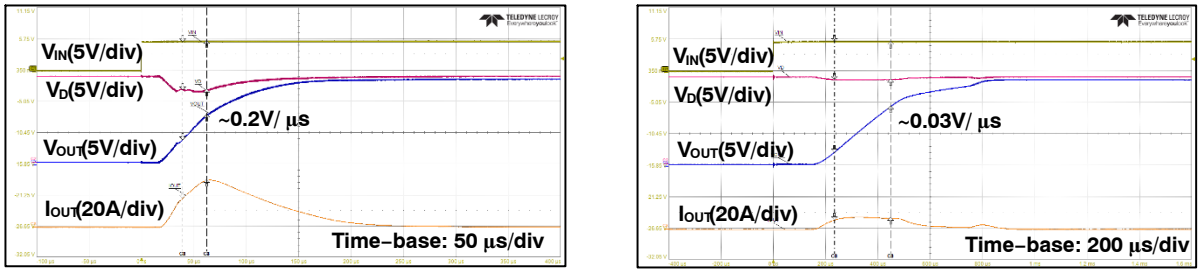

Figure 4. Capacitive Load Turn on Profiles Under a) Normal b) Reduced Slew Rates

However, it also takes longer to charge to a given output voltage leading to longer capacitive charging times and higher energy dissipated across the switching device. The switching losses and the energy delivered to the load for the two cases are presented in the waveforms below. While the load power dissipation is reduced by limiting the inrush current, the switching device clearly dissipates twice as much energy by reducing the output slew rates.

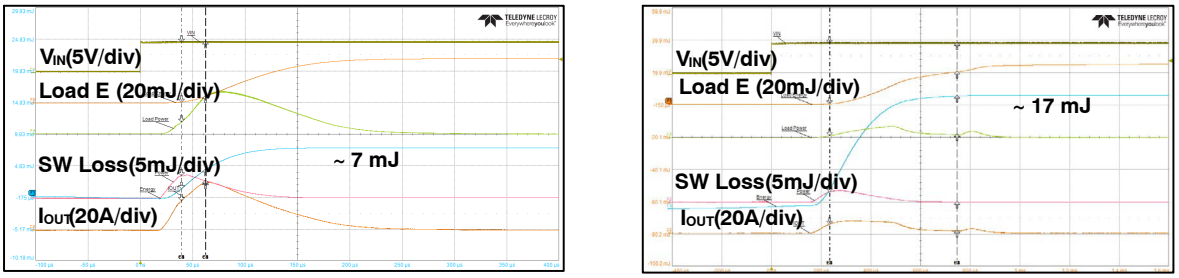

Figure 5. Switching Energy Losses in Capacitive Load Turn on Profiles Under a) Normal b) Reduced Slew Rates

onsemi offers eFuse devices such as NCV84003G, that have integrated slew rate reduction in capacitive charge mode, as well as devices such as NIV3071, that employ an external capacitor for the user to set the slew rate corresponding to the desired inrush current and turn-on time requirements. The applications note AND90247/D – The NIV3071 eFuse Advantages in Automotive Applications describes the details of external capacitor based slew rate reduction for capacitive charging. This slew rate control capacitor modulates the charge at the gate of the output stage, thereby allowing the external control of gate voltage and consequently the output voltage ramp. Since this pin directly interfaces with the performance of the power stage, any noise or parasitic impedance at this pin (due to PCB trace resistance, or peripheral components in the system) can influence the gate drive and this sensitivity, therefore, must be considered while designing the application for a given slew rate control. Refer to respective product datasheets for the specific slew rate adjustment implementation.

In-Rush Management Considerations-Avoiding Over-heating

While advantageous in powering on capacitive load to the order of a few 100's of µF's, the power dissipation and the resulting die temperature gradients across the switching device can rise to significantly higher levels when attempting to charge bigger capacitive loads. Further, if a short circuit condition is present during capacitive charging mode, it may inflict a higher thermal gradient on the die and overstress the device, potentially also invoking a differential/absolute over-temperature shutdown of the output stage (Refer to applications note High-Side SmartFETs with AND9733/D – Analog Current Sense for details on over-temperature shutdown mechanisms). Below is an example of a short circuit applied to a 3 mΩ switch that is being driven at reduced slew rates in the absence of a dedicated thermal shutdown scheme specific to reducing losses in CL mode. The power losses depicted in the waveform can cause a thermal gradient of more than 60 °C. To circumvent this, **onsemi** Smart Switches offering capacitive charge mode have the differential over-temperature shutdown protection specially configured for this mode of operation as will be described later in this note.

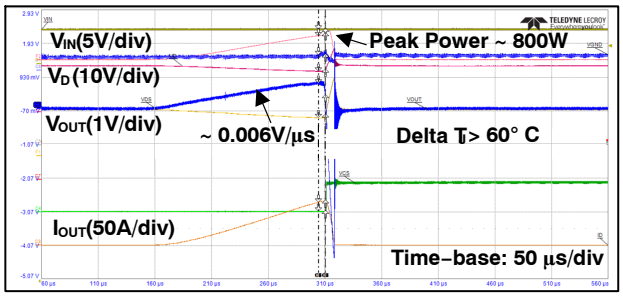

Figure 6. Thermal Gradient in a Short Circuit Condition With Reduced Slew Rate

Current Regulation vs Device SOA

Another approach to limit the peak current during inrush phase is to implement an internal current limit that will regulate the output stage at a constant current level once the load current reaches the defined threshold. This current limitation scheme, however, requires the device to regulate the output FET in linear region of operation over extended intervals (10's of milliseconds while charging capacitive load to the order of mF's) that could potentially infringe with the Safe Operating Area (SOA) of high density DMOS power FETs integrated in smart switches.

Once again referring to the current-time relationship of the capacitor, the load current required to charge the capacitor in a desired time can be calculated as: I = C*V/t. For a 5 mF capacitive load to be charged to 13.5 V typically using a 3~4 mΩ (nominal RON) power FET, the relationship is derived as I = 67.5/t, where t is inrush duration in milliseconds. For most applications, the window for maximum allowed inrush time is between 20~50 ms at startup. The consequent inrush current, therefore, can be calculated as 1~4 A. The SOA characteristic curve for a typical 4 mΩ power FET (NVTFWS4D9N04XM) is presented below in Figure 7(a). Considering (conservatively) a linear output voltage ramp from 0 to 13.5 V, the average output voltage during inrush phase can be roughly estimated as ~7 V. It can be noticed that for pulse durations of 10 ms, a 7 V average drop yields a current level slightly greater than ~4 A (as highlighted) and any longer pulse duration at 4 A (as desired in this particular capacitive charging example) would imply a possible infringement with the SOA curve. In case of smart switches or eFuses, this would imply that the integrated protection mechanism (power/temp limitation in this case) would trigger to allow sufficient margin below the output FET SOA and thereby, would interrupt capacitive charging. As an alternative, the regulated current during inrush can be reduced to prevent engaging the protection mechanism. Both these alternatives, although, would result in inrush times longer than the desired levels as discussed above.

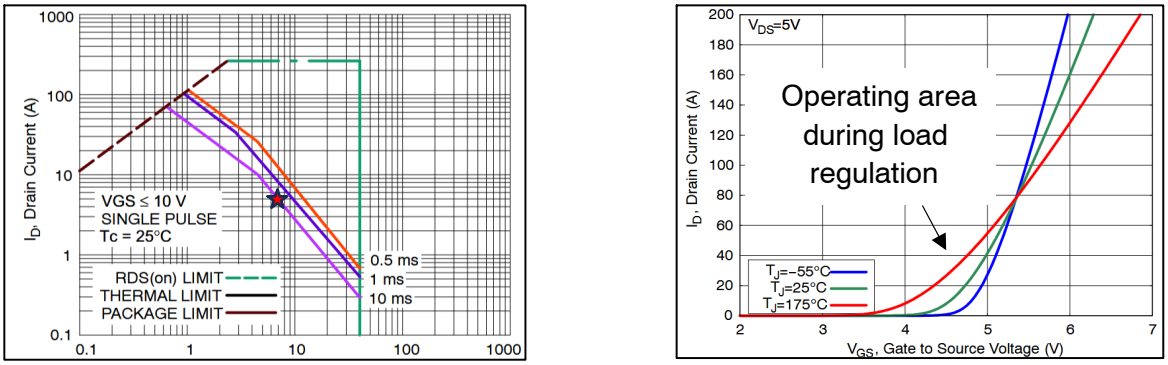

Figure 7. a) SOA and b) Transfer Characteristics of NVTFWS4D9N04XM

In addition to SOA concerns, operating the FET in linear mode over extended intervals introduces stability concerns and chances of hotspotting in high density FETs as the natural advantage of a negative temp-coefficient is lost in this region. Therefore, current regulation, while a feasible option can pose operating challenges as explained above.

Some applications, particularly, high voltage EV applications, employ a separate pre-charge path with a resistor to limit inrush during capacitive charging. Implementing such a design, however, would likely ensue an increase in PCB area and the overall system cost by adding more components (including the pre-charge switch, driver, resistor and any other associated fail-safe circuit) the BOM.

onsemi *Approach – Capacitive Load Mode*

Considering all the aspects discussed above, the capacitive load mode offered in **onsemi** smart switches integrates a) active slew rate control mechanism, b) foldback of the differential over-temperature shutdown, and c) auto-retry strategy for inrush management. The benefits of slew reduction in the form of inrush limitation have already been discussed in this document before. The increased power and thermal losses associated with a reduced slew (Refer to Figure 6) are prevented with the a help of a folded-back differential over-temperature shutdown. The dynamic temperature gradient in capacitive load mode is restricted to 30 °C instead of the nominal 80 °C that is designed for normal operating mode. The waveform in Figure 7, as measured on NCV84003G, depicts turning into a short circuit load – the worst case condition while operating in capacitive load mode. Comparing the performance to Figure 6, it can be observed that both the power loss and the temperature gradient across the switching device are reduced by more than half. Further, the folded DTSD threshold helps limit the peak current levels observed in this mode.

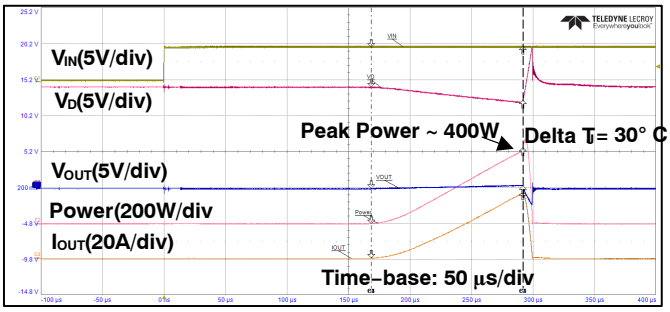

Figure 8. NCV84003G Short Circuit in Capacitive Load Mode

Now, at the switch-on of the output stage, the gate-source voltage is gradually ramped up implying that the device is operated in linear region during the load profile in Figure 7. However, limiting the pulse duration with a reduced DTSD threshold allows a greater margin below the SOA performance curve even though average current levels are elevated as compared to the current regulation approach described above. By curtailing extended operation in linear mode, the concerns with regards to instability and hotspot formation are also alleviated.

The final aspect of the capacitive load mode is the retry strategy. Even though the reduced DTSD threshold helps limit losses, the trade-off is the time to energize the capacitive load. The auto-retry strategy in capacitive load mode allows the output stage to be turned on again without any stimulus required from the microcontroller. The "cool-down" time between successive retries is designed to ensure that the FET does not accrue heat or run into SOA concerns over repetitive retries while allowing the capacitive load to be charged in reasonable time. The measurements below represent once again the 3.9 mF load capacitor, being charged by NCV84003G with the dedicated capacitive load mode. Observing the zoomed in picture of the individual pulse on the right, it can be noticed that the reduced slew rate helps limit the load current during inrush phase as compared to that in Figure 2, thereby allaying the safety concerns pertaining to PCB and harness connectors. The resulting drop in supply voltage is also reduced in comparison to Figure 2. The folded back DTSD limits the power dissipation across the die (as discussed above), and the auto-retry strategy allows a fast charge-up of the capacitive load (~10 ms for this example).

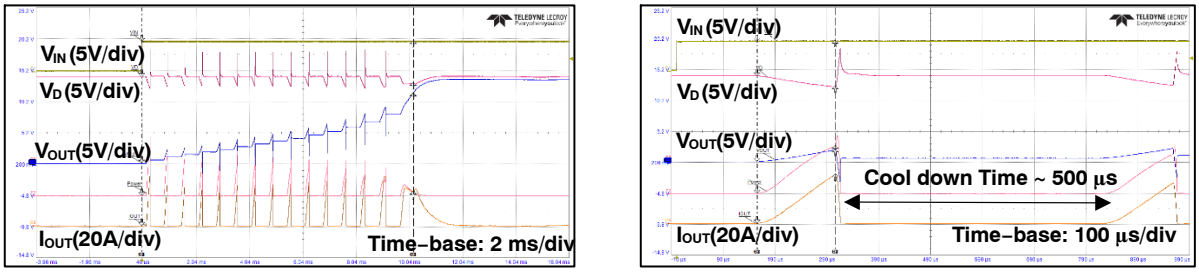

Figure 9. NCV84003G Switching on 3.9 mF Capacitive Load

Once the output voltage is "sufficiently" charged to within a defined threshold of supply voltage, the device automatically exits capacitive load mode to normal mode of operation as highlighted in the waveform above. It should also be noted that the maximum time in capacitive load mode at switch-on is internally limited by a timer (Refer product data sheet) to prevent repetitive output retries in case of a short circuit or over-sized capacitive load. In such a scenario, once the timer expires, the device exits capacitive load mode and protection circuitry as well as retry strategy defaults to normal mode. If the short circuit is still detected after this exit, then the over-current and/or over-temperature protection may engage and shut down the output of the eFuse while indicating corresponding diagnostic feedback at the same time.

With regards to initializing the capacitive load mode, the direct drive zonal smart switches offered by **onsemi** provide an auto-entry into capacitive load mode at switch-on from sleep together with options for overriding logic if such an entry is not desired. The devices with SPI communication can provide the microcontroller with specific configuration request registers to enable/disable the capacitive load mode. For details on parametric specification and entry/exit criteria, specific product data sheets should be referred to.

Additional Considerations

Finally, the external setup conditions and parasitics also determine various aspects of capacitive load charge characteristics. For instance, the ESR of the capacitive load can change across temperature, thereby affecting the charge time. The two waveforms below depict NCV84003G charging a 3.9 mF capacitive load at 25 °C and 85 °C ambient temperatures respectively. A change in the impedance presented by the capacitor (including dielectric properties and ESR) at high temperature leads to a longer charge time in this case. The load connected with the capacitor will also impact the capacitive charging time. A low impedance load, for instance, will “load the capacitor” and cause longer capacitive charging time. A very high impedance load, on the other hand, can delay capacitive discharge time potentially causing an open load detection. Further, any cable inductance in the setup can cause drain and output voltages to overshoot with inductive flyback as the output stage is shut down repetitively during capacitive charge retries. The device is designed to absorb the energy dissipated during such V_{DS} overshoots. **onsemi** can assist in providing the capacitive turn on data for loads under defined application conditions based on specific requests.

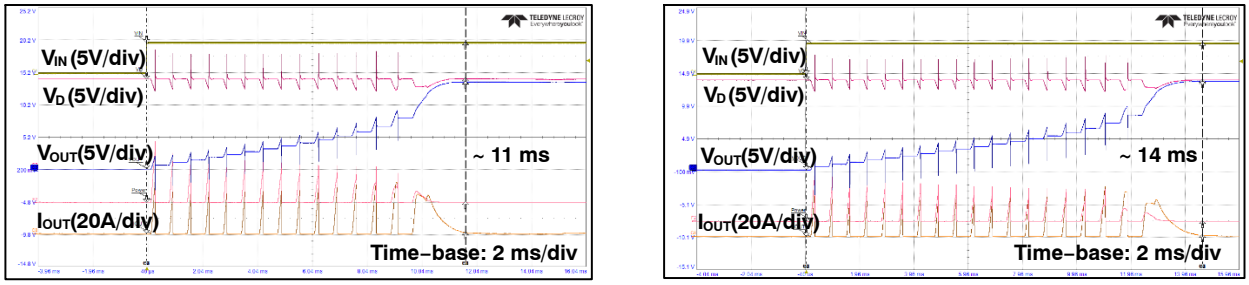

Figure 10. NCV84003G Switching on 3.9 mF Capacitive Load at a) 25 °C and b) 85 °C

REVISION HISTORY

Revision	Description of Changes	Date
0	Initial document version release.	08/20/2025

ADDITIONAL INFORMATION

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