3-phase Inverter Power Module 1200 V SPM® 3 Version 2 Series Application Note

AND90356/D

INTRODUCTION

This application note provides practical guidelines for designing with the SPM 3 version 2 Series power modules.

This series of Intelligent Power Modules (IPM) for 3-phase motor drives contains a three-phase inverter stage, gate drivers.

Design Concept

The SPM 3 version 2 design objective is to provide a minimized package and a low power consumption module with improved reliability. It is achieved by applying new gate-driving High-Voltage Integrated Circuit (HVIC), a new Insulated-Gate Bipolar Transistor (IGBT) of advanced silicon technology and improved Direct Bonded Copper (DBC) substrate based on transfer mold package. The SPM 3 version 2 achieves reduced board size and improved reliability compared to existing discrete solutions. Target applications are inverter motor drives for industrial use, such as commercial air conditioners, general-purpose inverters and servo motors. The temperature sensing function of SPM 3 version 2 products are implemented in the LVIC to enhance the system reliability. The analog voltage proportional to the temperature of the LVIC in module is provided for monitoring the module temperature and necessary protections against over-temperature situations. Figure 1 shows the package outline structure.

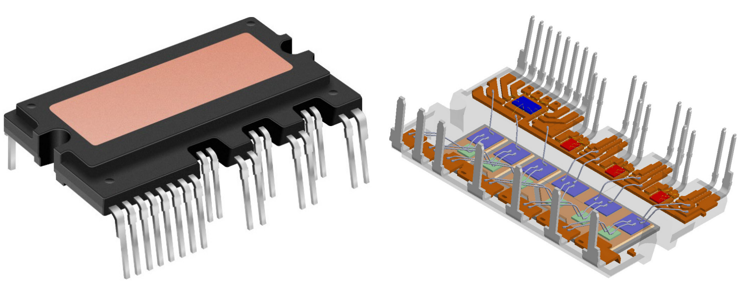
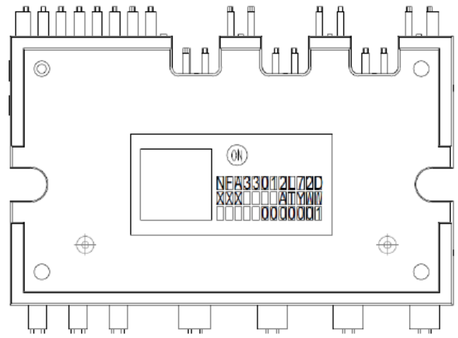


Figure 1. External View and Internal Structure of SPM 3 Version 2

MARKING DIAGRAM



NFA33012L72D = Specific Device Code
XXX = Last 3 Digits of Lot No
YWW = Year and Work Week Code
0000001 = Serial Number

ORDERING INFORMATION

Device	Package	Shipping
NFA33012L72D	SPM27-CA	10 Units / Tube

Key Features

- 1200 V / 15, 25, 30 A, Three Phase FS7 IGBT Inverter Including Control ICs for Gate Driving and Protections
- Very Low Thermal Resistance by Adopting DBC Substrate
- Easy PCB Layout Due to Built-in Bootstrap Circuits
- Open Emitter Configuration for Easy Monitoring of Each Phase Current Sensing
- Single-grounded Power Supply Due to Built-in HVICs
- Built-in Temperature Sensing Function by LVIC
- Isolation Rating of 2500 Vrms / Min.

PRODUCT DESCRIPTION

Ordering information

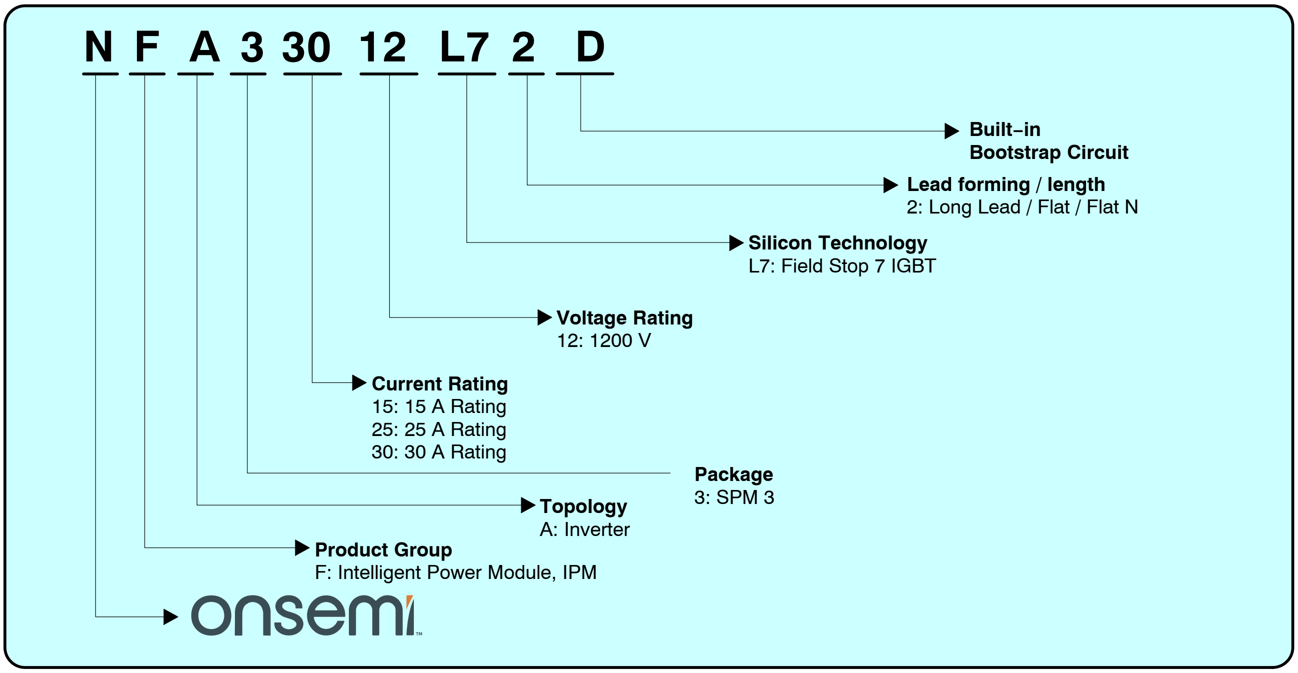


Figure 2. Ordering Information

Product Line-up

Table 1 shows the SPM3 version 2 product line up without package variations. Online simulation tool, Motion Control Design Tool (Click for simulation tool). is recommended to find out the right product for the desired application. For package drawing, please refer to the Package Outline section.

Table 1. PRODUCT LINE-UP

Product	Current/Voltage	Recommend Power (Note 1)	Target Application	Isolation Voltage
NFA31512L72D	15 A / 1200 V	2.0 kW	Air Conditioners, Industrial motors, General-purpose inverters, Servo motors	V_{ISO} = 2500 V_{RMS} (Sine 60 Hz, 1-min All Shorted Pins Heat Sink)
NFA32512L72D	25 A / 1200 V	3.5 kW		
NFA33012L72D	30 A / 1200 V	4.5 kW		

1. These power ratings are simulated result by specific operating conditions, so it can be changed by the operating conditions.

Internal Circuit Diagram

Three bootstrap circuits generate the voltage needed for driving the high-side IGBTs. The bootstrap diodes are internal part in HVIC and driving voltage of high-side IGBTs is sourced from VDD (15 V) through bootstrap circuits. There is an internal level shift circuit for the high-side drive signals allowing all control signals to be driven directly from GND levels common with the control circuit such as the microcontroller without requiring external isolation with opto-couplers. LVIC temperature sensing signal is output from the VTS pin.

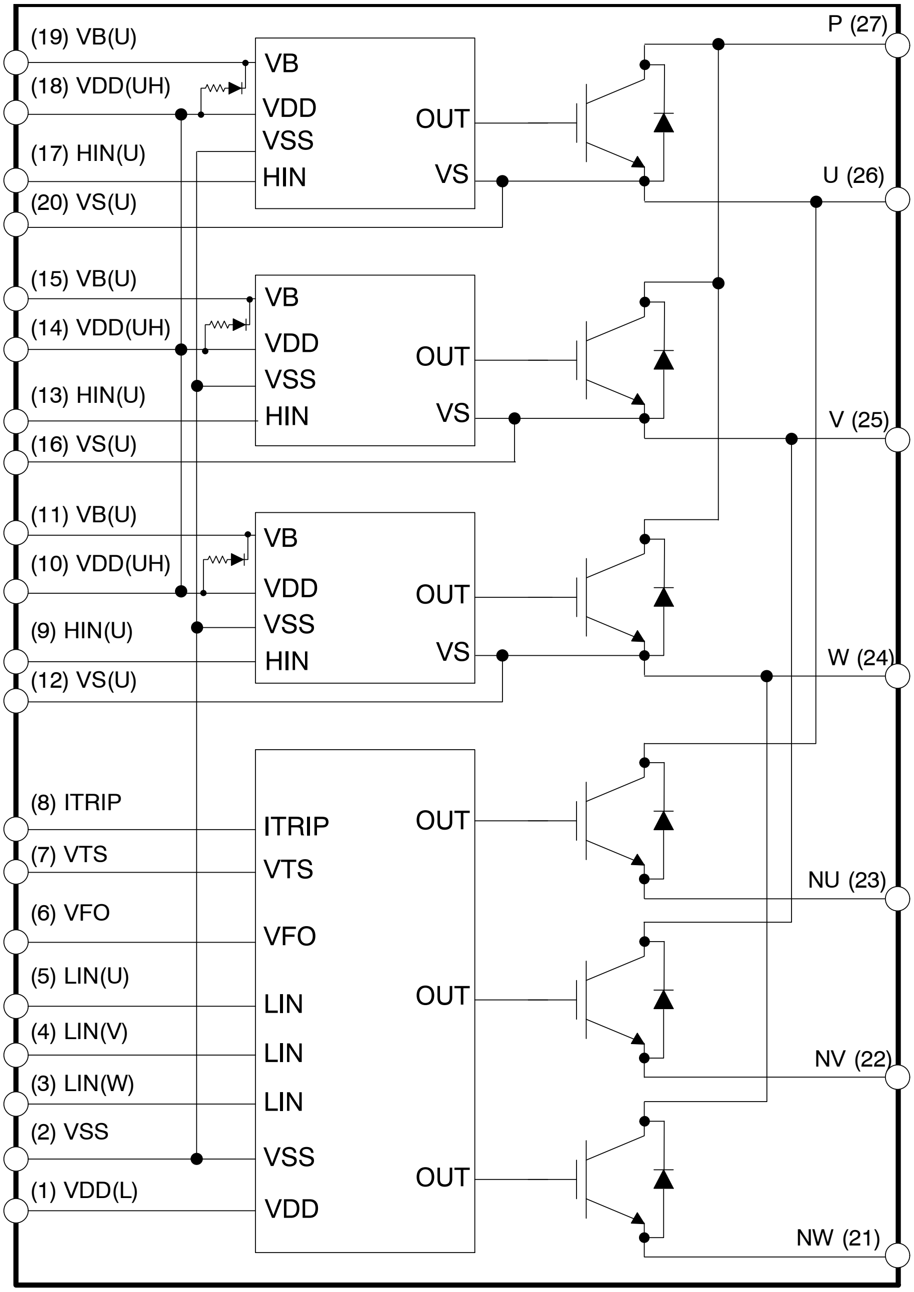


Figure 3. Internal Equivalent Circuit Diagram

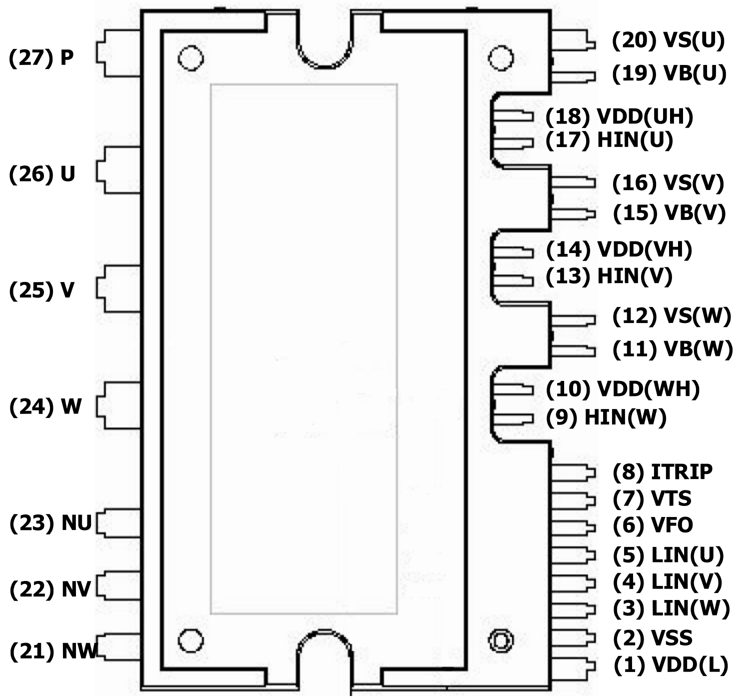


Figure 4. Package Top-View and Pin Assignment

Table 2. NUMBERS, NAMES AND DUMMY PINS

Pin Number	Name	Description
1	VDD(L)	Low-Side Bias Voltage for IC and IGBTs Driving
2	VSS	Low-Side Common Supply Ground
3	LIN(W)	Signal Input for Low-Side W-Phase
4	LIN(V)	Signal Input for Low-Side V-Phase
5	LIN(U)	Signal Input for Low-Side U-Phase
6	VFO	Fault Output
7	VTS	Output for LVIC Temperature Sensing Voltage Output
8	ITRIP	Input for Over Current Protection
9	HIN(W)	Signal Input for High-Side W-Phase
10	VDD(WH)	High-Side Bias Voltage for W-Phase IC
11	VB(W)	High-Side Bias Voltage for W-Phase IGBT Driving
12	VS(W)	High-Side Bias Voltage Ground for W-Phase IGBT Driving
13	HIN(V)	Signal Input for High-Side V-Phase
14	VDD(VH)	High-Side Bias Voltage for V-Phase IC
15	VB(V)	High-Side Bias Voltage for V-Phase IGBT Driving
16	VS(V)	High-Side Bias Voltage Ground for V-Phase IGBT Driving
17	HIN(U)	Signal Input for High-Side U-Phase
18	VDD(UH)	High-Side Bias Voltage for U-Phase IC
19	VB(U)	High-Side Bias Voltage for U-Phase IGBT Driving
20	VS(U)	High-Side Bias Voltage Ground for U-Phase IGBT Driving
21	NW	Negative DC-Link Input for W-Phase
22	NV	Negative DC-Link Input for V-Phase

Table 2. NUMBERS, NAMES AND DUMMY PINS (continued)

Pin Number	Name	Description
23	NU	Negative DC-Link Input for U-Phase
24	W	Output for W-Phase
25	V	Output for V-Phase
26	U	Output for U-Phase
27	P	Positive DC-Link Input

Detailed Pin Definition and Notification

Pins: VB(U) − VS(U), VB(V) − VS(V), VB(W) − VS(W)

- High-side bias voltage pins for driving the IGBTs and high-side bias voltage ground pins for driving the IGBTs.
- VB(U), VB(V), VB(W) pins are connected to cathode pins of bootstrap diodes on each phase.
- These are drive power supply pins for providing gate drive power to the high-side IGBTs.
- The virtue of the ability to bootstrap the circuit scheme is that no external power supplies are required for the high-side IGBTs.
- Each bootstrap capacitor is charged from the VDD supply during ON state of the corresponding low-side IGBTs and Diodes.
- To prevent malfunctions caused by noise and ripple in the supply voltage, a good quality (low-ESR, low-ESL) filter capacitor should be mounted very close to these pins.

Pins: VDD(L), VDD(UH), VDD(VH), VDD(WH)

- Low-side and high-side bias voltage pins.
- These are control supply pins for the built-in ICs.
- These four pins should be connected externally.
- To prevent malfunctions caused by noise and ripple in the supply voltage, a good quality (low-ESR, low-ESL) filter capacitor should be mounted very close to these pins.

Pin: VSS

- Common supply ground pin.
- This is supply ground pin for the built-in ICs.
- Important! To avoid noise influences, the main power circuit current should not be allowed to blow through this pin.

Pins: HIN(U/V/W), LIN(U/V/W)

- Signal input pins.
- These pins control the operation of the built-in IGBTs.
- They are activated by voltage input signals. The terminals are internally connected to a Schmitt-trigger circuit composed of 5 V-class CMOS.
- The signal logic of these pins is active high. The IGBT associated with each of these pins is turned ON when a sufficient logic voltage is applied to these pins.
- The wiring of each input should be as short as possible to protect the SPM 3 version 2 products against noise influences.
- To prevent signal oscillations, an RC coupling as illustrated in Figure 26 is recommended.

Pin: ITRIP

- Over-current and short-circuit detection input pin.
- The current sensing shunt resistor should be connected between the low-pass filter before the ITRIP pin and the low-side ground pin VSS to detect over or short circuit current.
- The shunt resistor should be selected to meet the detection levels matched for the specific application.
- An RC filter should be connected to the ITRIP pin to eliminate noise.
- The connection length between the shunt resistor and ITRIP pin should be minimized.

Pin: VFO

- Fault output pin.
- This is the fault output alarm pin. An active low output is given on this pin for a fault state condition in the SPM 3 version 2 products.
- The alarm conditions are Over-Current Protection (OCP), or low-side bias Under-Voltage
- Lock Out (UVLO) operation.
- The VFO output is open drain configured. The VFO signal line should be pulled up to the 5 V logic power supply with approximately 4.7 kΩ resistance.

Pin: VTS

- Analog temperature sensing output pin.
- This is to indicate the temperature of LVIC with analog voltage. LVIC itself creates some power loss, but mainly heat generated from the IGBTs will increase the temperature of the LVIC.
- VTS versus temperature characteristics is illustrated in Figure 14.

Pin: P

- Positive DC-link pin.
- This is the DC-link positive power supply pin of the inverter.
- It is internally connected to the collectors of the high-side IGBTs.
- To suppress surge voltage caused by the DC-link wiring or PCB pattern inductance, connect a smoothing filter capacitor close to this pin (tip: metal film capacitor is typically used).

Pins: NU, NV, NW

- Negative DC-link pins.
- These are the DC-link negative power supply pins (power ground) of the inverter.
- These pins are connected to the low-side IGBT emitters of each phase.
- These pins are used to connect one shunt resistor or three shunt resistors for current sensing.

Pins: U, V, W

- Inverter power output pins.
- Inverter output pins for connecting to the inverter load (e.g. motor).

PACKAGE

Package Structure

Since heat dissipation is an important factor limiting the power module's current capability, the heat dissipation characteristics of a package are important in determining the performance. A trade-off exists among heat dissipation characteristics, package size, and isolation characteristics. The key to a good package technology lies in the optimization package size while maintaining outstanding heat dissipation characteristics without compromising the isolation rating. In SPM 3 version 2, technology was developed with DBC substrate that resulted in excellent heat dissipation characteristics. This technology made it possible to achieve improved reliability and heat dissipation. Power chips are attached directly to the DBC substrate. Figures 5 and 6 show the package outline and the cross-sections of the SPM 3 version 2 package.

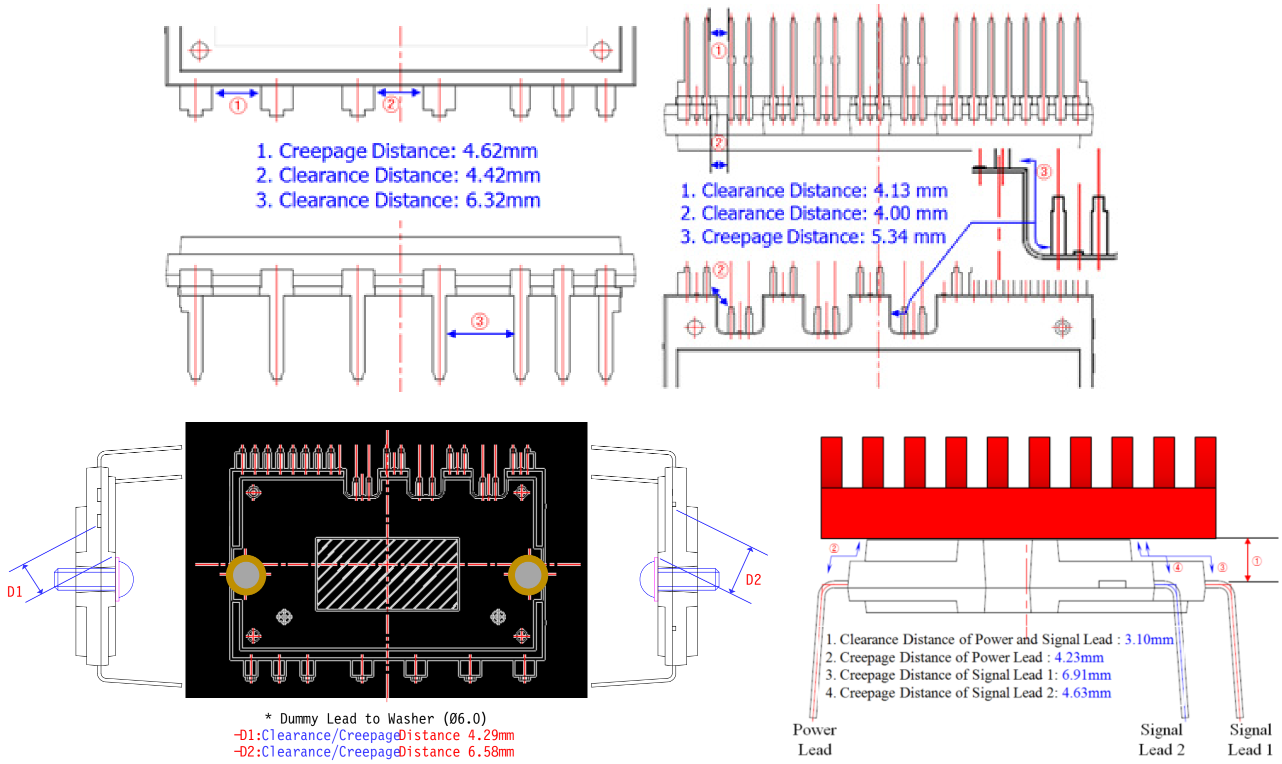


Figure 5. Isolation Distance for Pins, Mounting Screw and Pins to Heatsink

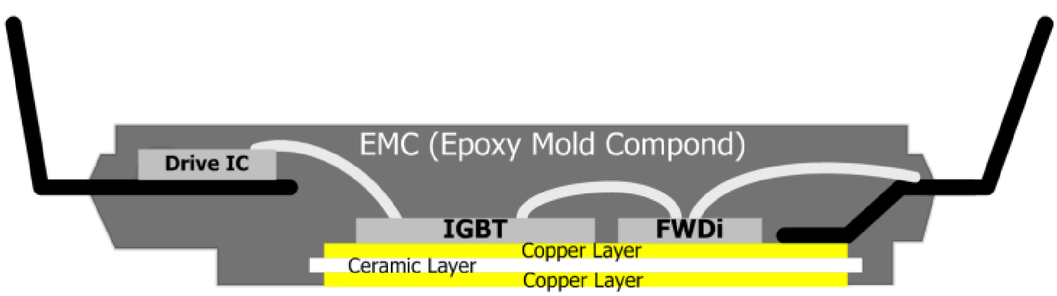
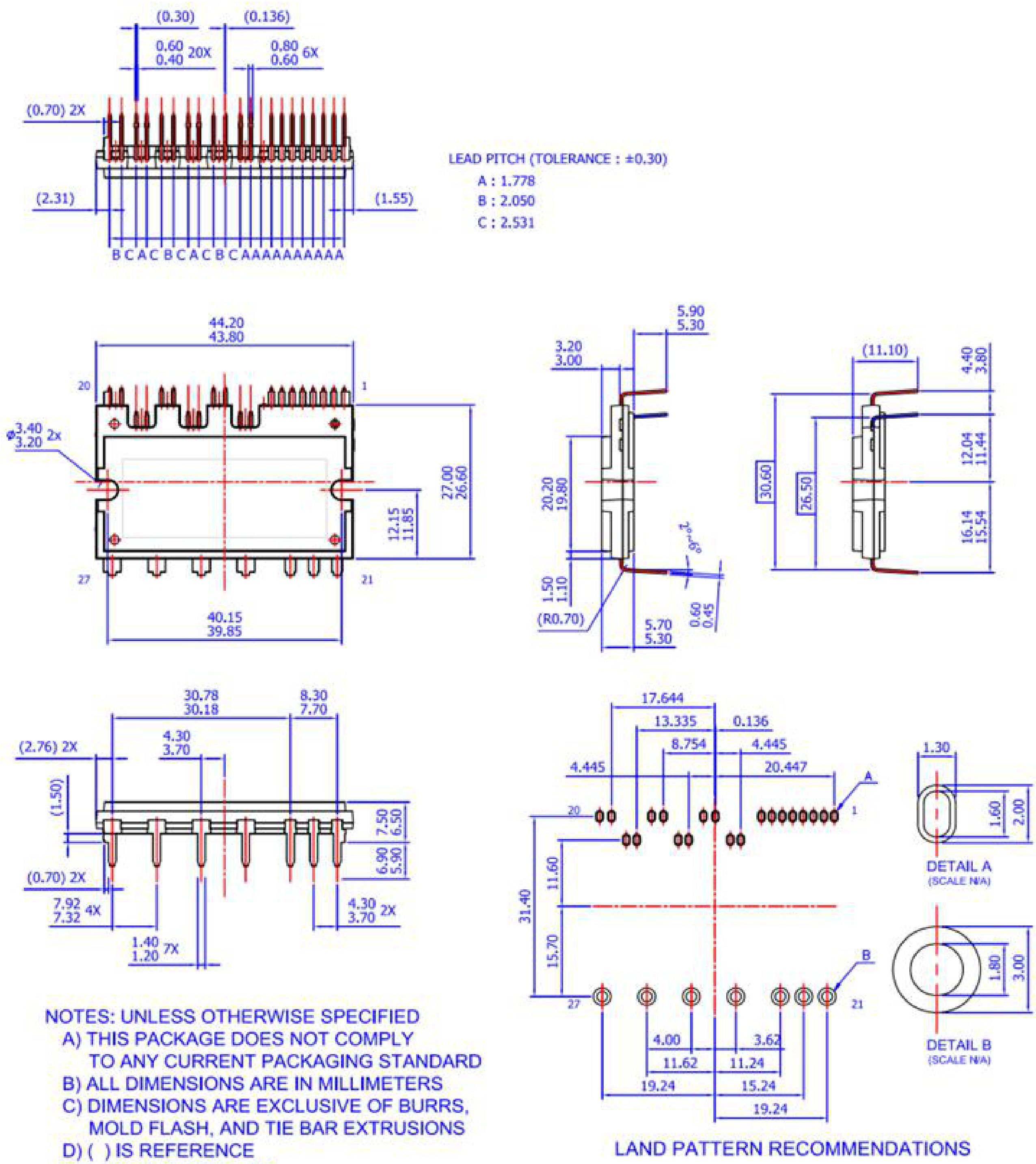


Figure 6. Package Structure and Cross Section for SPM 3 Version 2

Package Outline



NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE DOES NOT COMPLY TO ANY CURRENT PACKAGING STANDARD
B) ALL DIMENSIONS ARE IN MILLIMETERS
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D) ( ) IS REFERENCE
E) [ ] IS ASS'Y QUALITY
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Figure 7. Package Outline

PRODUCT SYNOPSIS

Absolute maximum ratings, electric characteristics, recommended operating conditions and mechanical characteristics are focused on in this section. Please refer to respective data sheets for the detailed description of each product.

Table 3. ABSOLUTE MAXIMUM RATING (T_J = 25 °C, unless otherwise specified)

Symbol	Parameter	Conditions	Rating	Unit
INVERTER PART (Base on NFA33012L72D)				
V_{PN}	Supply Voltage	Applied between P – NU, NV, NW	900	V
$V_{PN(surge)}$	Supply Voltage (Surge)	Applied between P – NU, NV, NW (Note 3)	1000	
V_{ces}	Collector – Emitter Voltage	(Note 2)	1200	
$\pm I_c$	Each IGBT Collector Current	T_c = 25 °C, $T_J \le$ 150 °C	30	A
$\pm I_{cp}$	Each IGBT Collector Current (Peak)	T_c = 25 °C, $T_J \le$ 150 °C, Under 1 ms Pulse Width	60	
P_c	Collector Dissipation	T_c = 25 °C per One Chip (Note 4)	357	W
T_J	Operating Junction Temperature		−40~150	°C
CONTROL PART				
V_{DD}	Control Supply Voltage	Applied between VDD(XX) – VSS	20	V
V_{BS}	High-Side Control Bias Voltage	Applied between VB(X) – VS(X)	20	
V_{IN}	Input Signal Voltage	Applied between HIN(X), LIN(X) – VSS	−0.3 ~ V_{DD} + 0.3	
V_{FO}	Fault Output Supply Voltage	Applied between VFO – VSS	−0.3 ~ V_{DD} + 0.3	
I_{FO}	Fault Output Current	Sink Current at VFO Pin	2	mA
V_{ITRIP}	Current Sensing Input Voltage	Applied between ITRIP – VSS	−0.3 ~ V_{DD} + 0.3	V
BOOTSTRAP DIODE PART				
V_{RRM}	Maximum Repetitive Reverse Voltage		1200	V
T_J	Operating Junction Temperature		−40~150	°C
TOTAL SYSTEM				
$V_{PN(PROT)}$	Self-Protection Supply Voltage Limit (Short-Circuit Protection Capability)	VDD(XX), VB(X) = 13.5 ~ 16.5 V, T_J = 150 °C, (Non-Repetitive, < 2 μs)	800	V
T_c	Case Operation Temperature	See Figure 8	−40~125	°C
T_{stg}	Storage Temperature		−40~125	
V_{iso}	Isolation Voltage	60 Hz, Sinusoidal, 1-minute, Connect Pins to Heat Sink	2500	Vrms

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. This is not for continuous DC voltage. Recommend to use max 960 V (80% of rated voltage) for continuous DC voltage
3. Surge voltage generated by the switching operation due to the wiring inductance between P and NU, NV, NW terminals.

Table 4. THERMAL RESISTANCE

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-c)Q}$	Junction to Case Thermal Resistance (Note 4)	Inverter IGBT Part (per 1/6 Module)	–	–	0.35	°C/W
$R_{th(j-c)F}$		Inverter FWDi Part (per 1/6 Module)	–	–	0.70	
$L\sigma$	Package Stray Inductance	P to NU,NV,NW		24		nH

4. For the measurement point of case temperature (Tc), please refer to Figure 8.

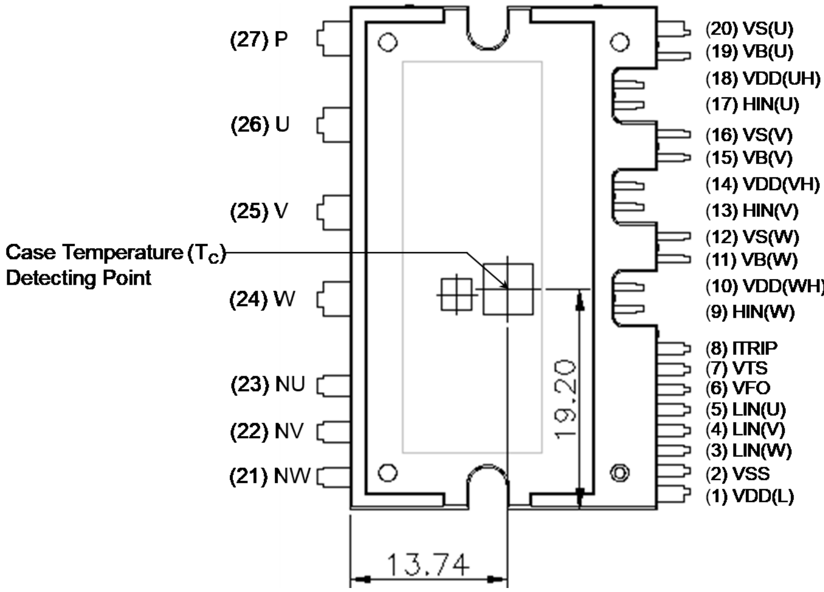


Figure 8. Case Temperature (Tc) Detecting Point

Table 5. ELECTRICAL CHARACTERISTIC (V_{DD} = 15 V and T_J = 25 °C, unless otherwise specified)

Symbol		Parameter	Condition	Min	Typ	Max	Unit
INVERTER PART (Base on NFA33012L72D)							
$V_{CE(sat)}$		Collector – Emitter Saturation Voltage	V_{DD} = V_{BS} = 15 V, I_c = 20 A, T_J = 25 °C	–	1.50	1.90	V
V_F		FWDi Forward Voltage	VIN = 0 V, IF = 20 A, T_J = 25 °C	–	1.70	2.10	
HS	t_{on}	High Side Switching Times	VPN = 600 V, VDD(XX) = 15 V, VBS(X) = 15 V, Ic = 20 A, T_J = 25 °C, HIN(X) = 0 V ↔ 5 V, Inductive Load (Note 5) See Figure 9	0.90	1.05	1.20	μs
	$t_{c(on)}$			–	0.15	0.30	
	t_{off}			–	1.15	1.25	
	$t_{c(off)}$			–	0.25	0.35	
	t_{rr}			–	0.20	–	
LS	t_{on}	Low Side Switching Times	VPN = 600 V, VDD(XX) = 15 V, VBS(X) = 15 V, Ic = 20 A, T_J = 25 °C, LIN(X) = 0 V ↔ 5 V, Inductive Load (Note 5) See Figure 9	0.60	0.75	0.95	μs
	$t_{c(on)}$			–	0.18	0.30	
	t_{off}			–	1.07	1.17	
	$t_{c(off)}$			–	0.25	0.35	
	t_{rr}			–	0.20	–	
I_{ces}		Collector – Emitter Leakage Current	Vce = Vces , T_J = 25 °C	–	–	1	mA
BOOTSTRAP CIRCUIT PART							
V_F		Bootstrap Diode Forward Voltage	IF = 10 mA, TJ = 25 °C (Including voltage drop by resistor)	0.7	1.05	1.4	V
			IF = 100 mA, TJ = 25 °C (Including voltage drop by resistor)	2.3	3.3	4.3	
R_{BOOT}		Built-in Limiting Resistance		15	20	28	Ω

Table 5. ELECTRICAL CHARACTERISTIC (V_{DD} = 15 V and T_J = 25 °C, unless otherwise specified) (continued)

Symbol	Parameter	Condition		Min	Typ	Max	Unit
CONTROL PART							
I_{QDDH}	Quiescent VDD Supply Current	VDD(xH) = 15 V, HIN(X) = 0 V	VDD(xH) – VSS	–	–	0.15	mA
I_{QDDL}		VDD(L) = 15 V, LIN(X) = 0 V	VDD(L) – VSS	–	–	5.00	
I_{QBS}	Quiescent VBS Supply Current	VB(X) – VS(X) = 15 V, HIN(X) = 0 V	VB(X) – VS(X)	–	–	0.30	
V_{FOH}	Fault Output Voltage	ITRIP= 0 V, 4.7 kΩ Pulled up to 5 V		4.5	–	–	V
V_{FOL}		ITRIP = 1 V, 4.7 kΩ Pulled up to 5 V		–	–	0.5	
V_{ITRIP}	Over Current Trip Level (Note 6)	V_{DD} = 15 V	ITRIP – VSS	0.45	0.50	0.55	V
U_{VDDD}	Supply Circuit, Under-Voltage Protection	Detection Level		10.3	–	12.8	V
U_{VDDR}		Reset Level		10.8	–	13.3	
U_{VBSD}		Detection Level		9.5	–	12.0	
U_{VBSR}		Reset Level		10.0	–	12.5	
t_{FOD}	Fault-Out Pulse Width			50	–	–	μs
V_{TS}	Voltage Output for LVIC Temperature Sensing Unit (Note 7)	VDD(L) = 15 V, TLVIC = 25 °C		0.88	0.98	1.08	V
$V_{IN(ON)}$	ON Threshold Voltage	Applied between HIN(X), LIN(X) – VSS		–	–	2.6	V
$V_{IN(OFF)}$	OFF Threshold Voltage			0.8	–	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. ton and toff include the propagation delay time of the internal drive IC. tc(on) and tc(off) are the switching time of IGBT itself under the given gate driving condition internally. For the detailed information, please see and Figure 9.
6. Short-circuit current protection is functioning only at the low-sides.
7. TLVIC is the temperature of LVIC itself. VTS is only for sensing temperature of LVIC and cannot shutdown IGBTs automatically.

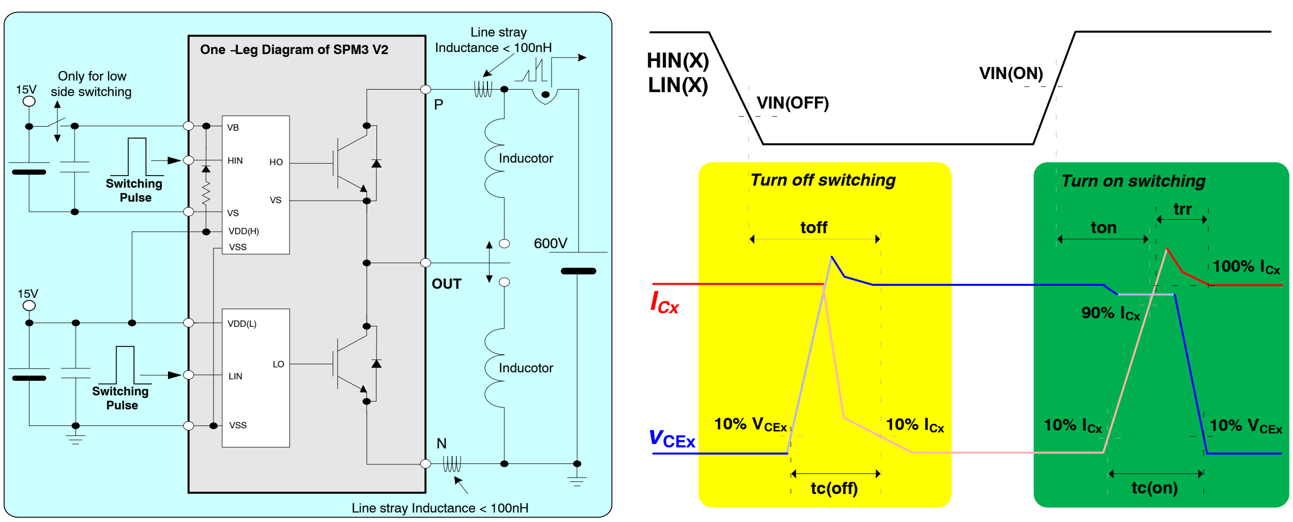


Figure 9. Switching Evaluation Circuit and Switching Time Definition

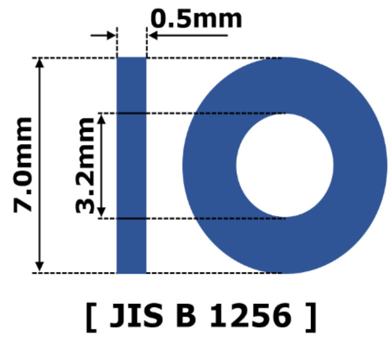
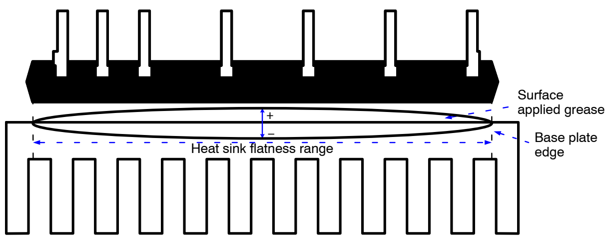
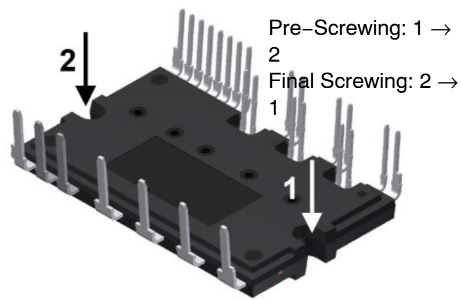
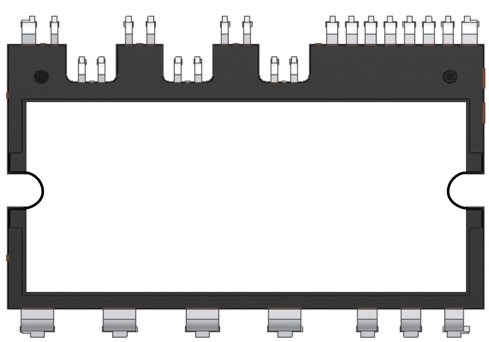
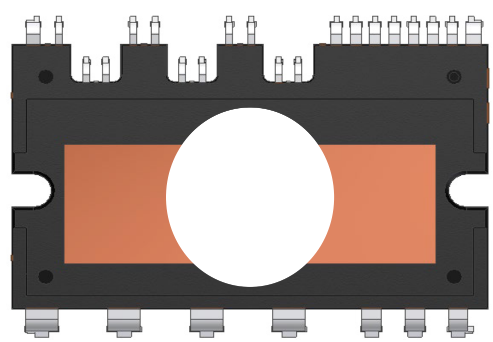
Table 6. RECOMMENDED OPERATING CONDITIONS (Base on NFA33012L72D)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{PN}	Supply Voltage	Applied between P – N_X	–	600	800	V
V_{DD}	Control Supply Voltages	Applied between VDD(XH) – V_{SS}	13.5	15.0	16.5	
V_{BS}	High-Side Bias Voltage	Applied between VB(X) – VS(X)	13.0	15.0	18.5	
dV_{DD} / dt, d_{VBS} / dt	Supply Voltage Variation		−1	–	1	V/μs
T_{dead}	Blanking Time for Preventing Arm – Short	For Each Input Signal	1.5	–	–	μs
f_{PWM}	PWM Frequency	−40 °C ≤ T_c ≤ 125 °C, −40 °C ≤ T_J ≤ 150 °C	–	–	20	kHz
$P_{WIN(ON)}$	Minimum Input Pulse Width (Note 9)	V_{DD} = V_{BS} = 15 V, Wiring Inductance between NU, NV, NW and DC Link N < 10 nH	1.5	–	–	μs
$P_{WIN(OFF)}$			2.0	–	–	
Package Mounting Torque		M3 Type Screw	0.6	0.7	0.9	Nm

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

8. Flatness tolerance of the heatsink should be within −50 μm to +100 μm.
9. Product might not make response if input pulse width is less than the recommended value.

Table 7. MECHANICAL CHARACTERISTICS

Item	Recommended Condition
Pitch	40.0 ±0.15 mm (Please refer to Package Outline Diagram)
Screw	Diameter: M3 Screw head types: pan head, truss head, binding head
Washer	Plane washer dimensions 
Heat sink	Material: Aluminum or Copper Warpage (the surface that contacts IPM): −50 to 100 μm No contamination on the heat sink surface that contacts IPM
Torque	Pre. tightening: 0.2~0.3 Nm on first screw Pre. tightening: 0.2~0.3 Nm on second screw Final tightening: 0.6~0.9 Nm on first screw Final tightening: 0.6~0.9 Nm on second screw 
Grease	Silicone grease. Thickness: 100 to 200 μm Uniformly apply silicon grease on whole IPM TOP surface. Thermal foils are only recommended after careful evaluation. Thickness, stiffness and compressibility parameters have a strong influence on performance.  Recommended  Do not Recommended

OPERATION SEQUENCE FOR PROTECTIONS

Short Circuit Protection

The 1200 V SPM 3 version 2 use external shunt resistor for the over current detection, as shown in Figure 10. The LVIC has a built-in over current protection function that senses the voltage to the ITRIP pin. If this voltage exceeds the VITRIP specified in the device data sheets (VITRIP, typ. is 0.50 V), a fault signal is asserted and all three low side IGBTs are turned off. Short circuit is included to over current situation. Typically, the maximum short-circuit current magnitude is gate-voltage dependent: higher gate voltage (VDD and VBS) is resulted in a larger short-circuit current. It is recommended that the maximum over current trip level is set below 1.5 times the nominal rated current. Over current protection-timing chart is shown in Figure 11.

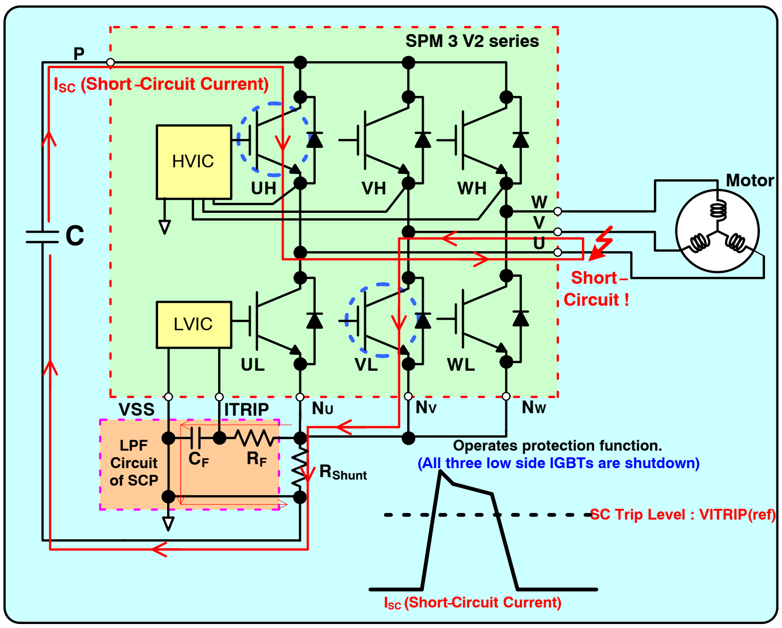
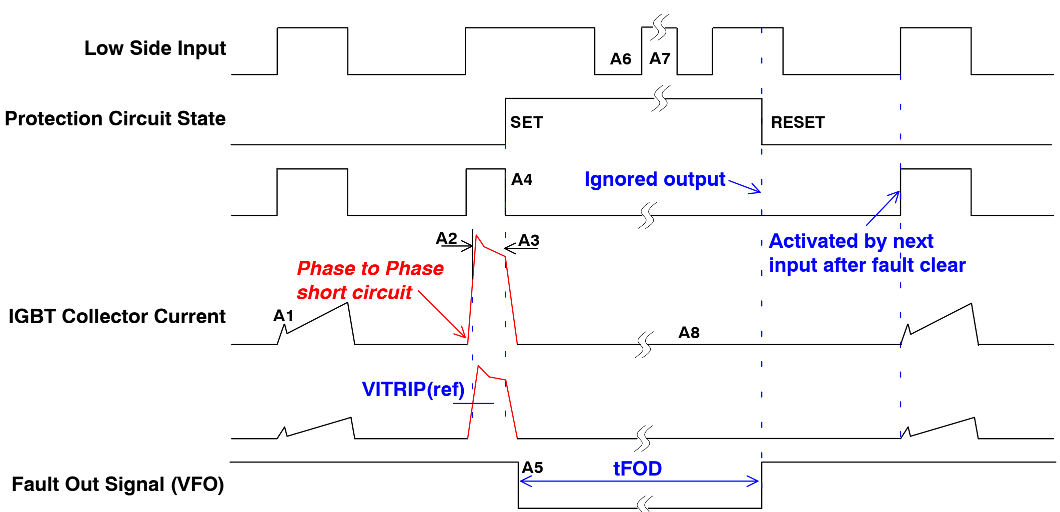


Figure 10. Operation of Short-Circuit Protection



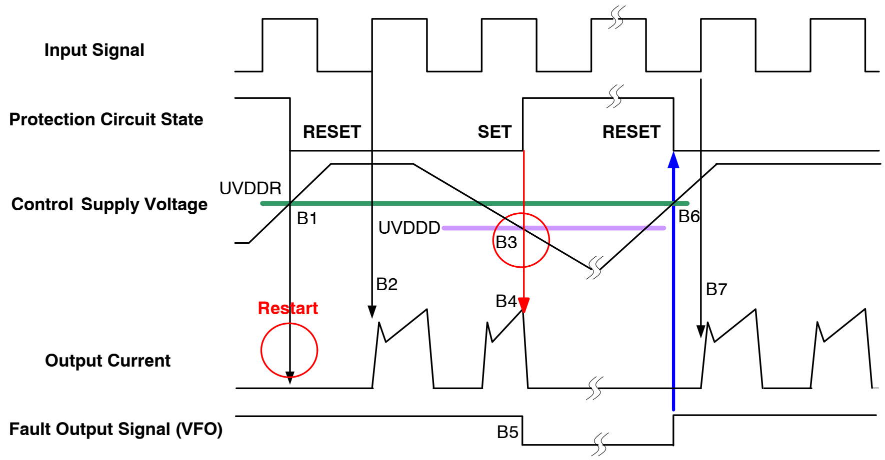
NOTE:

1. A1-Normal operation: IGBTs turn on and carrying current.
2. A2-Short circuit current detection (SC trigger).
3. A3-All low-side IGBT's gate are hard interrupted.
4. A4-All low side IGBTs turn off.
5. A5-Fault output timer operation start with internal delay(Typ. 3.0 μs), tFOD=min. 50 μs.
6. A6-Input "L": Low side IGBTs OFF state.
7. A7-Input "H": Low side IGBTs input ON state, but during the active period of fault output the IGBT doesn't turn ON.
8. A8-Low side IGBTs keeps OFF state.

Figure 11. Timing Chart of Short-Circuit Protection Function

Under-Voltage Lock Out Protection

The LVIC has an Under-Voltage Lock Out protection (UVLO) function to protect the low-side IGBTs from operation with insufficient gate driving voltage. A timing chart for this protection is shown in Figure 12.

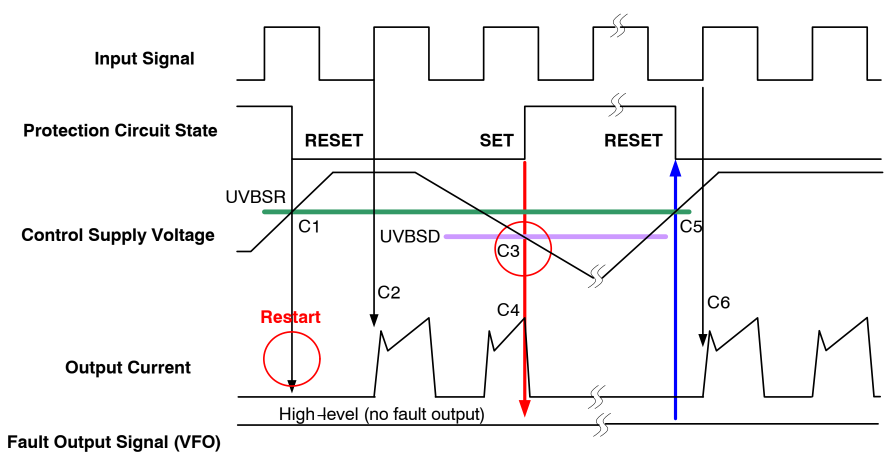


NOTE:

9. B1-Control supply voltage rise: after the voltage rises UVDDR, the circuits start to operate when the next input is applied.
10. B2-Normal operation: IGBT ON and carrying current.
11. B3-Under-voltage detection (UVDDD).
12. B4-IGBT OFF in spite of control input is alive.
13. B5-Fault output signal starts.
14. B6-Under-voltage reset (UVDDR).
15. B7-Normal operation: IGBT ON and carrying current.

Figure 12. Timing Chart of Low-side Under-Voltage Protection Function

The HVIC has an under-voltage lockout function to protect the high-side IGBT from insufficient gate driving voltage. A timing chart for this protection is shown in Figure 13. A fault-out (VFO) alarm is not given for low.



NOTE:

16. C1-Control supply voltage rises: after the voltage reaches UVBSR, the circuit starts when the next input is applied.
17. C2-Normal operation: IGBT ON and carrying current.
18. C3-Under-voltage detection (UVBSD).
19. C4-IGBT OFF in spite of control input is alive, but there is no fault output signal.
20. C5-Under-voltage reset (UVBSR).
21. C6-Normal operation: IGBT ON and carrying current.

Figure 13. Timing Chart of High-Side Under-Voltage Protection Function

KEY PARAMETER DESIGN GUIDANCE

For stable operation, there are recommended parameters for passive components and bias conditions, considering operating characteristics of the 1200 V SPM 3 version 2 series. This section focuses on the key parameter design guidance.

Circuit of VTS

The Thermal Sensing Unit(VTS) analog voltage output reflects the temperature of the LVIC in 1200 V SPM 3 version 2 series products. The relationship between VTS output voltage and LVIC temperature is shown in Figure 15. It does not have any self-protection function, and, therefore, it should be used appropriately based on application requirement. It should be noted that there is a time lag from IGBT temperature to LVIC temperature. It is very difficult to respond quickly when temperature rises sharply in a transient condition such as shoot-through event. Even though VTS has some limitation, it will be definitely useful in enhancing the system reliability. Figure 14 shows the LVIC location for VTS function of SPM 3 version 2 series and Figure 15 shows that the relationship between VTS voltage and LVIC temperature.

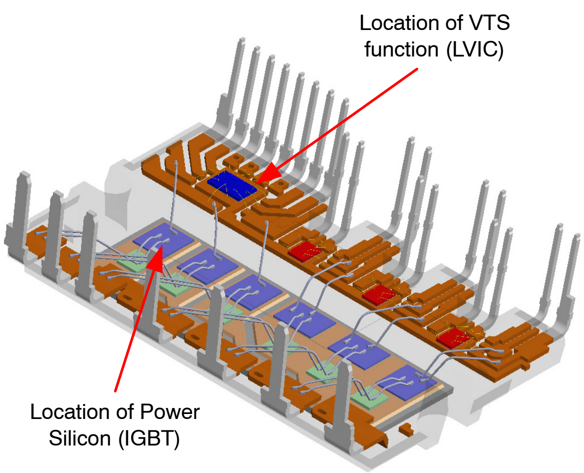


Figure 14. Location of VTS Function (LVIC)

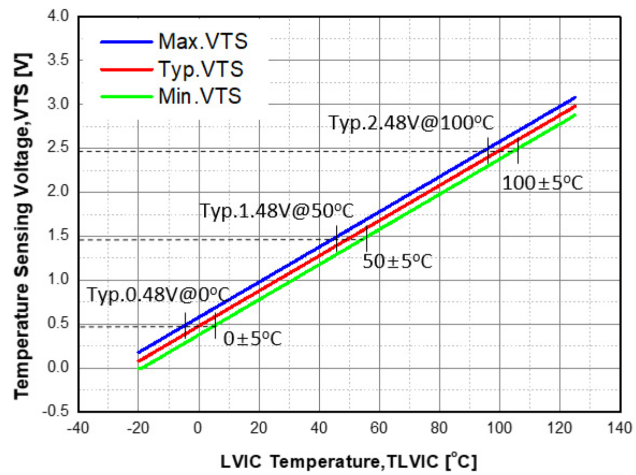


Figure 15. Temperature vs. VTS

Figure 16 shows the equivalent circuit diagram of VTS inside LVIC and a typical application diagram. This output voltage is clamped to 5.2 V by an internal Zener diode, but in case the maximum input range of Analog to Digital converter of MCU is below 5.2 V. an external Zener diode should be inserted between an A/D input and the analog ground pin of MCU. An amplifier can be used to change the range of voltage input to MCU to have better resolution of the temperature. It is recommended to add a ceramic capacitor of 10 nF to make the VTS more stable. Relationship of VTS and TLVIC can be expressed as the following equation.

$$VTS,_{Min} = 0.02 \times T_{LVIC} + 0.480 - 0.100\ (V) \quad \text{(eq. 1)}$$

$$VTS,_{Typ} = 0.02 \times T_{LVIC} + 0.480\ (V) \quad \text{(eq. 2)}$$

$$VTS,_{Max} = 0.02 \times T_{LVIC} + 0.480 + 0.100\ (V) \quad \text{(eq. 3)}$$

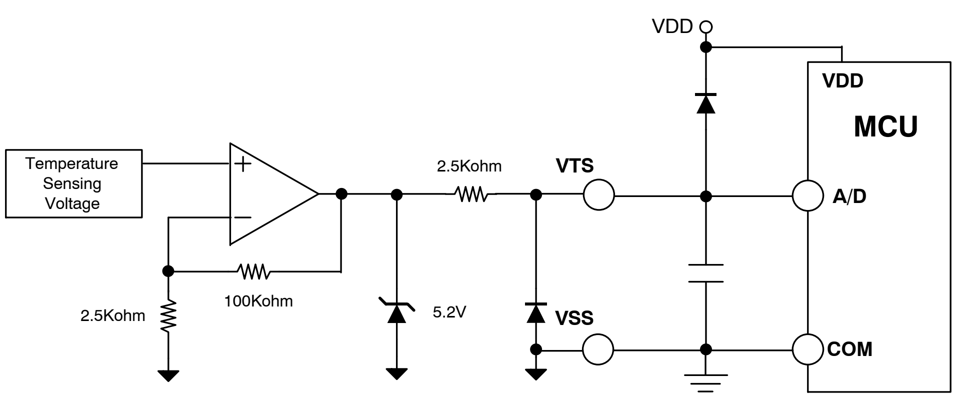


Figure 16. Internal Block Diagram and Interface Circuit of VTS

Table 8. VTS TABLE OF NFA3XX12L72D

T (°C)	Min (V)	Typ (V)	Max (V)	T (°C)	Min (V)	Typ (V)	Max (V)	T (°C)	Min (V)	Typ (V)	Max (V)	T (°C)	Min (V)	Typ (V)	Max (V)
−20	0.000	0.080	0.180	17	0.720	0.820	0.920	54	1.460	1.560	1.660	91	2.200	2.300	2.400
−19	0.000	0.100	0.200	18	0.740	0.840	0.940	55	1.480	1.580	1.680	92	2.220	2.320	2.420
−18	0.020	0.120	0.220	19	0.760	0.860	0.960	56	1.500	1.600	1.700	93	2.240	2.340	2.440
−17	0.040	0.140	0.240	20	0.780	0.880	0.980	57	1.520	1.620	1.720	94	2.260	2.360	2.460
−16	0.060	0.160	0.260	21	0.800	0.900	1.000	58	1.540	1.640	1.740	95	2.280	2.380	2.480
−15	0.080	0.180	0.280	22	0.820	0.920	1.020	59	1.560	1.660	1.760	96	2.300	2.400	2.500
−14	0.100	0.200	0.300	23	0.840	0.940	1.040	60	1.580	1.680	1.780	97	2.320	2.420	2.520
−13	0.120	0.220	0.320	24	0.860	0.960	1.060	61	1.600	1.700	1.800	98	2.340	2.440	2.540
−12	0.140	0.240	0.340	25	0.880	0.980	1.080	62	1.620	1.720	1.820	99	2.360	2.460	2.560
−11	0.160	0.260	0.360	26	0.900	1.000	1.100	63	1.640	1.740	1.840	100	2.380	2.480	2.580
−10	0.180	0.280	0.380	27	0.920	1.020	1.120	64	1.660	1.760	1.860	101	2.400	2.500	2.600
−9	0.200	0.300	0.400	28	0.940	1.040	1.140	65	1.680	1.780	1.880	102	2.420	2.520	2.620
−8	0.220	0.320	0.420	29	0.960	1.060	1.160	66	1.700	1.800	1.900	103	2.440	2.540	2.640
−7	0.240	0.340	0.440	30	0.980	1.080	1.180	67	1.720	1.820	1.920	104	2.460	2.560	2.660
−6	0.260	0.360	0.460	31	1.000	1.100	1.200	68	1.740	1.840	1.940	105	2.480	2.580	2.680
−5	0.280	0.380	0.480	32	1.020	1.120	1.220	69	1.760	1.860	1.960	106	2.500	2.600	2.700
−4	0.300	0.400	0.500	33	1.040	1.140	1.240	70	1.780	1.880	1.980	107	2.520	2.620	2.720
−3	0.320	0.420	0.520	34	1.060	1.160	1.260	71	1.800	1.900	2.000	108	2.540	2.640	2.740
−2	0.340	0.440	0.540	35	1.080	1.180	1.280	72	1.820	1.920	2.020	109	2.560	2.660	2.760
−1	0.360	0.460	0.560	36	1.100	1.200	1.300	73	1.840	1.940	2.040	110	2.580	2.680	2.780
0	0.380	0.480	0.580	37	1.120	1.220	1.320	74	1.860	1.960	2.060	111	2.600	2.700	2.800
1	0.400	0.500	0.600	38	1.140	1.240	1.340	75	1.880	1.980	2.080	112	2.620	2.720	2.820
2	0.420	0.520	0.620	39	1.160	1.260	1.360	76	1.900	2.000	2.100	113	2.640	2.740	2.840
3	0.440	0.540	0.640	40	1.180	1.280	1.380	77	1.920	2.020	2.120	114	2.660	2.760	2.860
4	0.460	0.560	0.660	41	1.200	1.300	1.400	78	1.940	2.040	2.140	115	2.680	2.780	2.880
5	0.480	0.580	0.680	42	1.220	1.320	1.420	79	1.960	2.060	2.160	116	2.700	2.800	2.900
6	0.500	0.600	0.700	43	1.240	1.340	1.440	80	1.980	2.080	2.180	117	2.720	2.820	2.920
7	0.520	0.620	0.720	44	1.260	1.360	1.460	81	2.000	2.100	2.200	118	2.740	2.840	2.940
8	0.540	0.640	0.740	45	1.280	1.380	1.480	82	2.020	2.120	2.220	119	2.760	2.860	2.960
9	0.560	0.660	0.760	46	1.300	1.400	1.500	83	2.040	2.140	2.240	120	2.780	2.880	2.980
10	0.580	0.680	0.780	47	1.320	1.420	1.520	84	2.060	2.160	2.260	121	2.800	2.900	3.000
11	0.600	0.700	0.800	48	1.340	1.440	1.540	85	2.080	2.180	2.280	122	2.820	2.920	3.020
12	0.620	0.720	0.820	49	1.360	1.460	1.560	86	2.100	2.200	2.300	123	2.840	2.940	3.040
13	0.640	0.740	0.840	50	1.380	1.480	1.580	87	2.120	2.220	2.320	124	2.860	2.960	3.060
14	0.660	0.760	0.860	51	1.400	1.500	1.600	88	2.140	2.240	2.340	125	2.880	2.980	3.080
15	0.680	0.780	0.880	52	1.420	1.520	1.620	89	2.160	2.260	2.360				
16	0.700	0.800	0.900	53	1.440	1.540	1.640	90	2.180	2.280	2.380				

Selection of Shunt Resistor

Figure 17 shows an example circuit of the short circuit protection using 1-shunt resistor. The line current on the N side DC-ink is detected and the protective operation signal is passed through the RC filter. If the current exceeds the short circuit reference level, all the gates of the N-side three-phase IGBTs are switched to the off state and the VFO fault signal is transmitted to MCU. Since short circuit protection is non-repetitive, IGBT operation should be immediately halted when the VFO fault signal is given.

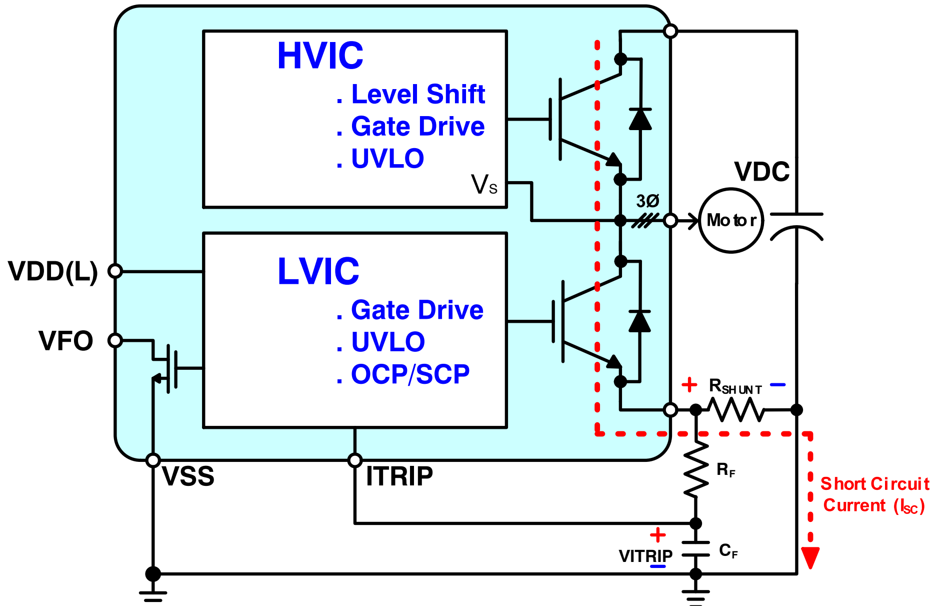


Figure 17. Short Circuit Current Protection Circuit with One Shunt Resistor

The value of shunt resistance is calculated by the following equation.

- Maximum Current Trip Level:
  - ♦ Depends on user selection:
  - – $I_{SC(max)}$ = 1.5 x I_C (Rated current)
- SC trip reference voltage:
  - ♦ Depends on data sheet
  - – VITRIP = Min. 0.45 V, Typ. 0.50 V, Max. 0.55 V
- Shunt resistance:
  - – $I_{SC(max)}$ = VITRIP_$_{Max.}$ / $R_{SHUNT(Min.)} \rightarrow R_{SHUNT(Min.)} = V_{SC(Max.)} / I_{SC(Max.)}$
- If the deviation of the shunt resistor should be limited below ± 5%,
  - – $R_{SHUNT(typ)}$ = VITRIP_$_{Typ.}$ / $I_{SC(max)}$,
  - – $R_{SHUNT(Min.)} = R_{SHUNT(Typ.)} \times 0.95$,
  - – $R_{SHUNT(Max\cdot)} = R_{SHUNT(Typ.)} \times 1.05$
- Actual short circuit trip current level becomes:
  - – $I_{SC(Typ\cdot)}$ = VITRIP_$_{Typ\cdot}$ / $R_{SHUNT(Typ\cdot)}$
  - – $I_{SC(Min\cdot)} = V_{SC(Min\cdot)} / R_{SHUNT(Max\cdot)}$
- Inverter output power:
  - – $P_{OUT} = \sqrt{3}$ x VO,LL x $I_{O(RMS)}$ x PF

  Where:
  - – $VO,LL = \frac{\sqrt{3}}{\sqrt{2}} \text{ x MI x } \frac{V_{DC}}{2}$
  - – $I_{O(RMS)}$ = Maximum load current of inverter
  - – M.I = Modulation Index
  - – VDC = DC link voltage
  - – PF = Power Factor
  - ♦ Average DC Current

– $I_{DC\_AVG} = (P_{out} \times Eff) / V_{DC\_Link}$
Where:
– Eff = Inverter Efficiency

- The power rating of shunt resistor is calculated by the following equation
  – $P_{SHUNT} = (I_{RMS}{}^2 \times R_{SHUNT} \times Margin) / De\text{-}rating\ Ratio$
  Where:
  – R_{SHUNT} is shunt resistance typical value at Tc = 25 °C
  – De-rating ratio is ratio of shunt resistor at T_{SHUNT} = 100 °C (From data sheet of shunt resistor)
  – Margin is safety margin (Determine by user)
- Shunt resistor calculation examples:
  ♦ Calculation conditions:
  – DUT: NFA33012L72D
  – Tolerance of shunt resistor: ± 5 %
  – SC Trip Reference Voltage, VITRIP:
  – $VITRIP_{\_Min.}$ = 0.45 V, $VITRIP_{\_Typ.}$ = 0.50V, $VITRIP_{\_Max.}$ = 0.55 V
  – Maximum Load Current of Inverter (I_{RMS}): 21 A_{rms}
  – Maximum Peak Load Current of Inverter (IC(max)): 45 A
  – Modulation Index(MI): 0.9
  – DC Link Voltage(VDC_Link): 600 V
  – Power Factor (PF): 0.8
  – Inverter Efficiency(Eff): 0.95
  – Shunt Resistor Value at Tc = 25 °C (R_{SHUNT}): 9.1 mΩ
  – De-rating Ration of Shunt Resistor at T_{SHUNT} = 100 °C: 70% (refer to Figure 18)
  – Safety Margin: 20 %
  ♦ Calculation results:
  – $I_{SC(Max\cdot)}$: $1.5 \times I_{C(Max\cdot)} = 1.5 \times 30\ A = 45\ A$
  – $R_{SHUNT(Typ\cdot)}$: $VITRIP_{\_Typ.} / I_{SC(Max\cdot)} = 0.50\ V / 45\ A = 11.1\ m\Omega$
  – $R_{SHUNT(Max\cdot)}$: $R_{SHUNT(Typ.)} \times 1.05 = 11.1\ m\Omega \times 1.05 = 11.6\ m\Omega$
  – $R_{SHUNT(Min\cdot)}$: $R_{SHUNT(Typ.)} \times 0.95 = 11.1\ m\Omega \times 0.95 = 10.5\ m\Omega$
  – $I_{SC(Min\cdot)}$: $VITRIP_{\_Min.} / R_{SHUNT(Max\cdot)} = 0.45\ V / 11.6\ m\Omega = 38.79\ A$
  – $I_{SC(Max\cdot)}$: $VITRIP_{\_Max.} / R_{SHUNT(Min\cdot)} = 0.55\ V / 10.5\ m\Omega = 52.38\ A$
  – $P_{OUT} = \sqrt{3}\ x \left(\frac{\sqrt{3}}{\sqrt{2}}\ x\ MI\ x\ \frac{V_{DC}}{2}\right) x\ I_{0(RMS)}\ x\ PF = \frac{3}{\sqrt{2}}\ x\ 0.9\ x\ (600 / 2)\ x\ 21\ x\ 0.8 = 9{,}622\ W$
  – $I_{DC\_AVG} = (P_{OUT} \times Eff) / V_{DC\_Link} = 15.23\ A$
  – $P_{SHUNT} = (I_{DC}{}^2{}_{\_AVG}\ R_{SHUNT} \times Margin) / De\text{-}rating\ Ratio = ((15.23)^2 \times 0.0111 \times 1.2) / 0.7 = 4.41\ W$ (therefore, the proper power rating of shunt resistor is over 4.41 W).

When over-current events are detected, the 1200 V SPM 3 version 2 series shuts down all low-side IGBTs and sends out the fault-out (VFO) signal. FAULT output timer operation starts with internal delay (typ. 3 us).

To prevent malfunction, it is recommended that an RC filter is inserted between Nx and ITRIP pin. To shut down IGBTs within 3 μs when over-current situation occurs, a time constant of 1.5 ~ 2 μs is recommended.

Table 9 shows the shunt resistance by typical current level of short-circuit protection for each product.

Table 9. OVER-CURRENT (OC) PROTECTION TRIP LEVEL

Device	R_{SHUNT}	Over current Trip Level	Remark
NFA31512L72D	22.2 mΩ	22.5 A	Typical value
NFA32512L72D	13.3 mΩ	37.5 A	
NFA33012L72D	11.1 mΩ	45.0 A	

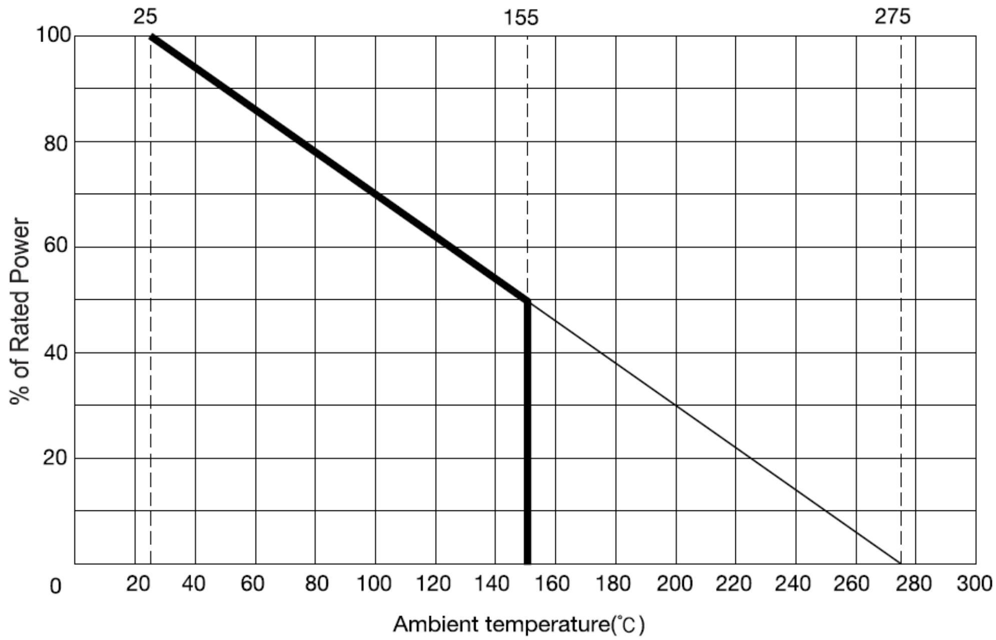


Figure 18. De-rating Curve Example of Shunt Resistor (from RARA Elec.)

Allowable Output Current

Figure 19 shows the allowable output current according to the switching frequency under the conditions described below. Inverter operation within the recommended current area is advised. The results may change depending on the applications and operating conditions.

$$\text{Condition}: V_{PN} = 600\text{ V}, V_{DD} = V_{BS} = 15\text{ V}, \text{M.I.} = 0.8,\ \text{P.F.} = 0.8, R_{thjc} = \text{Max.}, T_C = 100\,^\circ\text{C}, T_J = 125/150\,^\circ\text{C (Recommended/Allowable.)}, \text{3–phase modulation} \quad \text{(eq. 4)}$$

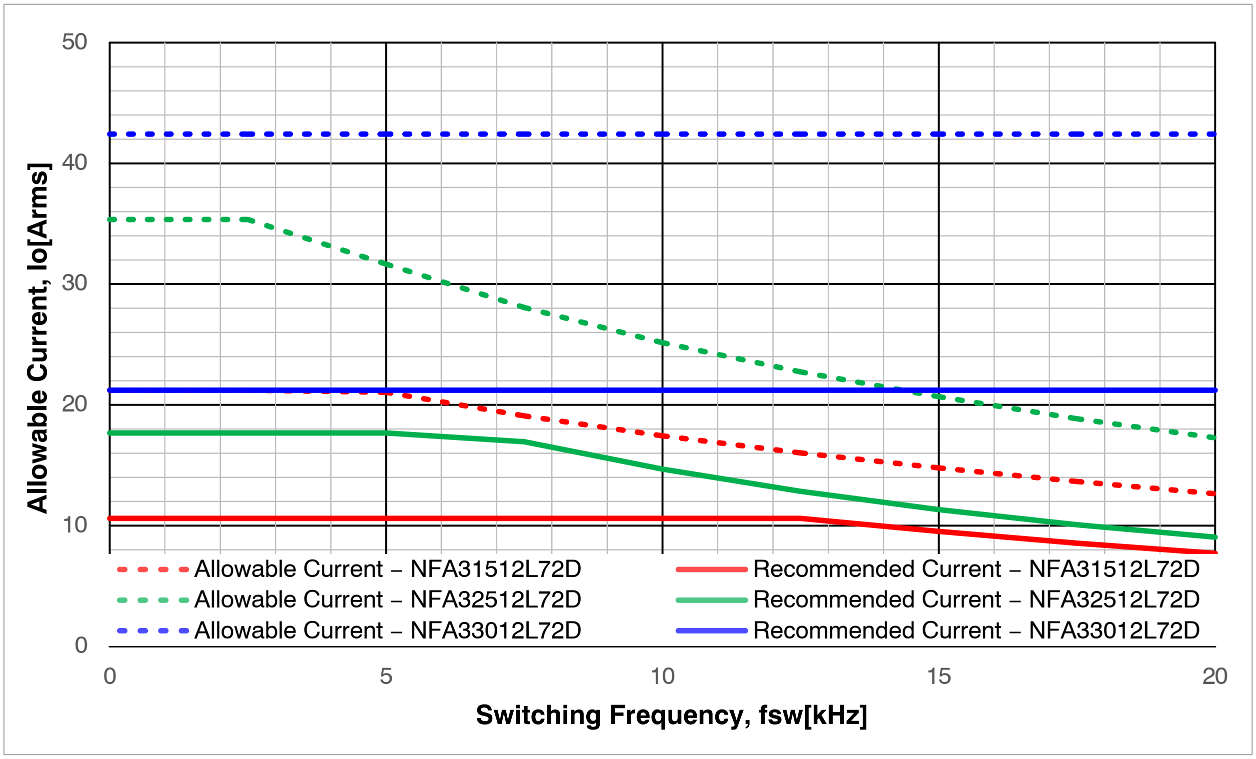


Figure 19. Allowable Operating Area by Switching Frequency for Each Product

Time Constant of Internal Delay

An RC filter prevents unexpected malfunction by related noise such as current protection and short circuit current protection (OCP, SCP) situation. The RC time constant is determined by the applied noise time and the Short-Circuit Withstanding Time (SCWT) of SPM 3 version 2 series. When the voltage of R_{shunt} exceeds the VITRIP level, It is applied to the ITRIP pin via the RC filter. The RC filter delay is the time required for the ITRIP voltage to rise to the referenced over current protection level. The LVIC has an internal filter time (logic filter time for noise elimination: around 0.85 μs). User should consider this filter time when they design the RC filter between shunt resistor and ITRIP pin. Figure 20 shows timing diagram of over current protection and short circuit protection. Measured time is shown Table 10. User should be considering each time sections for distribution under protection situation.

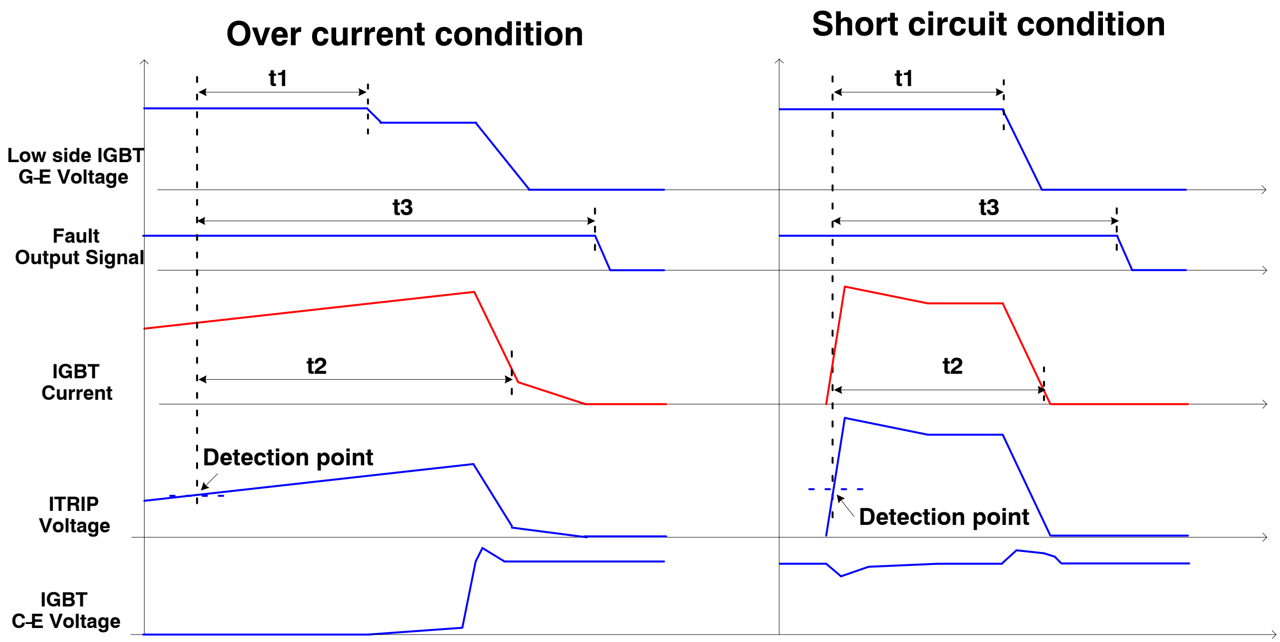


Figure 20. Timing Diagram of Over Current and Short Circuit Protection

Table 10. TIMETABLE OF O.C AND S.C PROTECTION; VITRIP TO LOW SIDE GATE, COLLECTOR CURRENT AND VFO

Ref. Condition VPN = 600 V, VDD = 15 V		Over Current (2 × rated current)						Short Circuit					
		t1 (μs) (Note 10)		t2 (μs) (Note 11)		t3 (μs) (Note 12)		t1 [μs] (Note 10)		t2 (μs) (Note 11)		t3 [(μs) (Note 12)	
Device	**T_J (°C)**	**Typ**	**Max**	**Typ**	**Max**	**Typ**	**Max**	**Typ**	**Max**	**Typ**	**Max**	**Typ**	**Max**
NFA31512L72D	**25**	1.25	1.50	1.00	1.30	3.00	4.00	1.25	1.50	0.90	1.20	3.00	4.00
	150	1.20	1.45	1.05	1.35	2.20	3.20	1.20	1.45	0.95	1.25	2.20	3.20
NFA32512L72D	**25**	1.25	1.50	1.10	1.40	3.00	4.00	1.25	1.50	1.00	1.30	3.00	4.00
	150	1.20	1.45	1.15	1.45	2.20	3.20	1.20	1.45	1.05	1.35	2.20	3.20
NFA33012L72D	**25**	1.25	1.50	1.10	1.40	3.00	4.00	1.25	1.50	1.00	1.30	3.00	4.00
	150	1.20	1.45	1.15	1.45	2.20	3.20	1.20	1.45	1.05	1.35	2.20	3.20

To guarantee safe short-circuit protection under all operating conditions, VITRIP should be detected within 1.0 μs after short circuit occurs. (Recommendation: SCWT < 3.0 μs, Conditions: VDC = 800 V, VDD = 16.5 V, T_J = 150 °C).
It is recommended that delay time should be minimized from short-circuit to ITRIP triggering

10. t1: from ITRIP detection to gate driver LO shut down
11. t2: from ITRIP detection to collector current 10%
12. t3: from ITRIP detection to fault out signal activation

SCSOA

Figures 21 through 23 show the typical SCSOA curves of each product. The graph for NFA33012L72D illustrates that if the short circuit time is less than 6.5 μs, IGBT can turn off safely. In this case, IGBT can shut down an SC current about 144 Apeak under a control supply voltage of 16.5 V. SCSOA region can change depending on operating condition (VPN, VDD, etc.).

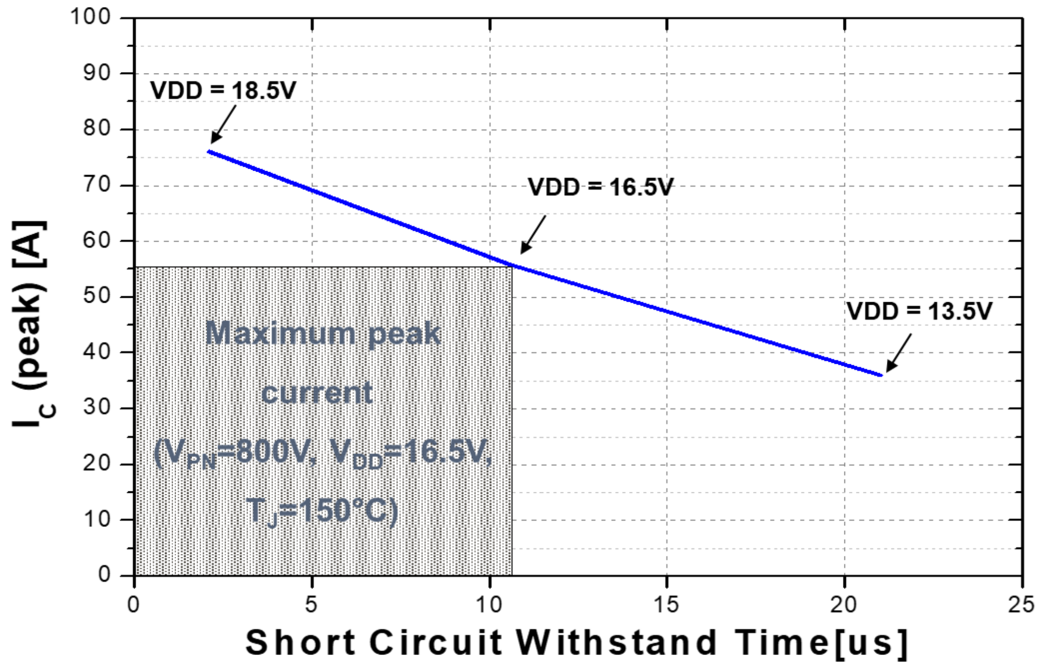


Figure 21. SCSOA Curve of NFA31512L72D (Typical)

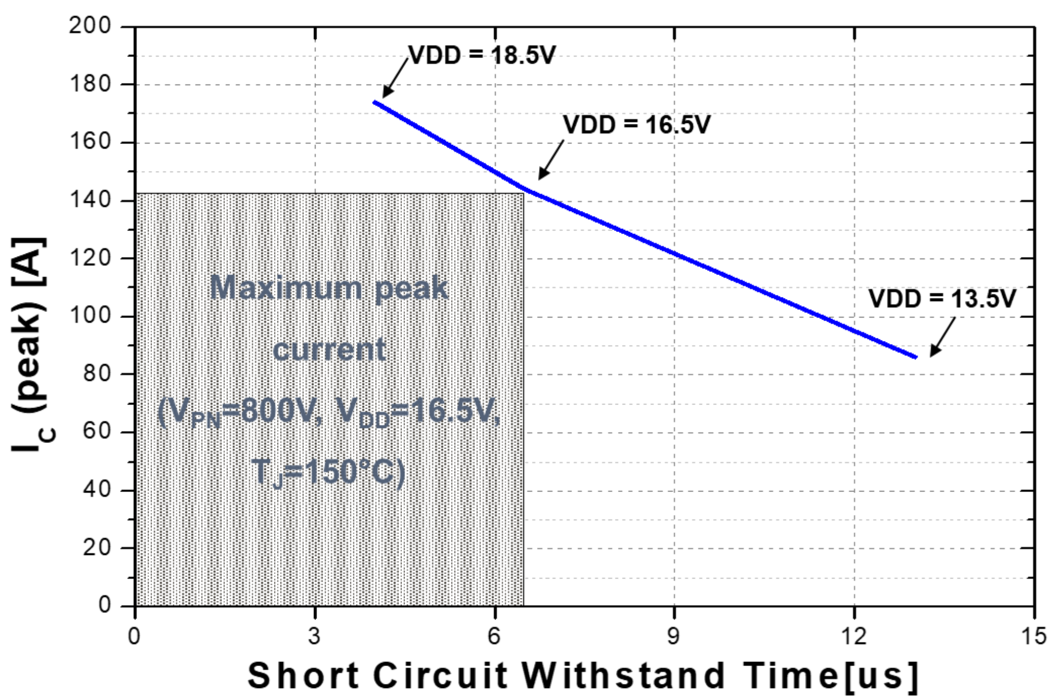


Figure 22. SCSOA Curve of NFA32512L72D (Typical)

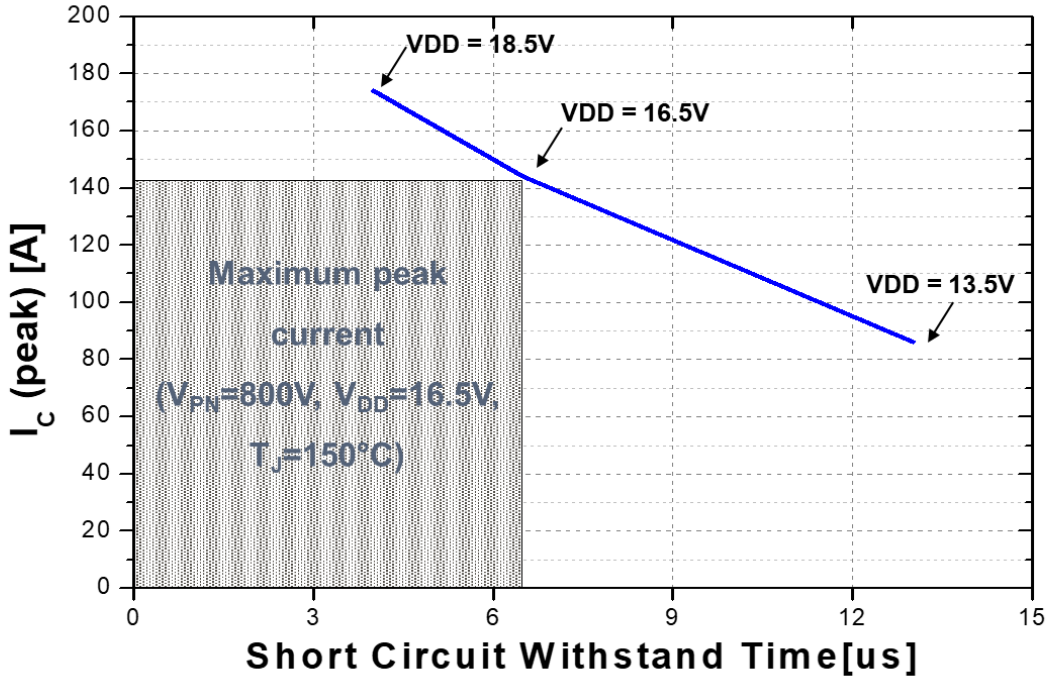


Figure 23. SCSOA Curve of NFA33012L72D (Typical)

Fault Output Circuit

VFO pin is the fault output alarm pin to give a fault state condition in SPM3 version 2 products. And an active low output is given on this pin for a fault state condition. The alarm conditions are Over-Current Protection (OCP), or low-side bias Under-Voltage Lock Out (UVLO) operation. The VFO output is open drain configured and VFO signal line should be pulled up to control power supply with 4.7 kΩ resistance as shown in Figure 24. The RC coupling shown dotted in Figure 24 can be changed depending on the application and the wiring impedance.

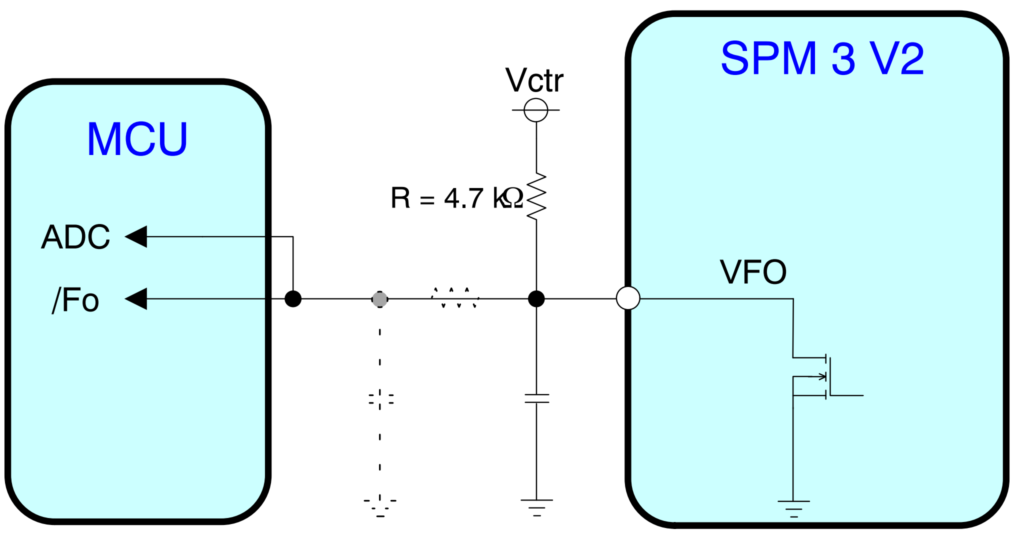


Figure 24. Propose Circuit for Fault Output Function

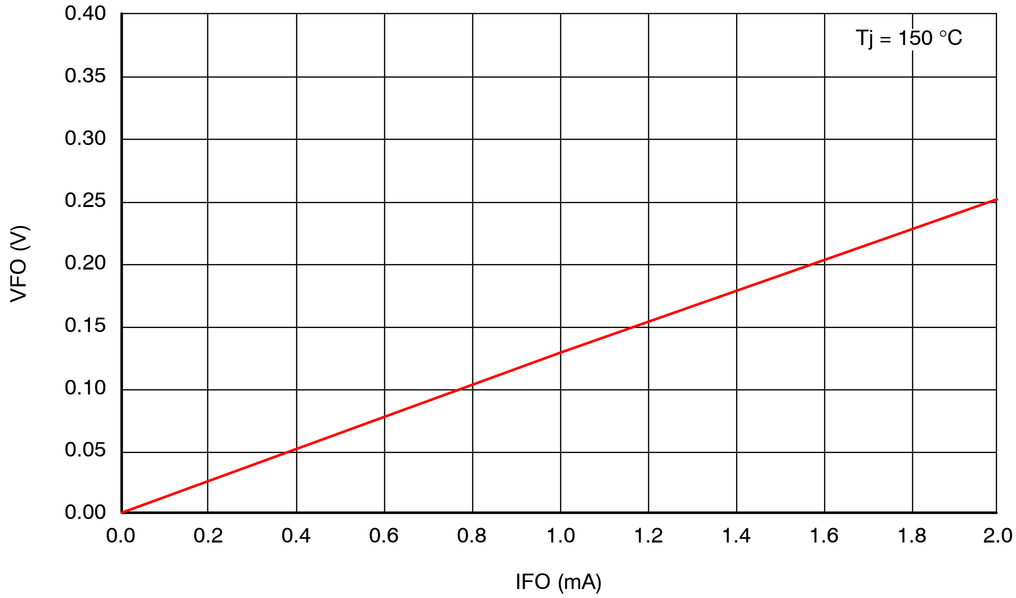


Figure 25. Voltage-Current Characteristics of VFO Terminal

Circuit of Input Signal (HINx, LINx)

Figure 26 shows recommended I/O interface circuit between the MCU and SPM 3 version 2. Because SPM 3 version 2 input logic is active HIGH and there are built-in pull-down resistors, external pull-down resistors are not needed.

Since the fault output is open drain and its rating is VDD + 0.3 V, 15 V supply interface is possible.

However, it is recommended that the fault output is configured with the 5 V logic supplies, which is the same as the input signals. It is also recommended that the decoupling capacitors is placed at both the MCU and Motion SPM 3 version 2 ends of the VFO signal line, as close as possible to each device. The RC coupling at each input (parts shown dotted in Figure 26) can be changed depending on the PWM control scheme used in the application and the wiring impedance of the PCB layout.

The input signal section of the SPM 3 version 2 series integrates a 5 kΩ (typical) pull-down resistor. Therefore, when using an external filtering resistor between the MCU output and the Motion SPM 3 version 2 input, attention should be given to the signal voltage drop at the Motion SPM 3 version 2 input terminals to satisfy the turn-on threshold voltage requirement. For instance, R = 100 Ω and C = 1 nF for the parts shown dotted in Figure 26.

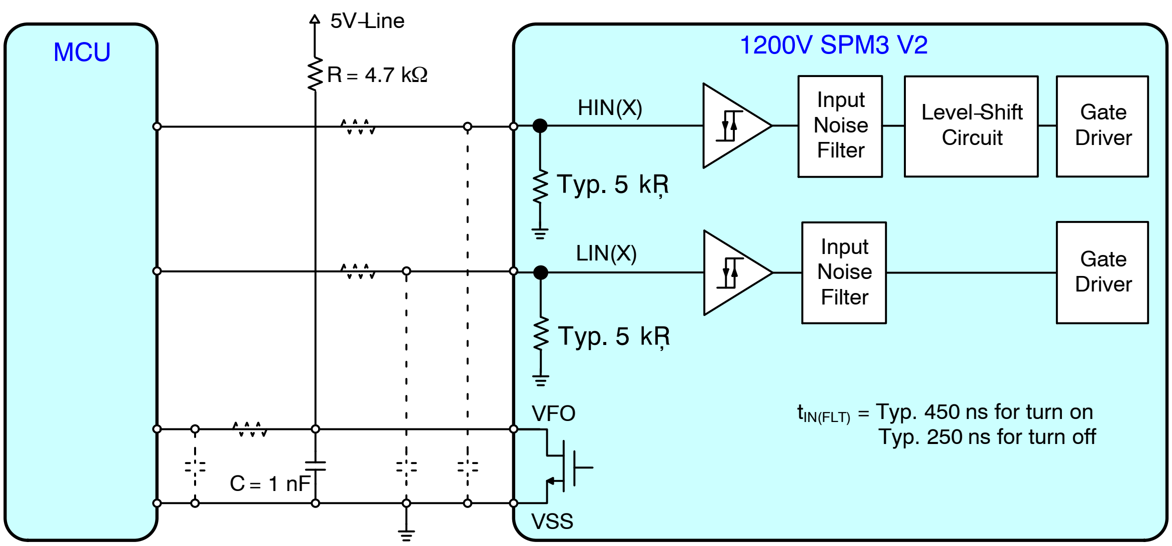


Figure 26. Recommended MCU I/O Interface Circuit

Bootstrap Circuit Design

Operation of Bootstrap Circuit

The VBS voltage, which is the voltage difference between VB(U,V,W) and VS(U,V,W), provides the supply to the HVIC within the 1200 V SPM 3 version 2 series. This supply must be in the range of 13.0 V ~ 18.5 V to ensure that the HVIC can fully drive the high-side IGBT. The SPM 3 version 2 series includes an under-voltage lock out protection function for the VBS to ensure that the HVIC does not drive the high-side IGBT, if the VBS voltage drops below a specified voltage. This function prevents the IGBT from operating in a high dissipation mode. There are a number of ways in which the VBS floating supply can be generated. One of them is the bootstrap method described here (refer to Figure 27). This method has the advantage of being simples and inexpensive. However, the duty cycle and on-time are limited by the requirement to refresh the charge in the bootstrap capacitor. The bootstrap to ground (either through the low-side or the load), the bootstrap capacitor (C_{BOOT}) is charged through the bootstrap diode (D_{BOOT}) and the resistor (R_{BOOT}) from the VDD supply.

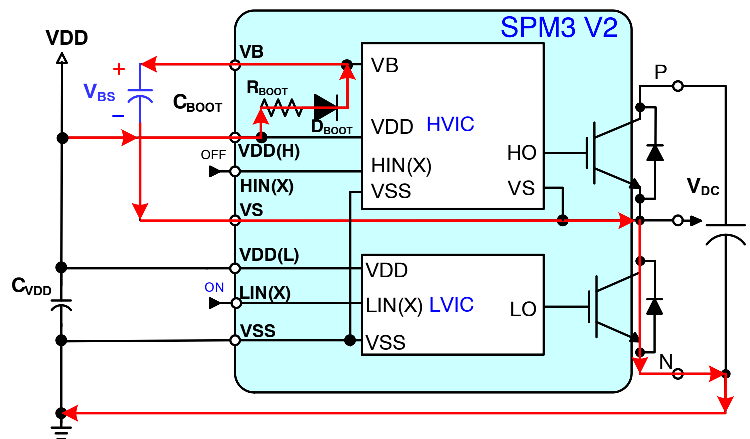


Figure 27. Current Path of Bootstrap Circuit

Selection of Bootstrap Capacitor Considering Initial Charging

Adequate on-time duration of the low-side IGBT to fully charge the bootstrap capacitor is required for initial bootstrap charging. The initial charging time (t_{charge}) can be calculated by:

$$t_{charge} = C_{BOOT} \times R_{BOOT} \times \frac{1}{\delta} \times \ln \frac{VDD}{VDD - VBS(Min.) - VF - VLS} \qquad \text{(eq. 5)}$$

Where:
VF = Forward voltage drop across the bootstrap diode;
VBS(Min.) = The minimum value of the bootstrap capacitor;
VLS = Voltage drop across the low-side IGBT or load; and
δ = Duty ratio of PWM.

Charging bootstrap capacitor is initially required before normal operation of PWM starts for the SPM 3 version 2 series. When the bootstrap capacitor is charged initially; VDD drop voltage is generated based on initial charging method, VDD line SMPS output current, VDD source capacitance, and bootstrap capacitance. If VDD drop voltage reaches UVDDD level, the low side is shut down and a fault signal is activated.

To avoid this malfunction, related parameter and initial charging method should be considered. To reduce VDD voltage drop at initial charging, a large VDD source capacitor and selection of optimized low-side turn-on method are recommended.

Figure 28 shows an example of initial bootstrap charging sequence. Once VDD establishes, VBS needs to be charged by turning on the low-side IGBTs. PWM signals are typically generated by an interrupt triggered by a timer with a fixed interval, based on the switching carrier frequency.

Therefore, it is desired to maintain this structure without creating complementary high-side PWM signals. The capacitance of VDD should be sufficient to supply necessary charge to VBS capacitance in all three phases. If a normal PWM operation starts before VBS reaches UVLO reset level, the high-side IGBTs cannot switch without creating a fault signal. It may lead to a failure of motor start in some applications. If three phases are charged synchronously, initial charging current through a single shunt resistor may exceed the over-current protection level.

Therefore, initial charging time for bootstrap capacitors need to be separated, as shown in Figure 29 if amount of initial current during short time should be minimized. The effect of the bootstrap capacitance factor and charging method (low-side IGBT driving method) is shown in Figure 28.

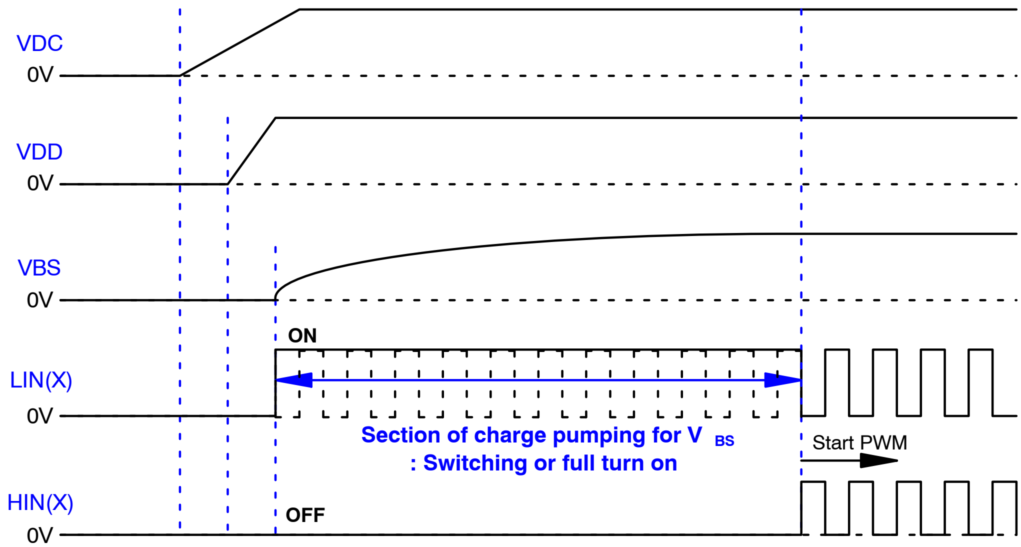


Figure 28. Timing Chart of Initial Bootstrap Charging

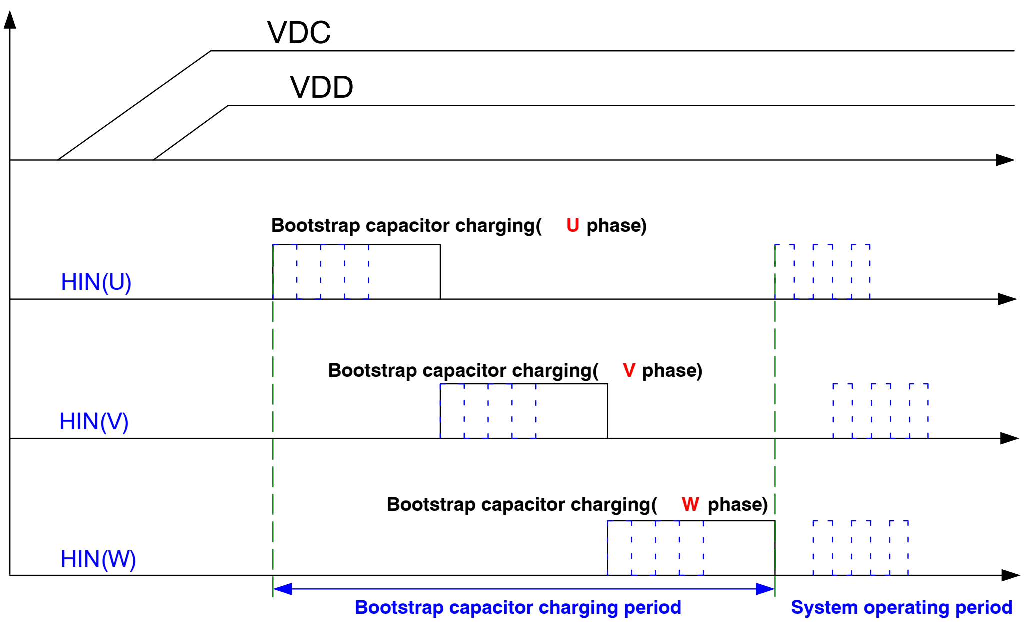


Figure 29. Recommended Initial Bootstrap Capacitors Charging Sequence

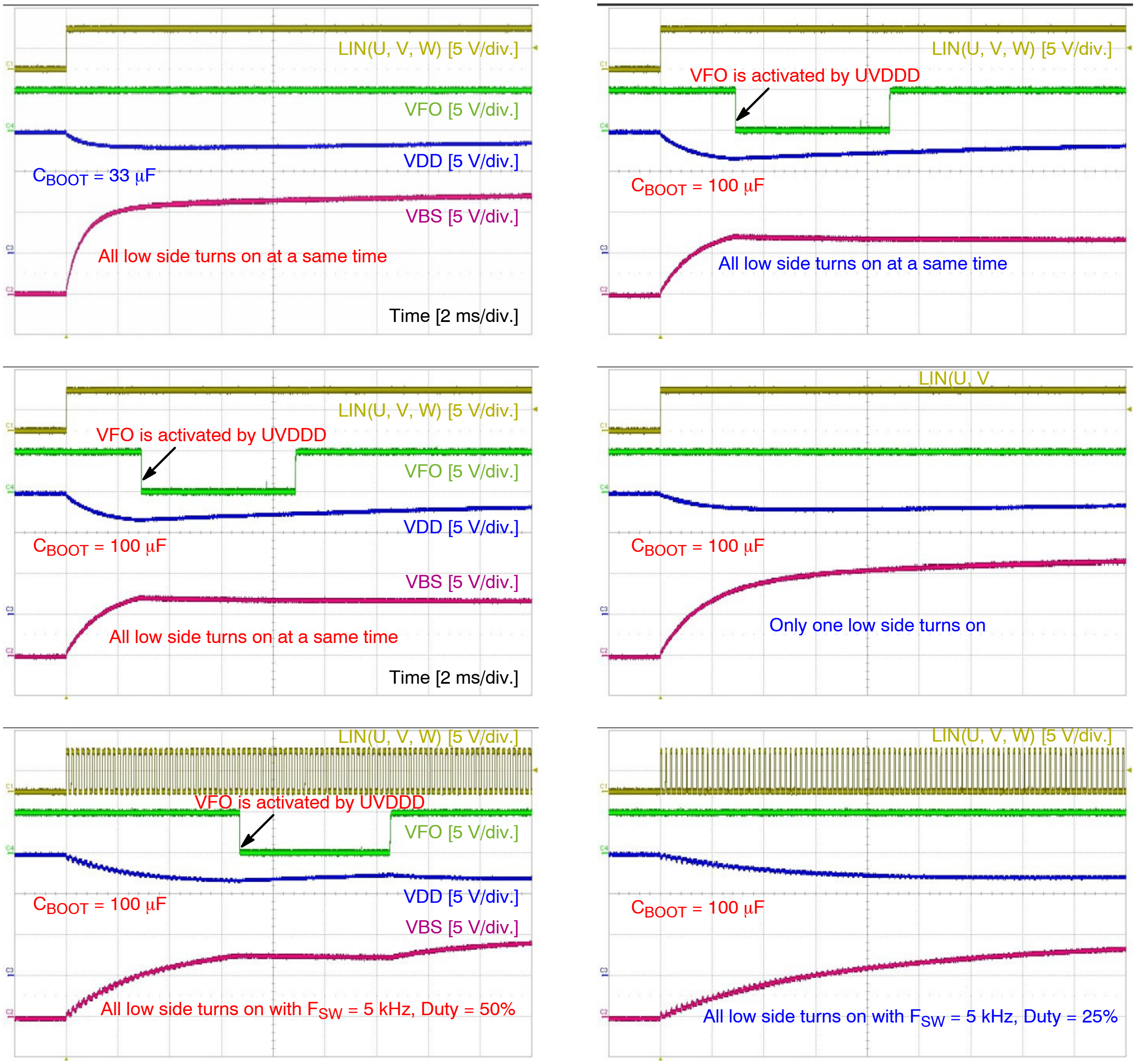


Figure 30. Initial Charging According to Bootstrap Capacitance and Charging Method (Ref. Condition: V_{DD} = 15 V / 300 mA, V_{DD} Capacitor = 220 µF, C_{BOOT} = 100 µF, R_{BOOT} = 20 Ω)

Selection of Bootstrap Capacitor Considering Operating

The bootstrap capacitance can be calculated by:

$$C_{BOOT} = \frac{I_{Leak} \times \Delta t}{\Delta VBS} \quad \text{(eq. 6)}$$

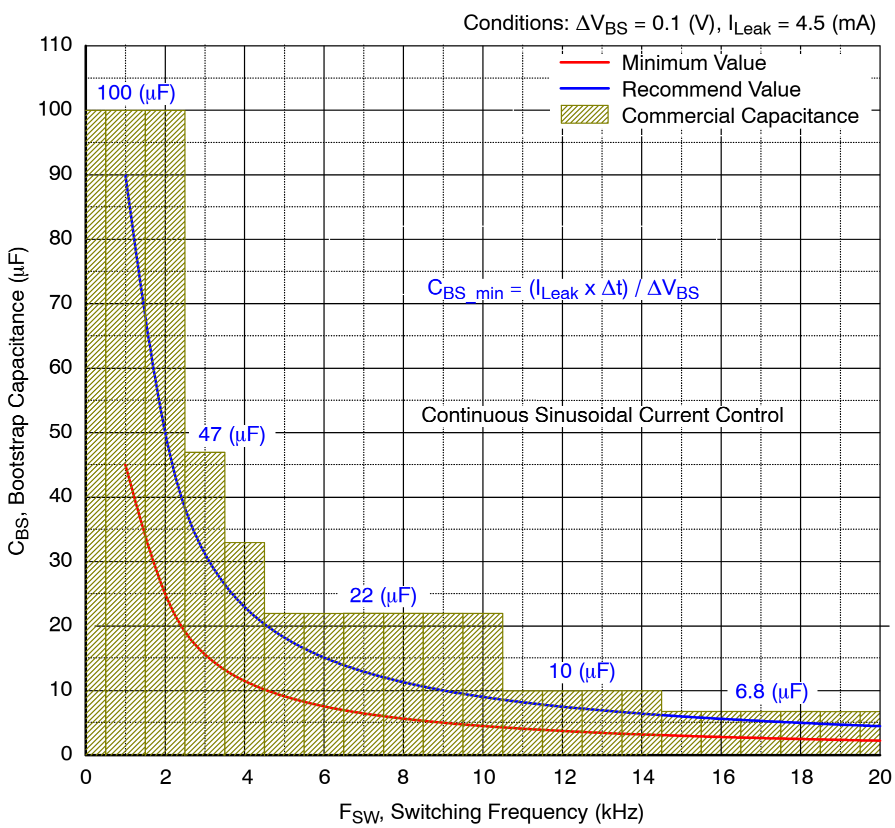
- Where:
- Δt: Maximum on pulse width of high-side IGBT;
- ΔVBS: The allowable discharge voltage of the C_{BOOT} (voltage ripple); and
- I_{Leak}: Maximum discharge current of the C_{BOOT}.

Mainly via the following mechanisms:

- Gate charge for turning the high-side IGBT on.
- Quiescent current to the high-side circuit in HVIC.
- Level-shift charge required by level-shifters in HVIC.
- Leakage current in the bootstrap circuit.
- C_{BOOT} capacitor leakage current (ignored for non-electrolytic capacitors).
- Bootstrap diode reverse recovery charge.

Practically, 4.5 mA of I_{Leak} is recommended for the 1200 V SPM 3 version 2 series. By considering dispersion and reliability, the capacitance is generally selected to be 2 ~ 3 times of the calculated one. The C_{BOOT} is only charged when the high-side IGBT is off and the VS(x) voltage is pulled down to ground.

The on-time of the low-side IGBT must be sufficient to ensure that the charge drawn from the C_{BOOT} capacitor to be fully replenished. This creates an inherent minimum on-time of the low-side IGBT (or off-time of the high-side IGBT).



NOTE:
13. The capacitance can be changed according to the switching frequency, capacitor type, and VBS voltage. The above result is a calculation example. So, this value can be changed according to the control method and lifetime of the component.

Figure 31. Capacitance of Bootstrap Capacitor on Variation of Switching Frequency

Based on switching frequency and recommended ΔVBS (Note 13).

I_{Leak}: circuit current = 4.5 mA (recommended value)
ΔVBS: discharged voltage = 0.1 V (recommended value)
Δt: maximum on pulse width of high-side IGBT = 0.2 ms (depends on application)

Built-in Bootstrap Circuit

When the low-side IGBT or diode conducts, the bootstrap diode (D_{BOOT}) supports the entire bus voltage. Hence, a diode with withstand voltage of more than 1200 V is recommended. It is important that this diode has a fast recovery (recovery time < 100 ns) characteristic to minimize the amount of charge fed back from the bootstrap capacitor into the VDD supply. The bootstrap resistor (R_{BOOT}) is to slow down the dVBS/dt and limit initial charging current (I_{charge}) of bootstrap capacitor.

Normally, a bootstrap circuit consists of bootstrap diode (D_{BOOT}), bootstrap resistor (R_{BOOT}), and bootstrap capacitor (C_{BOOT}). The built-in bootstrap circuit of SPM 31 version 2 product has special VF characteristics with bootstrap resistor. Therefore, only external bootstrap capacitors are needed to make bootstrap circuit.

The characteristics of the built-in bootstrap diode in the SPM 31 version 2 products are:

- Fast recovery diode: more than 1200 V / 2 A
- Resistive characteristic: equivalent resistor of approximately 20.0 Ω

Table 11 shows the specification of bootstrap circuit.

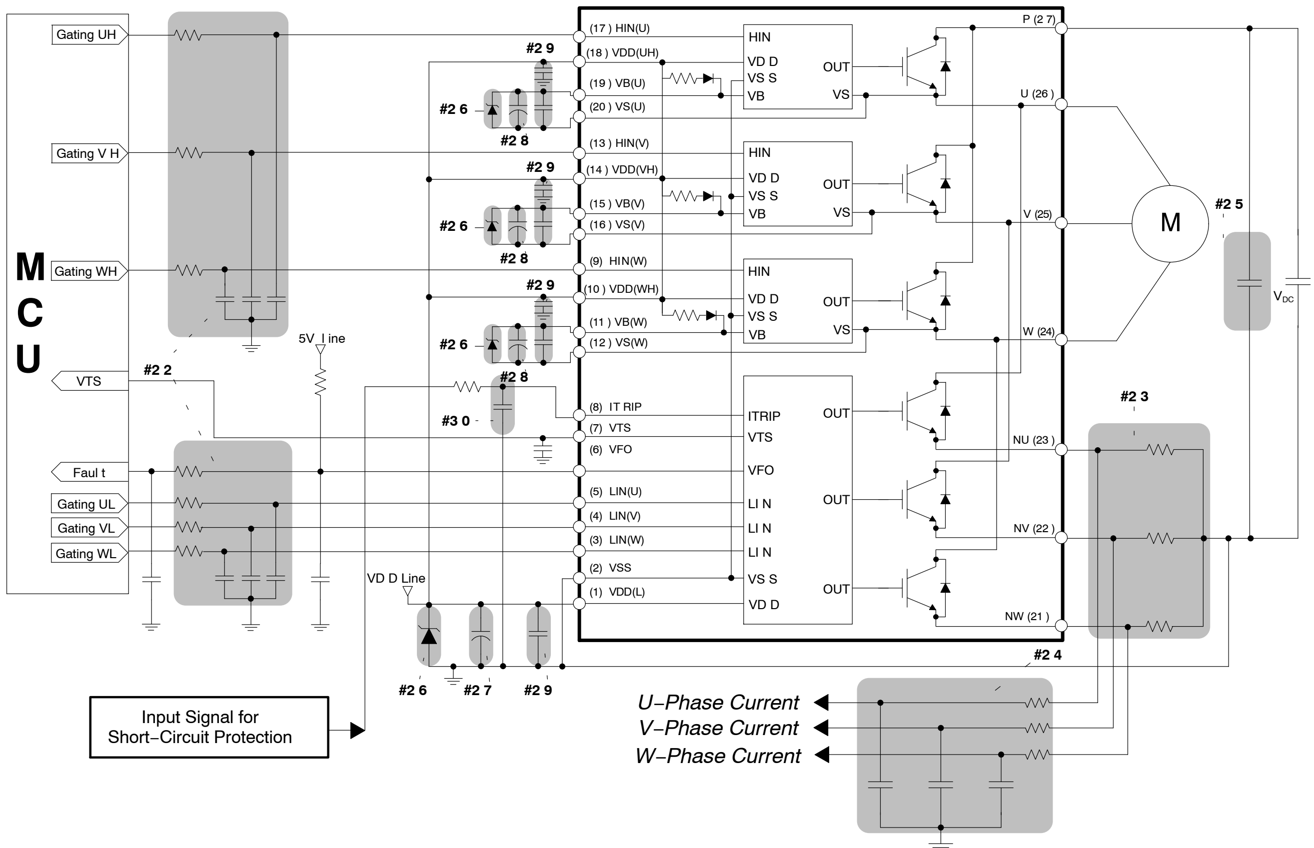
Table 11. SPECIFICATION FOR INTEGRATED BOOTSTRAP CIRCUIT

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_F	Bootstrap Diode Forward Voltage	IF = 10 mA, TJ = 25 °C (Including voltage drop by resistor)	0.7	1.05	1.4	V
	Bootstrap Diode Forward Voltage	IF = 100 mA, TJ = 25 °C (Including voltage drop by resistor)	2.3	3.3	4.3	
R_{BOOT}	Built-in Limiting Resistance		15	20	28	Ω

PRINT CIRCUIT BOARD (PCB) DESIGN

General Application Circuit Example

Figure 32 shows a general application circuitry of interface schematic with control signals connected directly to MCU. Figure 33 shows guidance of PCB layout for the 1200 V SPM 3 version 2 series.



To avoid malfunction, the wiring of each input should be as short as possible (less than 2−3 cm). Each capacitor should be mounted as close to the pins of the product as possible. VFO output is open-drain type. This signal line should be pulled up to the positive side of the MCU or control power supply with a resistor that makes IFO up to 1 mA. Please refer to Figure 26.

NOTE:

22. Input signal is active-HIGH type. There is a 5 kΩ resistor inside the IC to pull-down each input signal line to GND. RC coupling circuits should be adopted for the prevention of input signal oscillation. RC time constant should be selected in the range 50 ~ 150 ns. (Recommended R = 100 Ω , C = 1 nF)
23. Each wiring pattern inductance should be minimized (Recommend less than 10 nH). Use the shunt resistor of surface mounted (SMD) type to reduce wiring inductance. To prevent malfunction, wiring should be connected to the terminal of the shunt resistor as close as possible.
24. In the short-circuit protection circuit, please select the RC time constant in the range 1.5 ~ 2.0 μs. Do enough evaluation on the real system because short-circuit protection time may vary wiring pattern layout and value of the RC time constant.
25. To prevent surge destruction, the wiring between the snubber capacitor and the P & GND pins should be as short as possible. The use of a high-frequency non-inductive capacitor of around 0.1 ~ 0.22 μF between the P & GND pins is recommended.
26. The zener diode or transient voltage suppressor should be adopted for the protection of ICs from the surge destruction between each pair of control supply terminals (Recommended zener diode is 22 V / 1 W, which has the lower zener impedance characteristic than about 15 Ω).
27. VDD electrolytic capacitor is recommended around 7 times larger than VBS electrolytic bootstrap capacitor.
28. Please choose the VBS electrolytic bootstrap capacitor with good temperature characteristic.
29. 0.1 ~ 0.2 μF R-category ceramic capacitors with good temperature and frequency characteristics is recommended.
30. To prevent protection function errors, ITRIP capacitor should be placed as close to ITRIP and VSS pins as possible.

Figure 32. General Application Circuitry for 1200 V Motion SPM 3 Version 2

PCB Layout Guidance

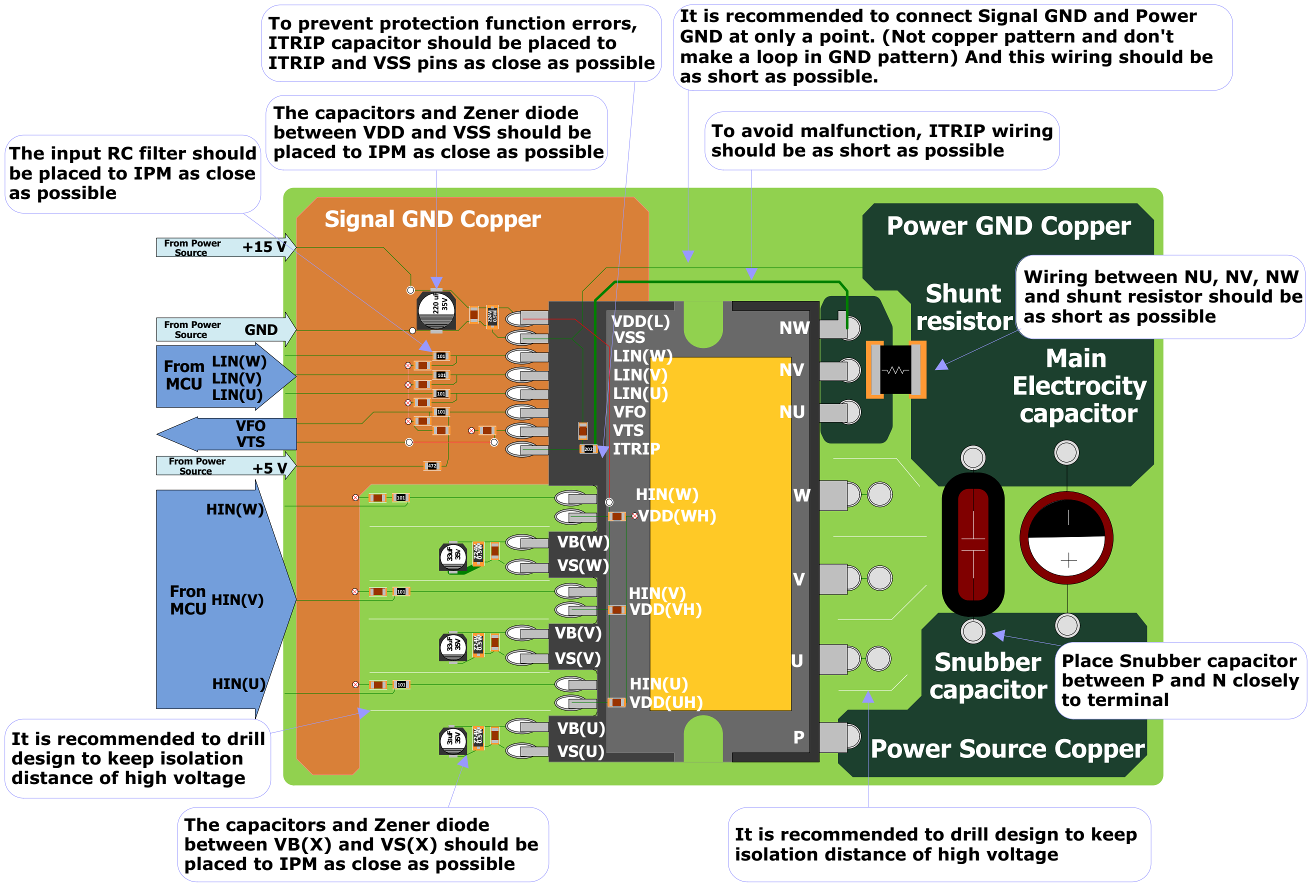
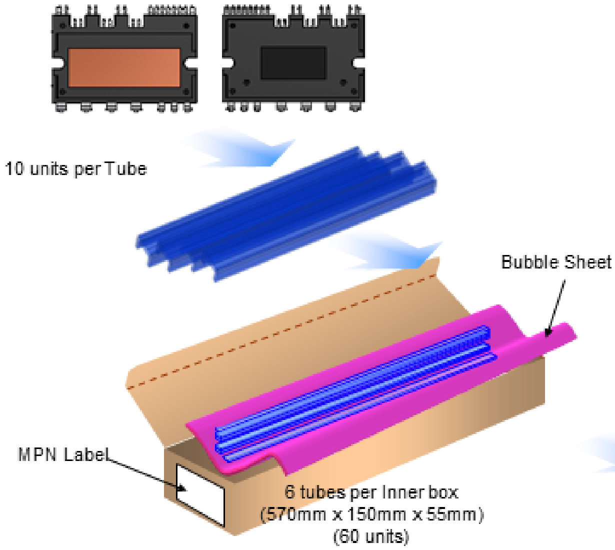


Figure 33. Print Circuit Board (PCB) Layout Guidance for SPM 3 Version 2 Series

REVISIONS				
REV	DESCRIPTION	ECN	DATE	NAME/SITE
1	RELEASE TO DOCUMENT CONTROL	N/A	31 JAN '13	KRPU
2	ADD SPM27-PA,QA,QB,RA,RB PKG	N/A	26 NOV'15	KRPU
3	REMOVE FAIRCHILD TEXT	N/A	13 MAR'19	KRPU

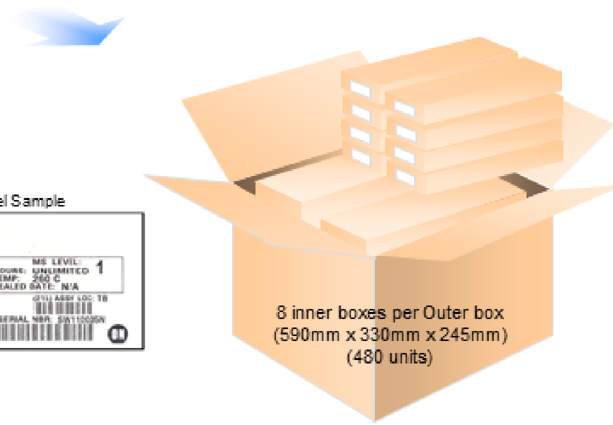
SPMCA-027 Tube Packing Configuration: Figure 1.0



Packaging Description:

SPMCA-027 parts are shipped normally in tube. The tube is made of PVC plastic treated with anti-static agent.These tubes in standard option are placed inside a dissipative plastic bubble sheet, barcode labeled, and placed inside a box made of recyclable corrugated paper. One box contains six tubes maximum (see fig. 1.0). And one or several of these boxes are placed inside a labeled shipping box which comes in different sizes depending on the number of parts shipped.

* SPMCC-027, SPMCD-027, SPMCE-027, SPMCF-027, SPMCG-027, SPMEA-027, SPMEC-027, SPMGA-027, SPMGC-027, SPMHA-027, SPMHC-027, SPMIA-027, SPMIC-027, SPMMA-027, SPMMB-027, SPMPA-027, SPMQA-027, SPMQB-027, SPMRA-027, SPMRB-027 packages also use this packing spec.



SPMCA-027 Packaging Information: Figure 2.0

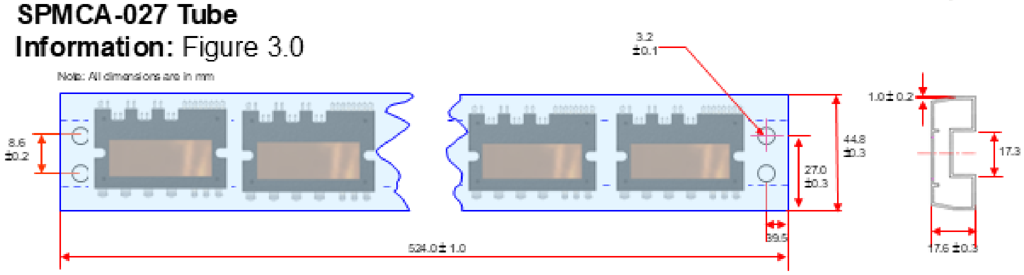
SPMCA-027 Packaging Information	
Packaging Option	Standard (no flow code)
Packaging type	Rail/Tube
Qty per Tube/ Inner Box	10
Inner Box Dimension (mm)	570x150x55
Max qty per Box	60
Outer Box Dimension (mm)	590x330x245
Max qty per Box	480
Weight per unit (gm)	-
Note/Comments	

Inner Box Barcode Label Sample

Sample MPN Label

SPMCA-027 Tube Information: Figure 3.0

Note: All dimensions are in mm



NOTES:

A : ALL DIMENSION ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED

B : DRAWING FIEL NAME : PKG-MOD27BAREV3

Figure 34.

REVISION HISTORY

Revision	Description of Changes	Date
0	Initial document version release.	4/29/2026
1	Updated MARKING DIAGRAM; updated Figure 34 per provided reference; removed Figure 32 and deleted corresponding references in text.	5/18/2026

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
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