Short-Circuit Protection Circuit Design for High Power Modules

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Introduction

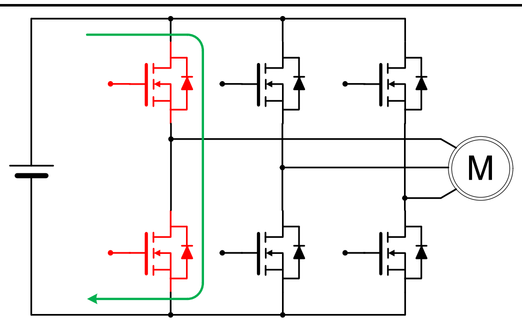
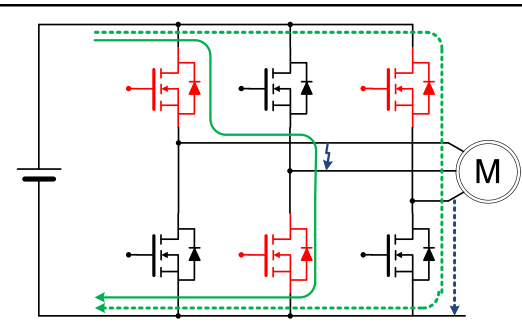
High-power semiconductors are an integral part of motor drives in industrial and automotive applications. As the power rating of motor drives is increasing, these semiconductors need to be designed to meet the ever-increasing demand for high efficiency and reliability. Silicon (Si) IGBT and Silicon Carbide (SiC) MOSFET power modules have played a pivotal role in traction inverter systems, but one challenging use case is that of short circuit events because the inherent short-circuit withstand time (SCWT) of these components is only a few microseconds. Therefore, during a short-circuit event, it is critical to protect the power device well within its withstanding time to prevent catastrophic failure due to electrical overstress (EOS). A traction inverter relies on the gate driver and its peripheral circuitry to detect the short-circuit event in the least amount of time and safely turn off the power device. This application note introduces the reader to the short-circuit fault scenarios encountered in a traction inverter system and illustrates power device protection strategies for both IGBT and SiC MOSFET. Lastly, circuit design guidance to implement short-circuit protection is also provided.

Short-Circuit Example in Traction Inverter

A three-phase traction inverter is used to convert DC input to three-phase AC output and is located between the high-voltage battery and the electrical load (motor). Short-circuit events in a traction inverter can occur due to various reasons like mechanical overload, miswiring, and uncontrolled PWM inputs. Table 1 categorizes short-circuit events in traction inverter under two categories:

1. Inverter shoot-through occurs due to the false turn-on of both high-side (HS) and low-side (LS) devices in one of the phase legs, thereby forming a direct short across the DC link through the power devices. This could happen either due to uncontrolled PWM input signals or electromagnetic interference (EMI).
2. Phase-to-phase and phase-to-GND short circuit could occur due to lifetime failure of insulation material when the traction inverter is operated out of its recommended operating conditions.

Table 1. SHORT-CIRCUIT EXAMPLES IN MOTOR SYSTEM

Shoot through in inverter.	Phase to Phase short-circuit. Phase to GND short-circuit.
	

Short-Circuit Characterization of IGBT and SIC MOSFET

One of the solutions for improving system efficiency and power density is to replace Si IGBT with SiC MOSFET because SiC MOSFET has several advantages relative to IGBT in a high voltage system. Because the critical electric field strength for SiC MOSFET is around ten times higher than that of a Si device, breakdown voltage can be achieved easily up to thousands of volts. For the same blocking voltage, the drift layer thickness is reduced by 90% in a SiC MOSFET as compared to its Si counterpart. Moreover, the saturation velocity in a SiC MOSFET is 2X that of silicon. Since drift layer thickness is directly proportional to on-state resistance and saturation velocity directly impacts current density and high-frequency switching capability, SiC MOSFET has lower switching and conduction loss and smaller die size as compared to Si IGBT for the same blocking voltage and current rating. Figure 1 shows that output characteristic curves for both Si IGBT (a) and SiC MOSFET (b). Si-IGBT curve is steep in the saturation region and flat when operating in active region, so it experiences high gain at gate voltage ranges higher than threshold. In contrast to Si devices, SiC MOSFET does not

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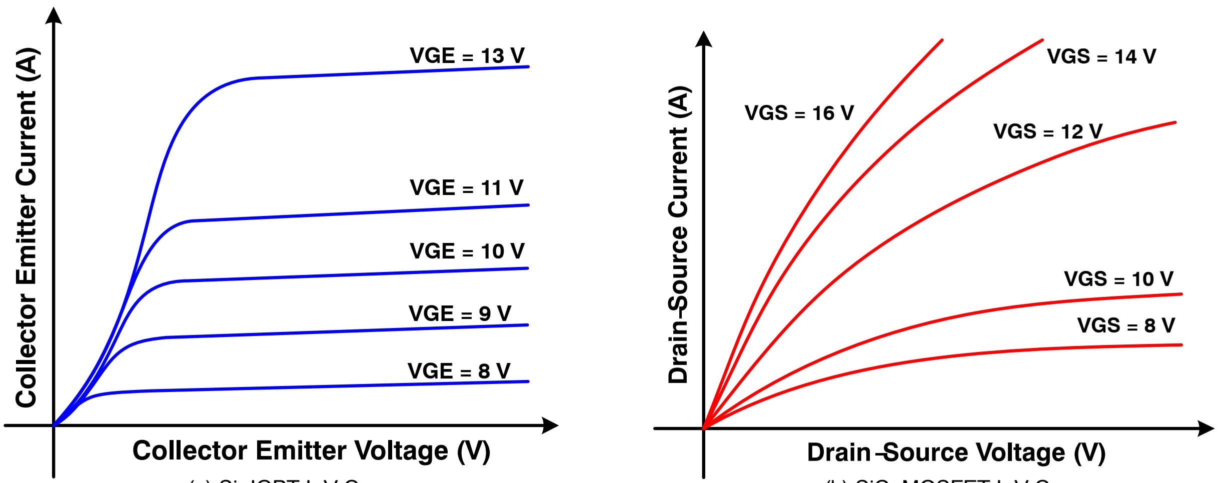
show a sharp transition between linear and saturation operating regions. Since SiC MOSFET have low trans-conductance, the only way to compensate low gain is to apply very high gate voltage to get low on-resistance and this causes the transition from linear to saturation to occur over a wider range of drain current. Figure 2 shows that short-circuit current for SiC MOSFET is much higher than IGBT with similar rating. The short-circuit current of SiC MOSFET rapidly increases to up to 10 times the nominal drain current causing higher short-circuit energy and rapid catastrophic failure. Therefore, to protect a SiC MOSFET with inherently lower short-circuit robustness and smaller die size, the gate driver must be specifically designed for reliable and fast detection of this event.



(a) Si−IGBT I−V Curve

(b) SiC−MOSFET I−V Curve

Figure 1. Output Characteristics of SiC MOSET and Si IGBT

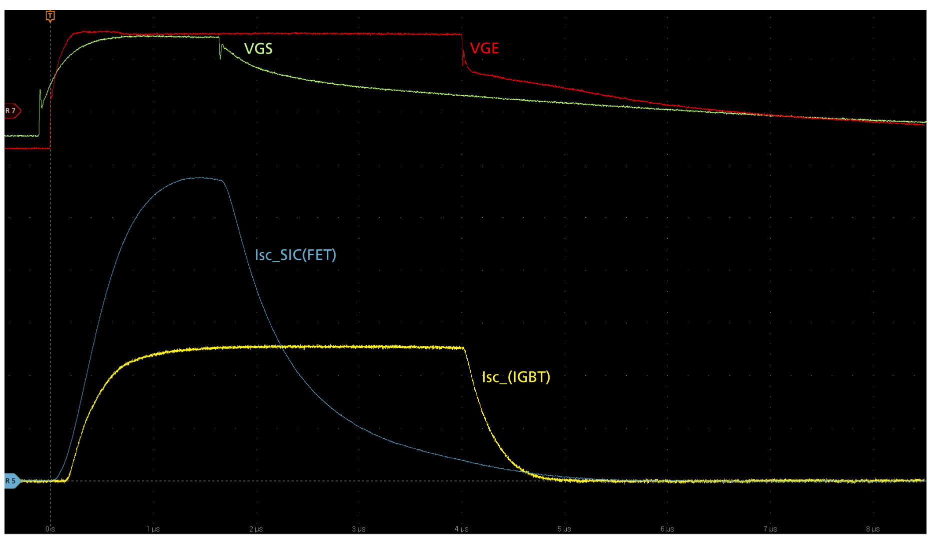
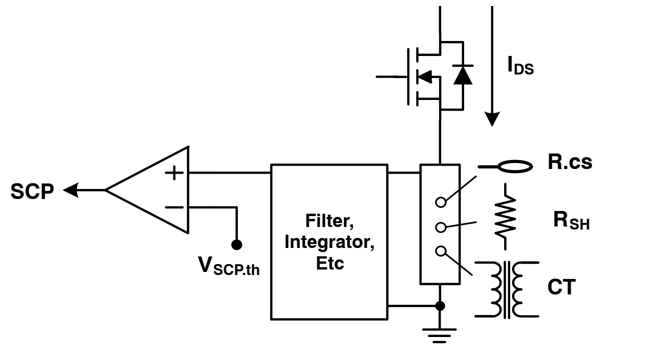
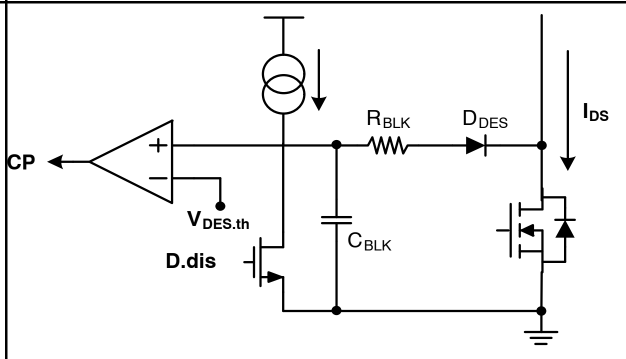


Figure 2. Waveform Comparison of SiC MOSET and Si IGBT in Short-Circuit Event

Short Circuit Protection Methods

onsemi NCV57100x series isolated gate drivers have short-circuit protection features that detect excessive current and protect the device from catastrophic failure. Table 2 shows the basic monitoring techniques used for short-circuit protection.

Table 2. DETECTION METHODS OF SHORT CIRCUIT-CURRENT

Current-Based Detection	VDS-Based Detection
	
Pros. Simple to implement and fast protection.	Pros. Simple to implement, no power loss, small, low cost.
Cons. Extra power loss, large, high cost.	Cons. Sensitive to high dv/dt noises.

Current Based Detection Method

In a current-based detection technique, current through the power device is monitored using current sensors like shunt resistor, current transformer, or Rogowski coil. Since the drain/collector current of the MOSFET/IGBT is monitored in real time, any abnormal rise in current (like short-circuit event) can be detected and prevented before it reaches critical magnitude. However, this would require complex circuitry on the gate driver board in addition to an integrated current sensor on the power module. The shunt resistance approach is easy to implement but generates additional power loss in high power inverter systems, so it is more commonly implemented in lower power systems. The shunt resistor connected in series with the DC bus needs to have a low temperature coefficient of resistivity and high accuracy. The current transformer and Rogowski coil have high noise immunity, but additional integrator and filter circuits are required to monitor short-circuit current with the gate driver because the circuit detecting the low voltage induced at magnetic coil output is galvanically isolated to the high-voltage busbar of the power module. Thus, magnetic field-based detection methods are bulky, complex, and relatively expensive.

V_{DS} Based Detection Method

The voltage-based detection technique has been used mainly in Si IGBT applications due to lower cost of implementation and relatively simple design. However, circuit design for both the response time for short circuit protection and the noise immunity from high dv/dt switching needs to be considered, especially when applied to SiC MOSFET. The voltage-drop across an IGBT (V_{CE}) or SiC MOSFET (V_{DS}) during conduction state is proportional to the forward current and device temperature. Once a short-circuit event occurs, the voltage drop will increase according to the device characteristic. Thus, this method of monitoring the voltage drop can be used to detect short circuit events with small size components as well as simple circuitry. This method is often called “Desaturation protection” or “Desat protection”. Although the voltage-based detection method is simple to understand, its implementation needs to be optimized for the device being monitored because the structure and I-V characteristic for Si IGBT and SiC MOSFET are different. The IGBT exhibits a saturation region at around 5 ~ 6 times the nominal current, while the SiC MOSFET exhibits much higher short-circuit current as compared to IGBT, and a rather gradual inflection point to the self-limiting current region as shown in Figure 2. Moreover, the smaller die size of SiC MOSFET further reduces the short circuit withstand time due to thermal properties. Therefore, the desaturation detection circuits used for IGBT must be optimized for SiC MOSFET to ensure proper operation.

Desaturation Protection Circuit Design for SiC MOSFET

The following considerations must be taken into account while designing a Desat protection circuit for SiC MOSFET:

1. The desaturation threshold voltage needs to be validated at high junction temperature because on-state resistance ($R_{DS(ON)}$) of SiC MOSFET is highly dependent on temperature.
2. Blocking diode, DDES needs to have fast reverse recovery time with low parasitic capacitances to minimize the noise caused by fast dV_{DS}/dt.
3. The blanking time t_{BLANK} to disable desaturation protection needs to be set to avoid false triggering under normal operation, as well as to protect the power device during a short-circuit event.
4. Soft turn-off and voltage clamping features are necessary to minimize the over voltage generated when short-circuit protection is triggered.

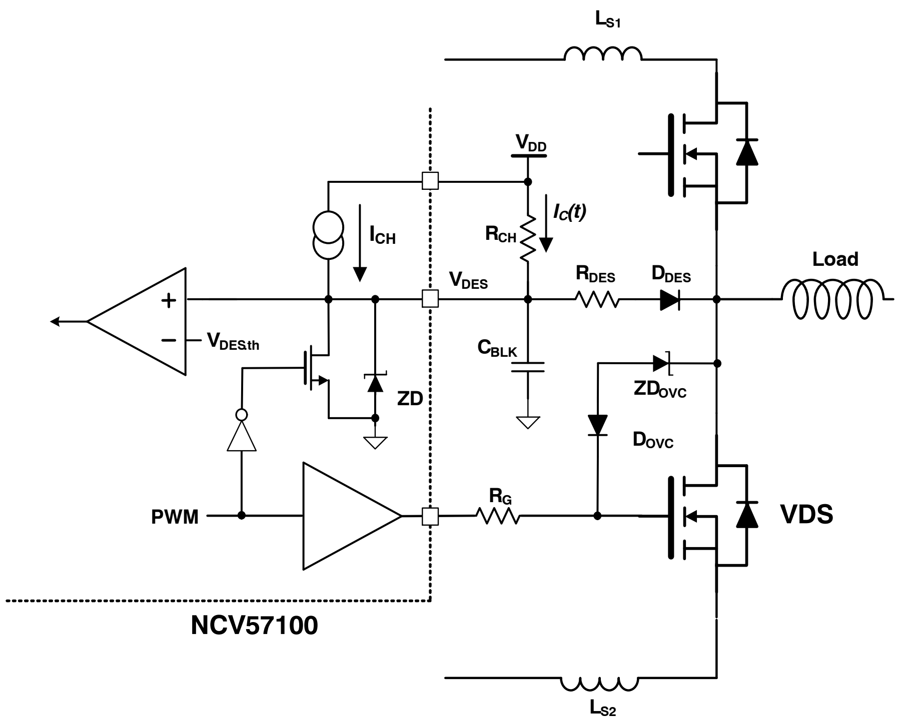


Figure 3. The Schematic for Desaturation Protection

A typical schematic of a desaturation protection circuit with **onsemi** gate driver NCV57100 is shown in Figure 3. Because the desaturation circuit consists of D_{DES}, R_{DES} and C_{BLK}, the blanking time t_{BLANK} and detection voltage V_{DES} can be calculated respectively as follows:

$$t_{BLANK} = \frac{C_{BLK} \times R_{CH} \times V_{DES}}{I_{CH}} \qquad \text{(eq. 1)}$$

$$V_{DES} = V_{DS} + V_F + V_R \qquad \text{(eq. 2)}$$

Although SiC MOSFET gate drivers have desaturation detection features, the internal current source charging the large capacitor C_{BLK} for guaranteeing noise immunity might be not high enough to trigger the desaturation protection within the proper reaction time. In case additional charging current is required for a faster short circuit response time, an external charging current $i_C(t)$ can be used by connecting R_{CH} between V_{DD} and C_{BLK}, and then $t_{BLANK.RCH}$ can be calculated with:

$$t_{BLANK.RCH} = -C_{BLK} \times R_{CH} \times \mathrm{Ln}\left(1 - \frac{V_{DES}}{V_{DD} + R_{CH} \times I_{CH}}\right) \qquad \text{(eq. 3)}$$

Note that the desaturation protection circuits should be designed so that V_{DES} goes below $V_{DES.th}$ during the turn-on transient period. Otherwise, desaturation protection might be triggered under normal operating conditions because V_{DES} is the sum of R_{DES} voltage drop V_R, D_{DES} forward voltage V_F and drain to source voltage VDS after leading edge blanking time t_{LEB}. In other words, VDS should be sufficiently low so that V_{DES} can be lower than $V_{DES.th}$ within t_{BLANK} during a normal turn-on transient. If VDS is not low enough within t_{BLANK}, the external gate resistance needs to be reduced to enhance gate driving current strength or R_{DES} needs to be reduced to reduce V_R the product of R_{DES} and total charging current $I_{CH} + i_C(t)$. C_{BLK} and R_{CH} are the main components to adjust blanking time, t_{BLANK}, but the circuit design with low capacitance is not recommended for noise immunity.

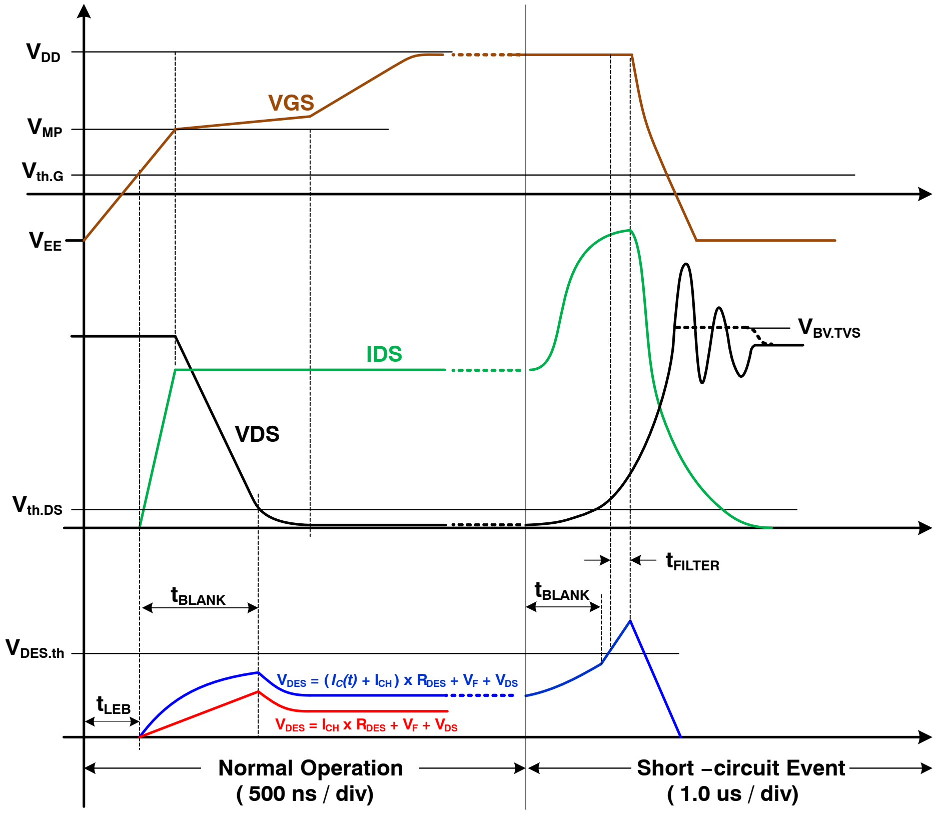


Figure 4. Timing Chart for Normal Operation and Fault Event

The Overshoot Voltage Caused by Hard Switching

With fast turn off switching (di/dt) of the power device and stray inductances L_{S1} and L_{S2} in the power loop as shown in Figure 3, overshoot voltage is expected during over-load or short-circuit events. Thus, conventional gate drivers with short-circuit protection have either soft turn-off control using constant current source or two-level turn-off control enabled after short-circuit protection is triggered. The soft turn-off method will increase the short-circuit energy due to longer on state. As mentioned previously, SiC device's short circuit withstand time is shorter than Si devices because the die size of SiC MOSFET is smaller compared to IGBT, thus the protection circuit needs to turn off the SiC device within allowable duration. However, hard switching at short-circuit condition will generate high drain voltage spikes as shown in Figure 3 and trade-off between fast short circuit response time and overshoot voltage suppression should be considered.

Over Voltage Clamping Using TVS

External TVS diode ZD_{OVC} and D_{OVC} in series connected between drain and gate terminal of the MOSFET in Figure 2 is activated when drain source voltage exceeds TVS breakdown voltage $V_{BR.TVS}$. TVS diode operates as a current source controlled by drain to source voltage and provides current to the gate terminal via D_{OVC}. This circuitry forces the device to conduction state, thereby clamping the overvoltage transient as shown in Figure 4. However, this will lead to extra power dissipation in the device during activation.

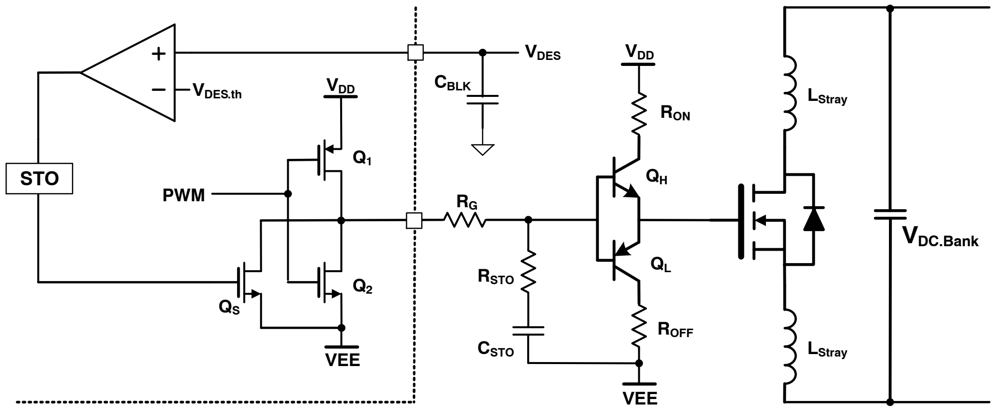


Figure 5. The Schematic of Soft Turn-off implemented with BJT Buffer

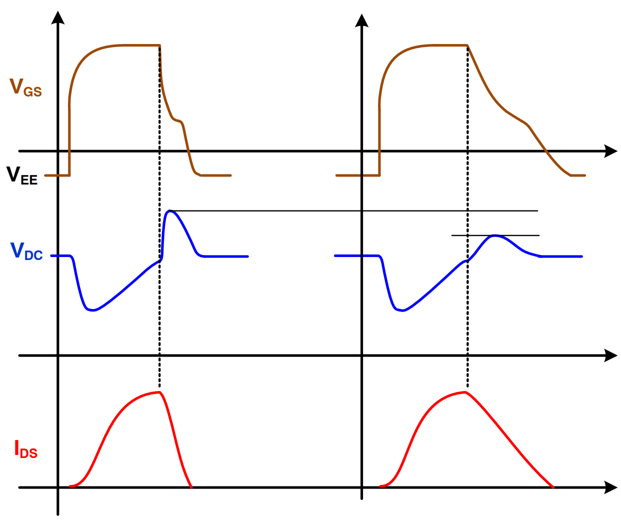


Figure 6. Waveform Comparison for Soft Turn Off Effect

Soft Turn Off Design with BJT Buffer Driver

In order to enhance the current capability driving power devices, extra BJT buffers might be used as shown in Figure 5. In this case, the soft turn-off features that gate driver provide are not easy to control BJT current gain (β) in buffer stage without the delay circuits because current gain in BJT buffers is changed in microampere range. When short-circuit protection in the gate driver is triggered, Q_S of N-MOS for soft turn off (STO) is activated and current with few of mA is flowed via Q_S and pnp transistor Q_L in buffer can turn off the power device quickly if there are not delay circuits. Therefore, an RC delay circuit consisting of R_{STO} and C_{STO} in parallel with base terminal of BJT buffer needs to be added to implement soft turn off functions. Generally, the current capability of PWM N-MOS in gate driver is high enough to quickly charge and discharge the delay circuit under normal operation while the current of Q_S enabled by triggering short circuit protection is much smaller than Q_2 of N-MOS and can implement soft turn-off function.

Conclusion

In this application note, short circuit examples in motor applications and detection methods have been described. The specific design method for fast short-circuit detection and suppressing the overshoot voltage caused by hard switching is provided for SiC MOSFET applications. Gate driver and peripheral circuits discussed in this document can be used with all Si and SiC power modules used in motor applications.

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