SiC Combo JFET Technical Overview

AND90336/D

Scope

onsemi has introduced the SiC JFET with exceptional RDSon*A performance. The SiC JFETs are ideal for applications requiring high current handling and slow switching speeds, such as solid−state circuit breakers and high current switching systems. Their performance benefits from SiC's superior material properties and JFET's efficient structure, which allow for lower on resistance and better thermal performance, making them suitable for applications that need multiple devices in parallel to manage high current loads efficiently.

For applications that require a normally off device, a low voltage Silicon MOSFET can be used in series with a normally-on SiC JFET to create a cascode configuration. In this setup, the SiC JFET handles high voltage, while the silicon MOSFET provides normally off behavior. This combination takes advantage of the high performance of the SiC JFET and the ease of control offered by the silicon MOSFET.

onsemi Combo JFET integrates a SiC JFET and a low voltage silicon MOSFET into a single package, meeting the requirement for a small footprint while delivering high performance with normally off behavior. Additionally, with various gate drive configurations, this Combo JFET offers advantages such as gate drive compatibility with silicon devices that have a 5 V threshold, enhanced reliability, and simplified speed control.

This document provides technical overview information for the **onsemi** SiC Combo JFET and covers static and dynamic performance. This application note also provides resource links to simulation models, assembly guidelines, thermal characteristics, reliability, and qualification documents.

Resource and Reference

[1] JFET Primer: AND90329/D
[2] JFET User Guide: UM70113/D
[3] **onsemi** SiC power solution central hub

Product Introduction

Combo JFET integrates a SiC FET and a low voltage silicon MOSFET into a single package, with both gates of the SiC JFET and the low voltage MOSFET accessible.

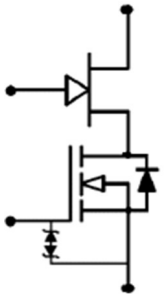

Figure 1. Combo JFET Structure

The Combo JFET offers several advantages due to the accessibility of both the JFET and low voltage MOSFET gates. These benefits include reduced $R_{DS(on)}$ with overdrive, simplified gate drive circuitry through external cascode connection, adjustable switching speed via JFET gate resistance, and the ability to monitor JFET junction temperature by measuring the gate-source voltage drop.

onsemi SiC Combo JFET Products

Table 1 and Figure 2 shows the Combo JFET products and available packages.

Table 1. COMBO JFET PRODUCT LIST

Part Number	RDS(on)	Package	Voltage Level
UG4SC075006K4S	6 mΩ	TO-247-4	750 V
UG4SC075005L8S	5 mΩ	TOLL	750 V
UG4SC075009K4S	9 mΩ	TO-247-4	750 V
UG4SC075011K4S	11 mΩ	TO-247-4	750 V
UG3SC120009K4S	9 mΩ	TO-247-4	1200 V

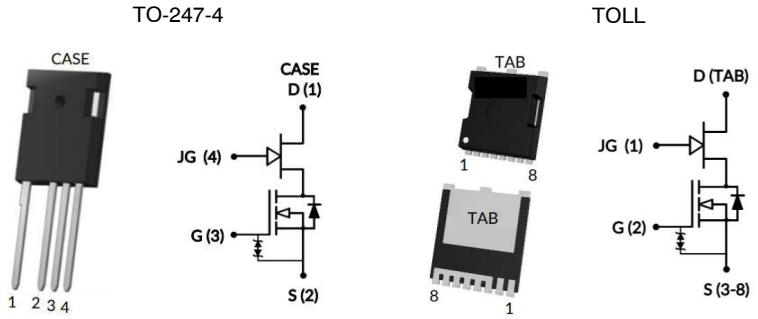

Figure 2. Combo JFET Packages and Schematics

Qorvo SiC Combo JFET Device Features and Benefits

Table 2 summarizes the features and benefits of **onsemi** SiC Combo JFET devices.

Table 2. onsemi SiC COMBO JFET FEATURES AND BENEFITS

Features	Benefits
Low $R_{DS(on)}$	Low loss
Peak Current (I_{DM})	High current ride through capability
Low $R_{\theta JC}$	Low T_J and better lifetime
Speed controllability	Ideal for circuit protection and multiple parallel application
Simple construction	Long lifetime without parameter shift

Static characteristics assessment in this section includes R_{DSON}, peak current (I_{DM}), $R_{\theta JC}$ (thermal resistance from junction to case). For circuit protection and multiple in parallel applications, dv/dt controllability is critical. The 750 V 5 mΩ TOLL package (UG4SC075005L8S) device is used as an example to assess static characteristics and dynamic characteristics.

Static Characteristics

onsemi's advanced SiC JFET technology enables superior electrical and thermal performance in the market as shown in Table 3.

Table 3. onsemi COMBO JFET KEY PARAMETERS

Specs	Value
Part Number	UG4SC075005L8S
I_D	120 A (T_C = 144 °C)
I_{DM} (T_C = 25 °C)	588 A
V_{DS} (max)	750 V
R_{DSON} (25 °C) with JFET $V_{GS} \geq 2$ V	5.0 mΩ
R_{DSON} (125 °C) with JFET $V_{GS} \geq 2$ V	8.3 mΩ
$R_{\theta JC}$ (max)	0.13 °C/W

onsemi Combo JFET has low $R_{DS(on)}$, high I_{DM}, and low thermal resistance.

Low $R_{DS(on)}$: **onsemi** Combo JFET devices utilize SiC JFET technology to achieve significantly lower $R_{DS(on)}$ per unit area ($R_{ds\cdot A}$). A flexible, externally configurable cascode structure (SiC Combo JFET) is employed to enable normally off operation, as illustrated in Figure 1. In **onsemi** SiC Combo JFET structure, the low voltage Si MOSFET contributes less than 10% of the total $R_{DS(on)}$.

Figure 3 shows the comparison of $R_{DS(on)}$ in TOLL package.

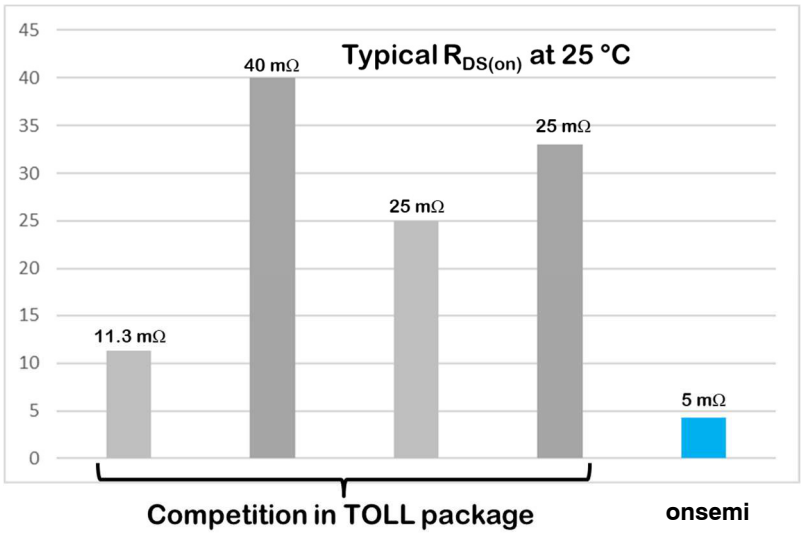

Figure 3. $R_{DS(on)}$ Comparison with TOLL Package

Higher I_{DM}: Peak current is crucial for circuit protection applications, with a high IDM SiC Combo JFET is ideal for such purposes. Circuit protection application require robustness and high current ride-through capability due to the specific operating conditions.

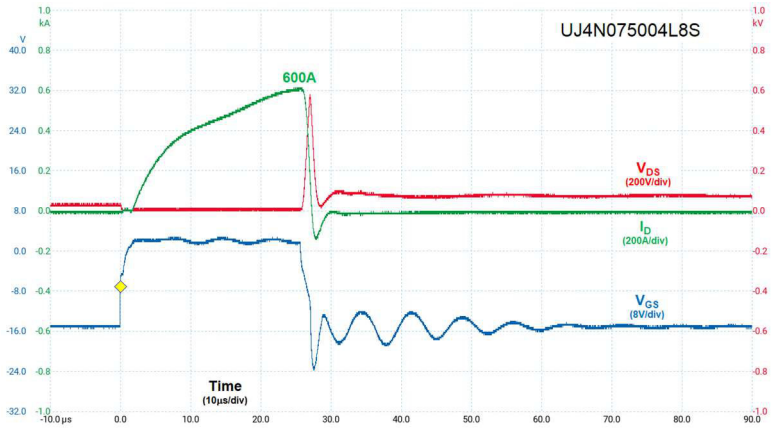

Figure 4. I_{DM} of JFET in Combo JFET Package

Low $R_{\theta JC}$: **onsemi** SiC Combo JFETs use silver sintering die attach to achieve six times better thermal conductivity at the interface comparing to most solder materials, resulting an equivalent or even lower junction-to-case thermal resistance with a smaller die size. A low $R_{\theta JC}$ helps maintain a lower junction temperature rise and ensures higher reliability.

Dynamic Characteristics

The excellent speed controllability achieved by tuning the JFET gate resistance in a Combo JFET configuration offers the following benefits:

- Reducing voltage overshoot by slowing down the turn-off speed enhances circuit protection, particularly for short circuit protection.
- Ease of paralleling, with an excellent trade-off between switching losses and dynamic current balance, is achieved.

Power Cycling

Reliability of power devices and lifetime assessment are crucial for enhancing system reliability and longevity, especially for emerging wide-bandgap (WBG) semiconductors (SiC, GaN, etc.). The primary failure modes of power devices are associated with thermomechanical fatigue. Powered thermal cycling tests are accelerated tests where the device under test (DUT) is frequently switched on and off, causing its junction temperature to cycle in a controlled manner. It applies thermo−mechanical stress to evaluate the reliability of the packaging (wire bond, die

attach, etc.). simultaneously, it applies electrical stress to both semiconductor die and packaging components (wire bond, lead, etc.), providing a more accurate simulation of temperature gradients encountered in actual applications compared to passive temperature cycling tests.

In a stacked structure, the Si MOSFET is positioned on top of SiC JFET, with the power source wires bonded to the source metallized layer of the Si MOSFET. Since silicon is less rigid than SiC, the thermo-mechanical stress during power cycling is significantly reduced, extending power cycling lifetime by up to 2X. Additionally, silver sinter die-attach is used for both layers, from Si MOSFET to SiC JFET and from SiC JFET to the thermal pad, to further enhance reliability compared to solder die-attach (widely used in today's SiC discrete devices). For more information on Si vs SiC power cycling performance please refer to this publication: *F. Hoffmann, N. Kaminski and S. Schmitt, "Comparison of the Power Cycling Performance of Silicon and Silicon Carbide Power Devices in a Baseplate Less Module Package at Different Temperature Swings," 2021 33rd International Symposium on Power Semiconductor Devices and ICs (ISPSD), Nagoya, Japan, 2021, pp. 175−178, doi: 10.23919/ISPSD50666.2021.9452242.*

Gate Control Method

There are two major control methods of Combo JFET for solid state circuit breaker application, quasi-cascode drive mode and direct drive mode.

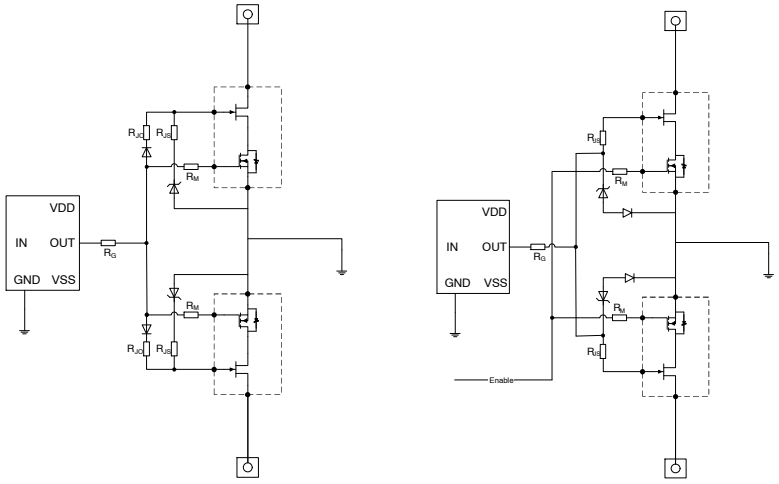

Figure 5. Combo JFET Drive Mode: Quasi-cascode Drive Mode (left) and Direct Drive Mode (right)

For high power switching mode application, besides the above two control methods shown in Figure 5, ClampDRIVE is developed and recommended. Or simplest gate control method with single JFET gate resistor to tune its switching speed, details see Figure 6.

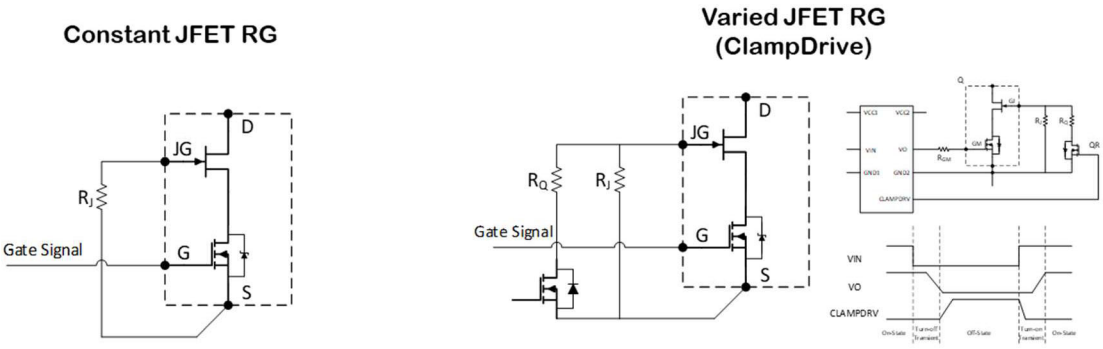

Figure 6. Control Methods of Combo JFET for Switching Mode Applications (Left: Constant JFET Gate Resistor, Right: ClampDRIVE)

Summary

onsemi SiC Combo JFETs offer the lowest $R_{DS(on)}$ and controllable switching speed to achieve superior efficiency and power density for circuit breaker and high-power low switching speed applications. It also provides Si level power cycling performance (reliability and lifetime) which is more than 2X better than SiC MOSFET.

EVB Available

onsemi provides two EVB options to support customer evaluation of the Combo JFET devices, one for circuit breaker application (common source) and one for high power switching mode application (half bridge). The EVBs are available through **onsemi** sales channel. Figure 7 and Figure 8 shows the pictures of Combo JFET circuit breaker and half bridge switching mode EVB.

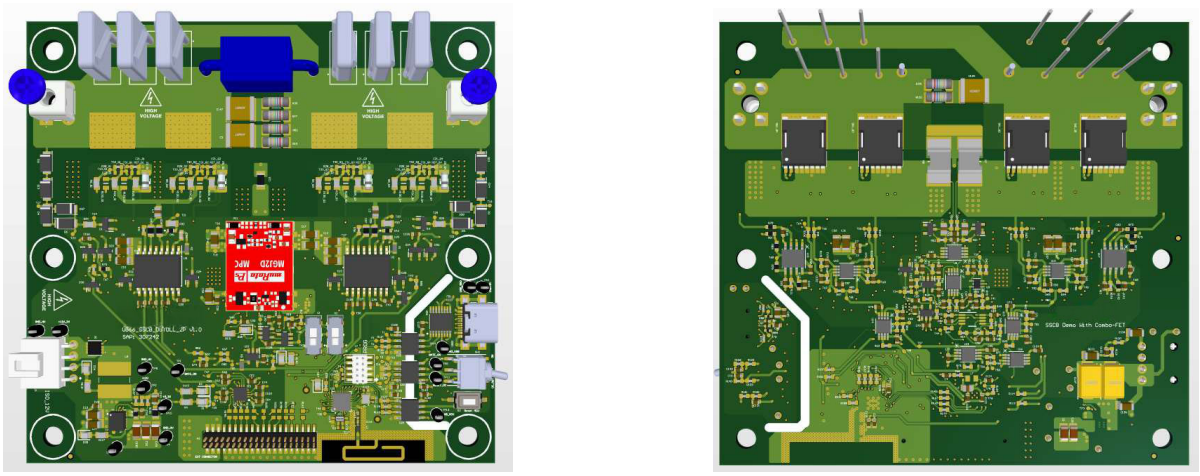

Figure 7. EVB for Circuit Breaker Application (Common Source)

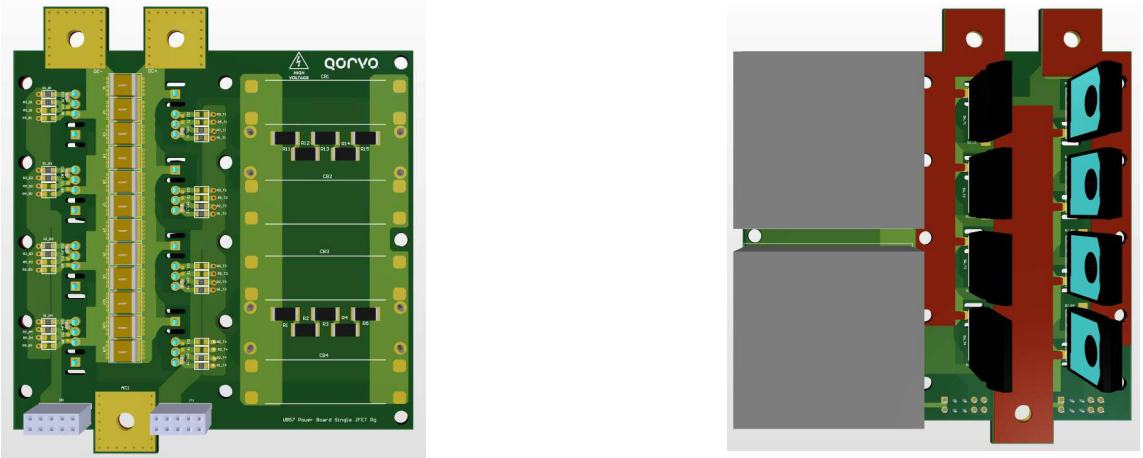

Figure 8. EVB for High Power Switching Mode Application (Half Bridge)

ADDITIONAL INFORMATION

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