Design of a Flyback Converter Using Source-Switched SiC JFET

AND90330/D

INTRODUCTION

The emergence of fast-switching wide-bandgap (WBG) devices has dramatically enhanced power density in a range of power conversion circuits such as active rectifiers, LLC resonant bridges, phase-shifted full bridges and dual active bridges to name a few. These circuits form the backbone of efficient AC-DC and DC-DC stages in automotive, solar inverters and data center power supplies, especially where high voltage and power density are key requirements.

Besides high-power density, SiC is also appealing for high-voltage (HV) applications such as energy storage, solar inverters and high-voltage traction. For these applications the DC voltage can be easily above 800 V dc, and AC voltages can range from 480 V ac to 530 V ac. Such high power and high voltage systems are typically controlled by circuitry that uses much lower voltages. Microprocessors, communication protocols, cooling fans and sensors require a variety of low voltages. A common approach to generating these voltages is with the flyback topology.

High-voltage input, medium power converters are also widely used in different industries such as LED lighting and laser power supplies. In these kinds of applications, galvanic isolation and high-voltage step down ratios from HV primary to low-voltage secondaries are usually required. Its isolation transformer makes the flyback converter a good candidate for these kinds of industrial applications.

onsemi has pioneered the introduction of SiC JFET-based cascode FETs with gate-driving compatibility with Si MOSFETs, IGBTs as well as SiC MOSFETs, based on the 5 V threshold voltage and wide-gate operating range of 20 V. These devices are inherently very fast switching.

In this application note, a discrete 1.7 kV SiC JFET together with a 30 V Si MOSFET in the cascode configuration is used as the main power switch in a flyback power supply. The JFET not only provides high-voltage blocking capability and efficiency but also simplifies the startup circuitry by doubling as the startup circuit's high-voltage pass element. [1][2][3] A design procedure for the flyback converter will be given. Simulated results are included to show the design concepts.

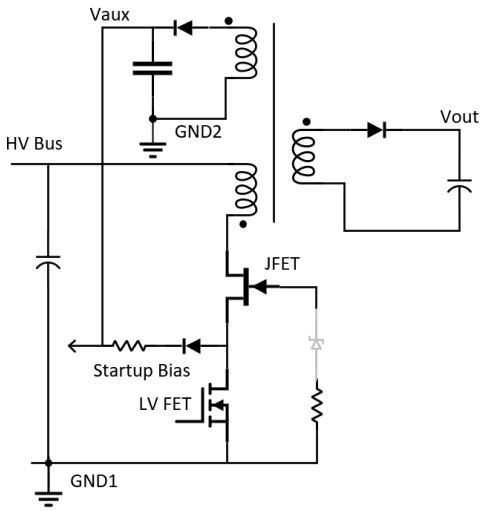

Figure 1. Source-switched Flyback Converter with JFET Doubling as Start-up Power Source

SOURCE-SWITCHED FLYBACK CONVERTER USING A HV JFET

Figure 1 is a simplified schematic of the flyback converter that is implemented in this application note. In this example, an input voltage of up to 1000 V generates regulated 12 V 60 W low voltage output.

A JFET cascoded with a Low Voltage MOSFET (LV MOS) is used as the main switch. This combination offers low $R_{DS(on)}$ and fast switching. The source of the JFET is connected to the controller IC's V_{CC} pin to supply starting power. Output voltage of an auxiliary winding (V_{aux}) is used to power the controller IC after starting. If the output voltage (V_{out}) falls in the controller IC's bias voltage range and input-output galvanic isolation is not required, bias power after starting can be taken directly from the output winding.

After powering up, the D-S voltage of the LV MOS (V_{ds_LV}) charges up quickly and stays at a level approximately equal to the inverse of the JFET gate threshold ($|V_{jgs\_th}|$). The supply voltage of the controller IC

(V_{CC}) is regulated at this voltage until the controller starts to drive the gate of the LV MOS. Therefore, for a successful starting, $|V_{jgs\_th}|$ needs to be higher than the minimum V_{CC} required to start. If this requirement is not satisfied, a zener can be used in the JFET gate path to lift up V_{ds_LV} and regulate the starting V_{CC} at a higher level.

After the controller starts to switch, the auxiliary winding voltage V_{aux} starts to build up. This voltage is Or'ed to V_{CC} and starts to supply the bias power once it is higher than V_{ds_LV}. To avoid bias power draw from the JFET source after starting, V_{aux} needs to be designed at a level higher than $|V_{jgs\_th}|$ with certain margin.

In many applications the main output needs to be galvanically isolated from the primary side. In those cases, either an opto-isolator must be used in the output voltage feedback path, or primary-side regulation should be used. To focus on power stage design, a non-isolated feedback loop is used with cycle-by-cycle peak current control (PCC) in this design example.

Under a certain input/output working condition, a flyback converter can be designed to work in either Discontinuous Conduction Mode (DCM), Critical Conduction Mode (CrM) or Continuous conduction Mode (CM). It is common practice to design the converter in CrM mode for the working condition desired for optimal operation. In this application note, the converter is designed to work in CrM when the converter is fully loaded, and input voltage is at the lower end of its nominal range. It goes to DCM when operating at higher input voltages and/or lighter loads and enters CM mode when operating in lower input voltages and full load.

POWER STAGE DESIGN

Step 1. Determine the switching Frequency (F_{SW}) and Duty Cycle for CrM mode (D_{CrM})

In general, switching frequency is dictated by the size and efficiency requirements of a design. The higher the frequency, the smaller the passive component sizes, and hence lower costs in general. On the other hand, higher F_{SW} increases power losses in switching devices and magnetic components. Therefore, while the decision on this parameter is somewhat arbitrary, a compromise needs to be made according to the design constraints. Medium to low power flyback converters typically switch in the range of a few hundred kilohertz. With tight constraints on competing design requirements, a few design iterations may be necessary for this parameter selection.

A main consideration of duty cycle selection for CrM is the energy transfer balancing in each switching cycle. Since primary inductive energy is built up in the turn-on cycle and released in the turn-off cycle, it makes sense to use a balanced duty cycle of 0.5 for the CrM operation.

Step 2. Determine the Maximum Primary Inductance

The maximum L_{pri} can be found by applying Equation 1 to CrM operation at nominal minimum voltage ($V_{in\_nom\_min}$):

$$P_{in} = \frac{P_o}{\eta} = V_{in}\frac{I_{pp1}}{2}D_{CrM} = \frac{D_{CrM}{}^2 V_{in}{}^2}{2L_{pri}F_{SW}} \qquad \text{(eq. 1)}$$

Where P_o is the total output power, η is the assumed efficiency, I_{pp1} is primary peak-peak current, L_{pri} is the flyback transformer primary winding inductance, and F_{SW} is the switching frequency.

The maximum L_{pri} can be found from Equation 1:

$$L_{pri} = \frac{\eta D_{CrM}{}^2 V_{in\_non\_min}{}^2}{2F_{SW}P_{out}} \qquad \text{(eq. 2)}$$

With an L_{pri} equal or smaller than that calculated from Equation 2, the converter operates in CM or CrM under full loading and input voltage up to $V_{in\_nom\_min}$, and DCM under other working conditions.

Step 3. Determine the Maximum Transformer Turns Ratio

Ignore the voltage losses in the output rectification diode and resistive elements, input-output voltage regulation under CrM can be represented by Equation 3.

$$\left(1 - D_{CrM}\right) N_{ps} V_{out} = D_{CrM} V_{in\_nom\_min} \qquad \text{(eq. 3)}$$

Where N_{ps} is the transformer turns-ratio from primary winding to the main output winding.

Step 4. Find the Currents and Voltages For Main Component Selections

When the converter works in CM or CrM mode, the primary currents can be calculated with the equations below.

Average input current during the turning on cycle:

$$I_{avg1(on)} = \frac{P_{out}\left(V_{in} + N_{ps}V_{out}\right)}{\eta V_{in} N_{ps} V_{out}} \qquad \text{(eq. 4)}$$

Peak-peak current:

$$I_{pp1} = \frac{V_{in} N_{ps} V_{out}}{L_{pri} F_{SW}\left(V_{in} + N_{ps}V_{out}\right)} \qquad \text{(eq. 5)}$$

Primary peak current:

$$I_{pk1} = I_{avg(on)} + \frac{I_{pp1}}{2} \qquad \text{(eq. 6)}$$

The corresponding primary RMS current:

$$I_{rms1} = \sqrt{D}\sqrt{I^2_{avg1(on)} + \frac{I^2_{pp1}}{12}} \qquad \text{(eq. 7)}$$

Duty cycle D is 0.5 when working in CrM, and calculated by equation below when it is operating in CM mode:

$$D_{cm} = \frac{N_{ps}V_{out}}{V_{in} + N_{ps}V_{out}} \quad \text{(eq. 8)}$$

Secondary currents can be calculated by reflecting primary currents to secondary side:

$$I_{avg2(off)} = I_{avg1(on)}N_{ps} \quad \text{(eq. 9)}$$

$$I_{pp2} = I_{pp1}N_{ps} \quad \text{(eq. 10)}$$

$$I_{pk2} = I_{avg2(off)} + \frac{I_{pp2}}{2} \quad \text{(eq. 11)}$$

$$I_{rms2} = \sqrt{(1 - D)}\sqrt{I^2_{avg2(off)} + \frac{I^2_{pp2}}{12}} \quad \text{(eq. 12)}$$

The maximum voltage stress added to the power switch happens when the DC input voltage is at the maximum level.

$$V_{ds\_max} = V_{in\_max} + N_{ps}V_{out} \quad \text{(eq. 13)}$$

Turn-on current spikes during switching transients also need to be carefully evaluated, as it is a major contribution factor to the turn-on switching losses. It can also disturb the peak current detection of the controller. When the spike duration is wider than the controller's Leading-Edge Blanking (LEB) time, the controller will turn off the main switch before primary current reaches the peak level set by the feedback loop. A major part of the turn-on current spike comes from the transformer primary winding's parasitic capacitance. This capacitance needs to be minimized in transformer design. Charging and discharging currents of snubber capacitances is another contributing source to this spike current. Therefore, the capacitances in the snubbers should be kept at a minimum level, no more than necessary for turn-off dv/dt and voltage overshoot controls.

The LV MOS cascaded with JFET turns the JFET on and off and conducts above currents the same way as the JFET. Its current rating needs to meet all the worst-case requirements. Its voltage rating needs to be higher than the JFET gate threshold voltage with significant margin. Typically, 30 V MOSFET is used.

During the turn-off transient, steady state V_{ds_LV} is just above the JFET gate threshold voltage $|V_{jgs\_th}|$. But if the JFET is being turned off too slow, the V_{ds_LV} can be charged to a level higher than the rated voltage of the LV MOS, and repetitive avalanches happen. To avoid this repetitive avalanche, the turning off transient of the LV MOS should be designed slower than that of the JFET by properly sizing the gate resistors of the two switches. Otherwise, a repetitive avalanche rated LV MOS need to be used, or an external device like an appropriately rated Zener can be added in parallel with the LV MOS to clamp the V_{ds_LV} below its avalanche voltage during the turning off transients.

STARTUP CIRCUIT AND CONTROLLER DESIGN

One of the unique advantages of the cascode switch is its simplification of the converter's startup circuit. In a typical high-voltage startup circuit, a second high-voltage circuit (usually a resistance string that takes power directly from the HV bus) is needed to provide the initial power to the controller. This high-voltage circuit continues to dissipate power after the converter is started. Using a high-voltage JFET in the cascode configuration, that startup circuit and associated power loss can be eliminated.

onsemi's NCV12711 is used to control the power switch in this design. It is a Peak Current Controller (PCC) and capable of cycle-by-cycle current limiting. Due to its skip-cycle mode, the output can be regulated in very light loading conditions with minimum power loss in the converter.

NCV12711 starts to switch once its V_{CC} reaches 4 V. This is lower than the threshold voltages of most high voltage JFETs. Therefore, the converter can be started without using a Zener in the JFET gate path to generate starting V_{CC} higher than $|V_{jgs\_th}|$. However, gate voltage of 4 V may be too low to drive many LV MOS on. To address this concern, the UVLO pin of the IC can be used to override this minimum V_{CC} and ensure that the controller only starts switching when it's V_{CC} reaches a level higher than 4 V (but still less than $|V_{jgs\_th}|$). This will be demonstrated in the simulation model in a later section.

Another consideration is the maximum current draw of the controller's V_{CC} pin before it starts switching. It needs to be smaller than the current the JFET can supply when V_{CC} is biased at the level for starting. From the data sheet of this controller IC, the $I_{CC(max)}$ to start switching is 4 mA. The JFET selected for this application needs to supply at least this current before V_{ds_LV} passes its gate threshold and completely turns it off.

SNUBBER DESIGN CONSIDERATIONS

Snubbers are usually needed in a flyback converter due to the unavoidable leakage inductances of the flyback transformer and parasitic inductance in the power loops. Traditionally an RCD snubber is used to capture and dissipate the energy in the leakage of the transformer primary winding during turning off, and an RC snubber is used across the secondary rectifier diode to dampen the turning on current ringing.

The primary RCD snubber is effective in clamping the voltage spikes caused by the transformer leakage inductance. However, once the capacitor in the snubber is charged up, it does not change the turn-off slew rate (dv/dt) of the main switch.

The secondary RC snubber helps dampen the current ringing during the primary switching on cycle. With high leakage inductance of the transformer, this RC snubber is more effective when put in the primary side, in parallel with the transformer winding or the RCD diode. This RC snubber adds turning on current and hence the switching loss. Therefore, capacitance used in this snubber needs to be minimum, just enough to dampen the current ringing and provide the controller IC CS pin with a clean ramping up current signal.

Besides above snubbers, another RC snubber directly across the cascaded switching device may also be necessary. The purpose of this device RC snubber is to:

- control the V_{ds} turning off overshoot,
- dampen the V_{ds} ringing after turning off transient,
- and reduce the V_{ds} turning off dv/dt.

In HV flyback applications, the turning off current is usually low. If the loop inductance is minimized too, this device RC snubber may not be necessary. Decision needs to be made together with the test results after the design is implemented. In case this device snubber is used, RC parameters need to be carefully sized as it adds extra turning on loss to the main switch and the resistor itself. CJFET user guide [5] can be referenced for initial selection of the RC parameters.

DESIGN EXAMPLE

Key design specifications for the example flyback converter are given below:

- V_{in}: Nominal range 200 V to 800 V, working range 30 V to 1000 V;
- V_{out}: 12 V;
- P_{out}: 60 W;
- $V_{o\ (Aux)}$: 12 V;
- P_{aux}: 2 W

Selecting a switching frequency of 150 kHz and duty cycle of 0.5, and assuming a 95% efficiency at input voltage of 200 V, the maximum primary inductance is found using Equation 2:

$$L_{pri} = \frac{0.95}{2}\frac{0.5^2 \times 200^2}{(60 + 2) \times 150k} = 511\ \mu H \qquad \text{(eq. 14)}$$

Use Equation 3, the maximum turns-ratio from primary to the main output is found to be:

$$N_{ps} = \frac{0.5 \times 200}{(1 - 0.5) \times 12} = 16.7 \qquad \text{(eq. 15)}$$

To avoid fractional turns of the auxiliary winding, an integer number 16 is selected in this design. The transformer turns-ratio is:

$$\text{Npri:Nsec:Naux} = 16{:}1{:}1 \qquad \text{(eq. 16)}$$

The magnetizing inductances of the output and auxiliary windings are:

$$L_{sec} = L_{aux} = \frac{511}{16^2} = 2\ \mu H \qquad \text{(eq. 17)}$$

The maximum voltage stress on the power switch happens when it is turned off:

$$V_{ds\_max} = 1000 + 16 \times 12 = 1192\ V \qquad \text{(eq. 18)}$$

From Equations 4 to 7, the primary currents when the converter is working in CrM with 200 V input and full load are calculated:

- $I_{avg1(on)(200Vin)}$ = 0.66 A;
- $I_{pp1(200Vin)}$ = 1.28 A;
- $I_{pk1(200Vin)}$ = 1.31 A;
- $I_{rms1(200Vin)}$ = 0.54 A.

The secondary currents are:

- $I_{avg2(off)\ (200Vin)}$ =10.56 A;
- $I_{pp2(200Vin)}$ = 20.48 A;
- $I_{pk2(200Vin)}$ = 20.38 A;
- $I_{rms1(200Vin)}$ = 8.55 A

Since lower input voltage results in higher current, the currents for the minimum input voltage also need to be calculated as the worst-case condition.

Using Equation 8, duty cycle when input voltage is minimum at 30 V is:

- D30 V_{in} = 0.87

And the currents are:

- $I_{avg1(on)(30Vin)}$ = 2.47A;
- $I_{pp1(30Vin)}$ = 0.34A;
- $I_{pk1(30Vin)}$ = 2.64 A;
- $I_{rms1(30Vin)}$ = 2.30 A.

The secondary currents are:

- $I_{avg2(off)(30Vin)}$ = 39.5 A;
- $I_{pp2(30Vin)}$ = 5.28 A;
- $I_{pk2(30Vin)}$ = 42.14 A;
- $I_{rms1(30Vin)}$ = 14.52 A

These calculated results confirmed the maximum current stresses happen at the very low input voltage of 30 V and full load.

The maximum V_{DS} across the power switch was calculated to be 1192 V. With 20% margin, a switching device of at least 1430 V should be used. The RMS drain current was calculated at 2.3 A and repetitive current spikes at 2.64 A. This current peak is the maximum sensed by the

controller CS pin and used to determine the time instant to turn off the switch. In actual circuits the turning on transient spikes may be much higher and need to be checked by testing.

Controller NCV12711 quiescent current draw is about 4 mA. With some margin for current bleeding in the starting circuit, the starting current supplied by the JFET needs to be greater than 5 mA.

Based on the above calculations, **onsemi**'s 1700 V/6.8 A JFET UF3N170400B7S is a good fit for this application. Its V_{jgs_th} is about 9 V. It can supply the starting current at this gate voltage in the full operating temperature range, as shown in Figure 2. Leave some margin for the V_{jgs_th} variations and design the controller UVLO voltage at 7.0 V, the converter can be started by this JFET source voltage.

onsemi's 30 V MOSFET NTMD4N03R2 is used for the LV mosfet in the simulation. With the gate resistor values showing in Figure 3, V_{ds_LV} is well below 30 V, and no repetitive avalanche observed in the simulations in next section.

The full schematics with component values of this example flyback converter is shown in Figure 3, which is also the simulation model used to obtain the simulation results in the next section. In the simulation model, Cxpri, L4, and L5 are parasitic components for the simulation. They have different values in different board and transformer design. To make the simulation time shorter, a rather small filter capacitance is used in the output. In an actual application, they may need to be bigger depending on output ripple requirements.

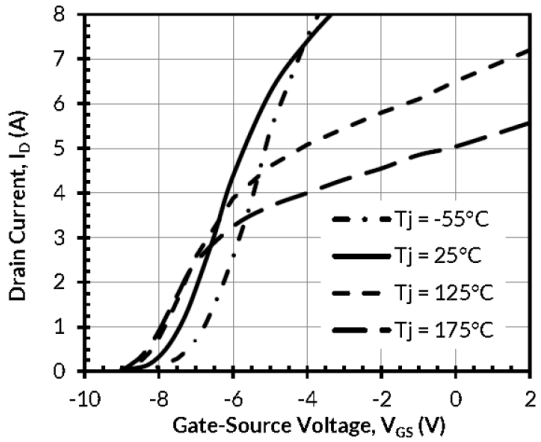

Figure 2. UF3N170400B7S Drain Current vs. Gate-source Voltage Curves

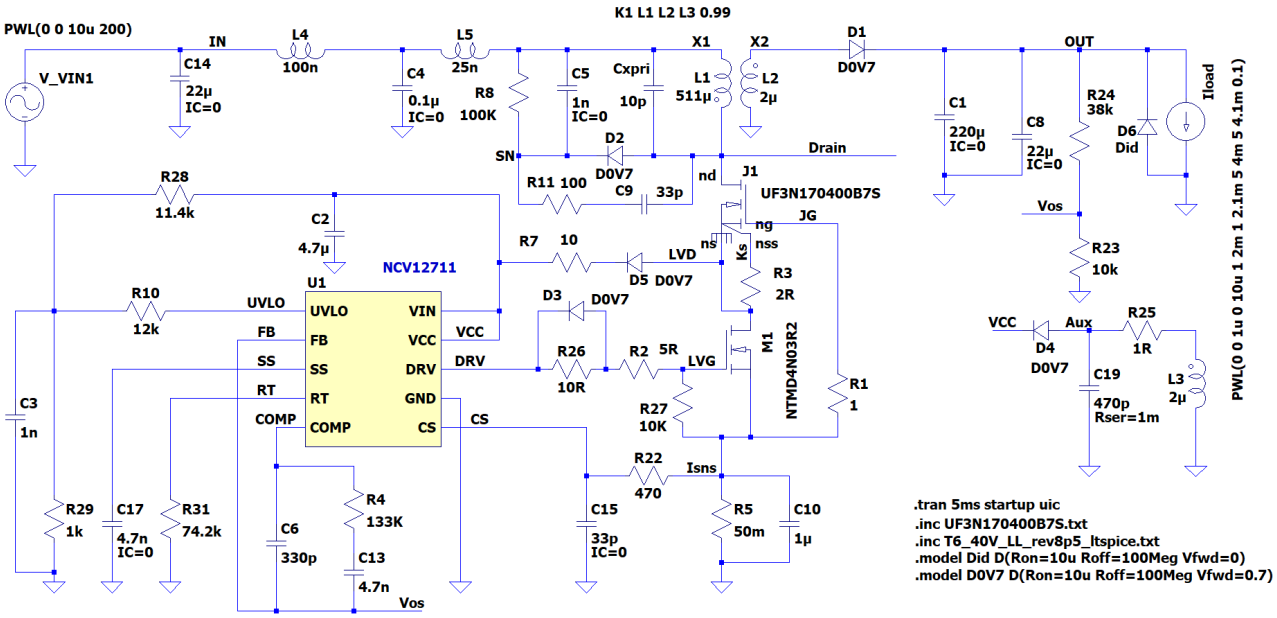

Figure 3. Simulation Model of a Flyback Converter Using Cascoded JFET as Main Switch

SIMULATED RESULTS

Simulated key waveforms for three input voltages at 200 V, 400 V, and 1000 V are given in this section. For each input voltage, a current source loading is used to demonstrate the load step transients and the steady state behaviors at different loading conditions.

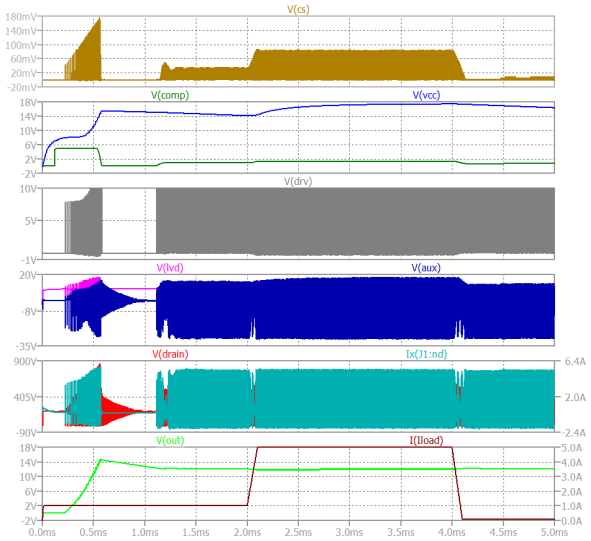

Figure 4. Simulated Waveforms With Input Voltage Set to 200 V

Figure 4 shows the waveforms for the full transient simulation run with input voltage set to the nominal minimum, 200 V. V(lvd) and V(aux) traces can be used to demonstrate the starting bias power sharing between two power sources: JFET power source and transformer aux winding. Before switching starts, V(lvd) (pink trace) is higher than V(aux) (blue trace) and JFET power source provides starting bias power.

At about 0.6 ms, the soft-starting process is not finished yet but the output over-voltage protection kicks in and stops the switching, until V_{out} drops down to the point when the switching starts again.

Light load operation at input voltage of 200 V is shown in Figure 6, where output current is set to 1 A. The waveforms show a typical flyback operation in the DCM mode. Full load operation is shown in Figure 7 with the output setting to 5 A. This is the designed CrM operation.

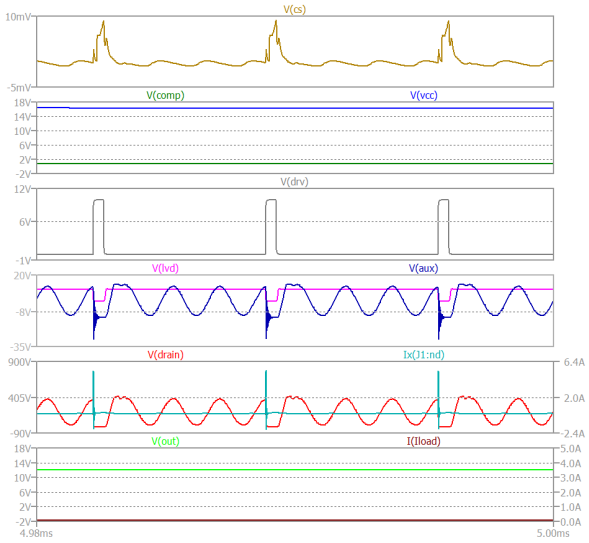

Figure 5.

Shows the waveforms at very light load working condition of 0.1 A (1.2 W).

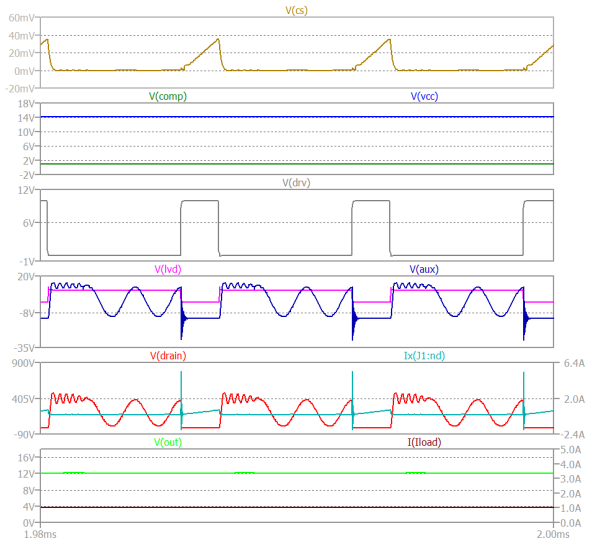

Figure 6. Zoomed-in Section of the Simulated Waveforms Under the Working Condition of 200 V Input and 1 A Loading

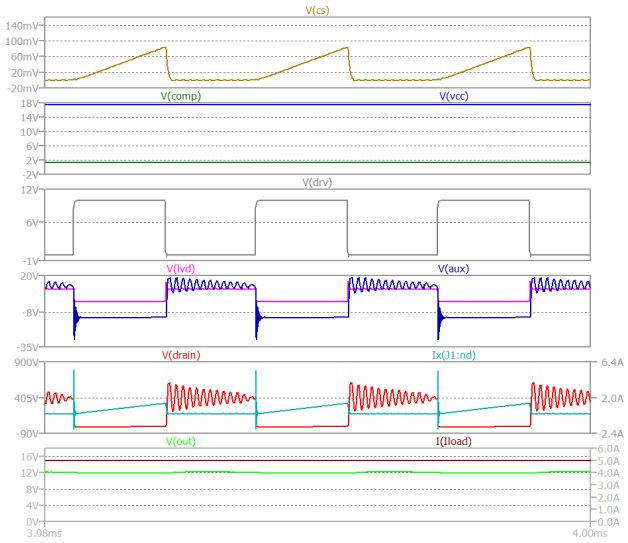

Figure 7. Zoomed-in Section of the Simulated Waveforms Under the Working Condition of 200 V Input and 5 A Loading

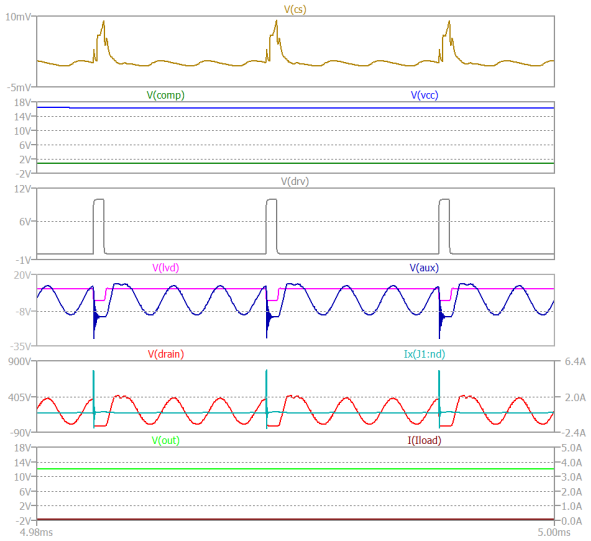

Figure 8. Zoomed-in Section of the Simulated Waveforms Under the Working Condition of 200 V Input and 0.1 A Loading

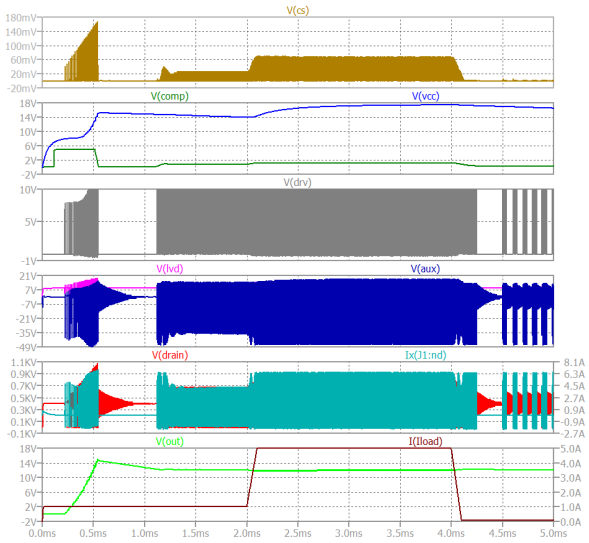

Figure 9. Simulated Waveforms With Input Voltage Set to 400 V

Figure 9 shows the waveforms with input voltage set to 400 V. The starting of the converter and light load at 1 A are similar to that with 200 V input. It can also be seen when the load drops to 0.1 A the converter enters skip-cycle mode. Full load of 5 A operation is shown in Figure 10.

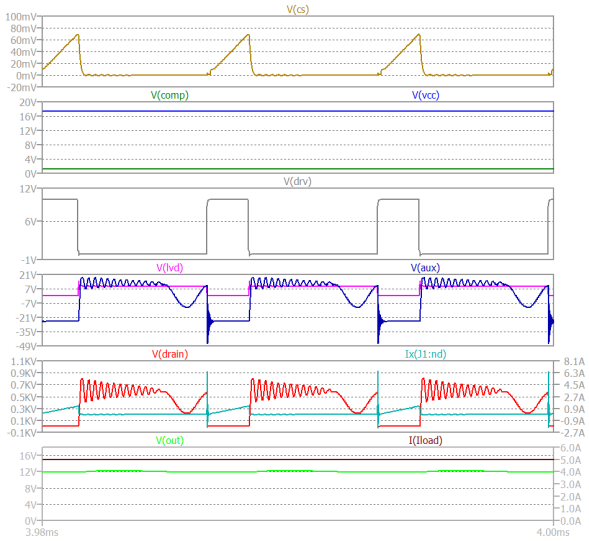

Figure 10. Zoomed-in Section of the Simulated Waveforms Under the Working Condition of 400 V Input and 5 A Loading

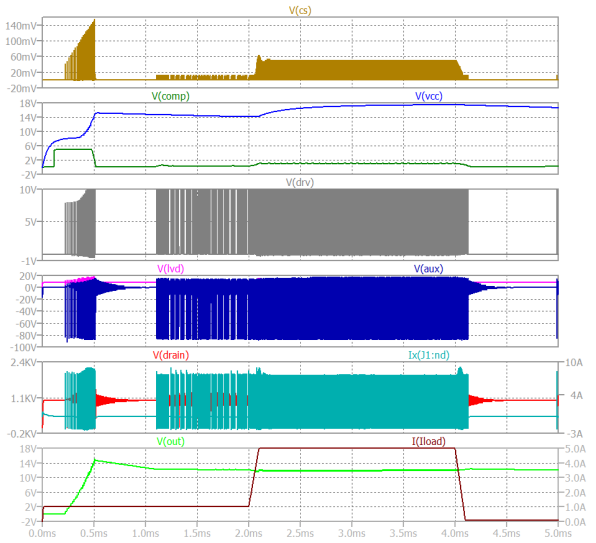

Figure 11. Simulated Waveforms With Input Voltage Set to 1000 V

Figure 11 shows the waveforms with input voltage set to the working maximum, 1000 V. Light load operation at input voltage of 1000 V is shown in Figure 12 with output of 1 A. Skip cycle operation can be seen. Full load operation is shown in Figure 13.

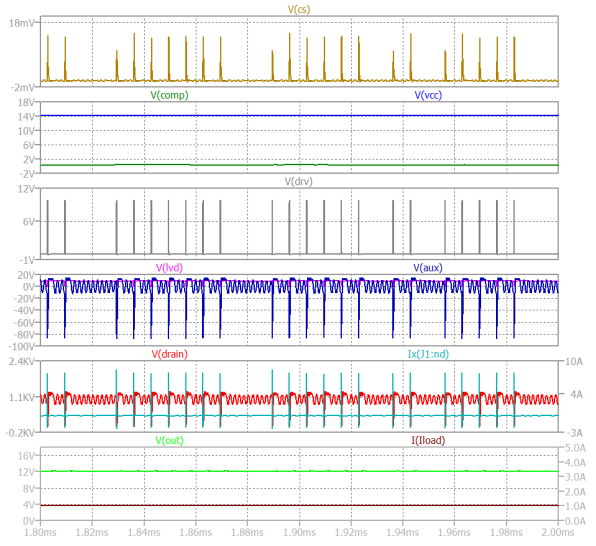

Figure 12. Zoomed-in Section of the Simulated Waveforms Under the Working Condition of 1000 V Input and 1 A Loading

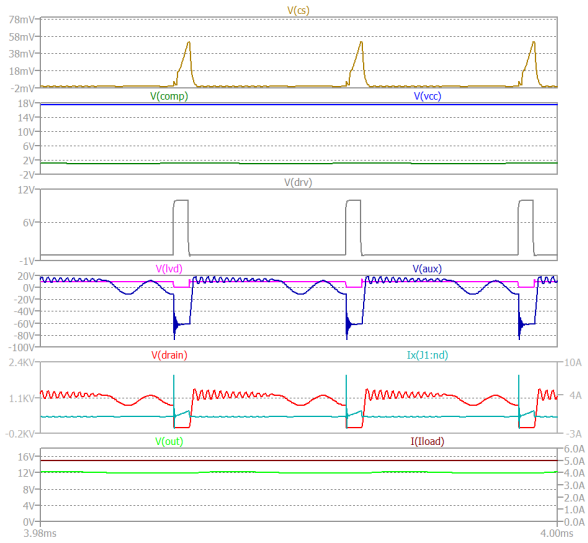

Figure 13. Zoomed-in Section of the Simulated Waveforms Under the Working Condition of 1000 V Input and 5 A Loading

SUMMARY

In this application note a high voltage input flyback converter is designed. With cascode configuration of an HV JFET and LV MOSFET as the power switch, the starting circuit is simplified and power loss from the high voltage starting circuit is saved. The cascode switch can be gated on and off with a MOSFET controller. **onsemi**'s NCV12711 is used in this design.

For more information regarding **onsemi**'s high-voltage JFETs and the simulation model used in this application note, please use the links provided in the Reference section.

REFERENCES

[1] Depletion-mode SiC VJFET Simplifies High Voltage SMPS, PCIM 2012, Nigel Springett and Jeff Casady

[2] Filter Inductor and Flyback Transformer Design for Switching Power Supplies, Lloyd Dixon (Unitrode Design Seminar, 1991)

[3] Switch-Mode Power Supplies, SPICE Simulations and Practical Designs, Christophe Basso (McGraw Hill, 2008)

[4] **onsemi** Silicon Carbide (SiC) Cascode JFETs products: https://www.**onsemi**.com/products/discrete−power−modules/silicon−carbide−sic/silicon−carbide−sic−cascode−jfets

[5] JFET User Guide: https://www.**onsemi**.com/download/user−s−manual/pdf/um70113−d.pdf

[6] JFET Primer: https://www.**onsemi**.com/download/application−notes/pdf/and90329−d.pdf

REVISION HISTORY

Revision	Description of Changes	Date
2	1. Changed Input/output design specification ranges; 2. Changed controller IC and LV Mos used in the design; 3. updated the simulation model and results.	11/6/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

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