# How to Achieve 99.3% Efficiency in 3.6 kW Totem-pole PFC Using 750 V Gen 4 SiC Cascode JFETs

# AND90324/D

### Introduction

This application note explains how the breakthrough performance of **onsemi** 750 V Gen 4 SiC Cascode JFETs enables a simple design of highly efficient Totem-pole PFC. Efficiency measurements on the developed unit will demonstrate a 99.3% efficiency rating. Insight into the losses is provided by the new **onsemi** Elite Power Simulator on-line tool, which are shown to match the actual measurements quite well. Finally, we discuss how the high efficiency of SiC Cascode JFETs allows further BOM cost reduction for Totem-pole PFC.

### Background

To help power grids operate reliably and efficiently, there are international standards that limit harmonics injected by numerous electronic applications. Power factor correction (PFC) is a very efficient and effective approach to reduce harmonics injected to power grid. PFC achieves low harmonics by controlling the AC input current to follow the shape and phase of AC input voltage so that load appears resistive to the power grid. As electrification accelerates in everyday life single-phase PFC gets more popular and its efficiency becomes more important for power applications less than 7 kW (server, telecom, blockchain mining power supply, EV OBC, etc.).

Bridgeless totem-pole PFC (TPPFC) is a single-phase PFC that further improves efficiency over conventional boost PFC by reducing the number of semiconductor devices in the conduction path from three to two. Silicon based totem-pole PFC has been limited to critical conduction mode (CrM) due to the high Qrr of silicon switches. CrM operation requires complex control and interleaving making it less attractive for higher power applications than continuous conduction mode (CCM). **onsemi** offers the industry leading Gen 4 SiC Cascode JFETs that enable CCM operation of TPPFC making it a simple, efficient, and cost-effective solution. Industry leaders already deploy this solution in many fields such as automotive on-board charging, telecom power supplies, datacenter servers, etc. A 3.6 kW CCM TPPFC demo board demonstrates the 99.3% high efficiency enabled by Gen 4 SiC Cascode JFETs.

### Benefits of TPPFC

*High Efficiency*

For AC-DC power converters less than 7 kW a single-phase bridgeless totem-pole PFC is a superior topology to enable titanium efficiency than conventional boost PFC. Conventional PFC converters use a full-wave diode rectifier to achieve input rectification and a subsequent boost converter to provide the desired DC output. This topology takes three semiconductor devices in the line-current path as shown in Figure 1. The arrows indicate current path in positive half-cycle of AC line input. To reduce the conduction loss, the totem-pole bridgeless topology uses a full-bridge and reduces the number of devices in the conduction path to two.

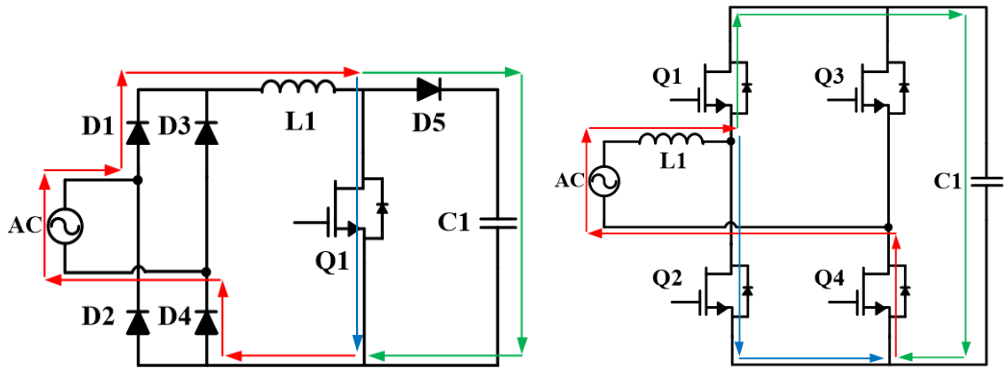


**Figure 1. Convention PFC with Full-wave Diode Rectifier and Boost Converter (Left), Bridgeless Totem-pole PFC (Right)**

*Less EMI*

Besides the lower conduction loss, totem-pole PFC also introduces less common mode electromagnetic interference (EMI) compared to other bridgeless PFC topologies [1]. However, even with the best silicon devices, this topology was impractical in continuous conduction mode (CCM) due to the large reverse recovery loss of the freewheeling device body diode [2].

*CCM vs CrM*

CCM and CrM has its pros and cons in EMI, inductor design and device selection. Generally, for high power applications, CrM requires interleaving which increases BOM and complexity. For a given design, if target efficiency can be achieved with one power device per switch position, non-interleaved CCM will be more cost-effective. Figure 2 shows the concept of CCM and CrM.

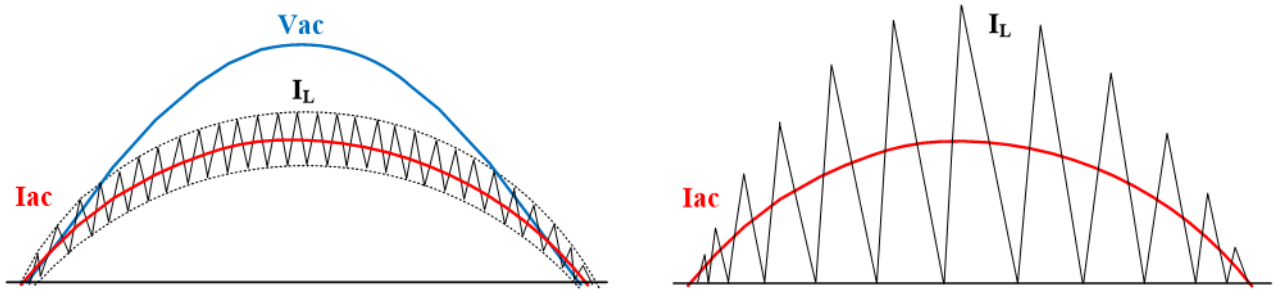


**Figure 2. CCM Inductor Current Waveforms on the Left; CrM Inductor Current Waveforms on the Right**

The name of CCM (continuous conduction mode) comes from the fact that inductor current is always above zero at every switching cycle in one half-line-cycle. DCM (discontinuous conduction mode) means the inductor current drops down to zero and stays at zero for rest of the switching period at every switching cycle. CrM (critical conduction mode) is the boundary condition between CCM and DCM.

The difference in inductor current waveform implies another fundamental difference that CCM uses average current control which has constant switching frequency while CrM uses constant on-time control which has variant switching frequency. Both operates in discontinuous mode (DCM) near zero-crossing. The operation difference leads to different features in EMI, inductor design and device selection.

*EMI*

In CCM the PFC inductor peak-to-peak current ripple is usually limited within 40% of average current. On the other hand, CrM requires turn-off current to be twice of input AC current at every switching cycle which makes peak-to-peak current ripple 200%. This high current ripple introduces switching frequency harmonics as differential mode conducted EMI for high power applications. For example, for a 3.6 kW TPPFC working at 230 Vac (high line) input voltage, the peak of average inductor current is 22 A which means 44 A peak turn-off current for CrM if not interleaved.

CCM requires hard switching for both active and freewheeling devices. Therefore, CCM requires good reverse recovery performance for the freewheeling device. CrM achieves soft switching for both active and freewheeling devices. The freewheeling device has zero current turn-off (ZCS), the active device has ZCS for turn-on which reduce reverse recovery related EMI and turn-on loss. When freewheeling device is in synchronous rectification the CrM can also achieve zero voltage switching (ZVS) for the active device by allowing inductor current goes slightly below 0 A. However, due to high current ripple, CrM has high turn-off switching loss for the active device. High turn-off current will also introduce high frequency harmonics from the fast dv/dt, di/dt slew rate.

Therefore, CCM has less current ripple and less slew rate related EMI compare to CrM.

*Inductor Design*

CCM requires higher PFC inductance to reduce current ripple. For a given design, if we can achieve target efficiency with one power device per switch position, CCM saves cost in gate drive, device count and board size. CrM requires much less inductance due to high current ripple. But interleaving is needed to reduce turn-off current in each inductor thus increasing cost in device count, gate drive and board size. The high turn-off current requires magnetic core with high saturation current, the high switching frequency together with high current ripple requires low core loss, also high current ripple means high RMS current which requires thicker winding to reduce copper loss.

*Device Selection*

CCM requires hard switching thus demands great switching performance from power devices, especially diode fast reverse recovery capability. CrM provides soft switching to relieve fast reverse recovery requirement on device. But CrM has 200% peak-to-peak current ripple which leads to high turn-off current stress, high turn-off switching loss and fast turn-off slew rate related EMI.

To sum up, if a given design does not require multiple devices in parallel to handle power loss, non-interleaved CCM is simpler, more cost-effective and has less EMI than

CrM. The 3.6kW TPPFC demo board demonstrates high efficiency and simple design enabled by **onsemi**'s Gen 4 SiC Cascode JFETs.

### Performance of Gen4 SiC Cascode JFETs

The new Gen 4 series of SiC Cascode JFETs include a 750 V rating allowing additional design margin for 400 V or 500 V battery/bus voltage applications. Despite the increased voltage rating, Gen 4 devices employ advanced cell density to reduce the RDS(on) per unit area, delivering the industry's lowest resistance products in all packages. High current ratings are achieved by the advanced sintered die attach technology offering improved thermal performance. Figure 3 left chart shows the new 750 V specific on-resistance versus 650 V rated SiC competitors, offering substantially lower conduction losses across the full temperature range.

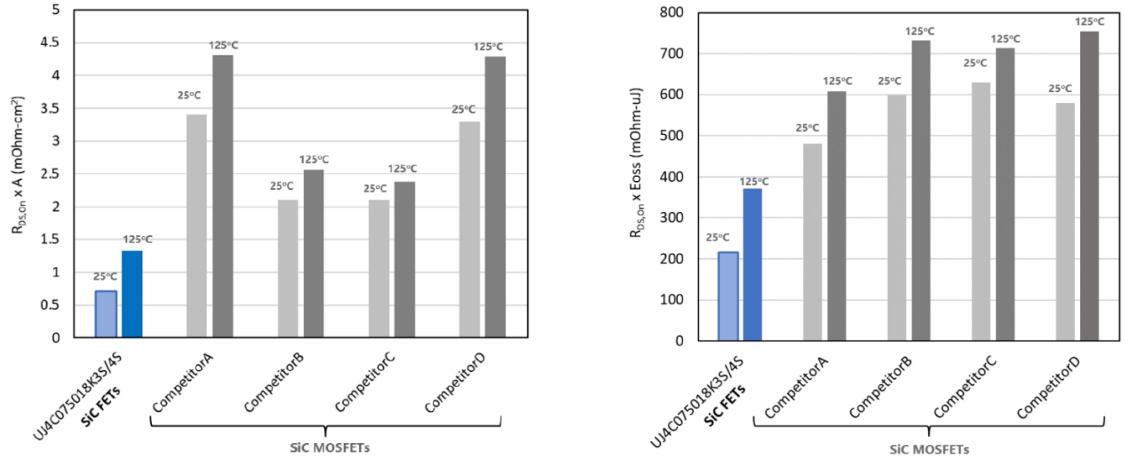


**Figure 3. Left chart Shows 750 V Gen 4 onsemi FET On-resistance per Unit Area Compared to 650 V Rated SiC Competitors. Right Chart Shows Hard-switching Figure of Merit Compared to SiC Competitors**

Along with low on-resistance, these new SiC Cascode JFETs offer improved efficiency in both hard and soft-switched circuits. In hard-switched circuits such as CCM TPPFC or standard 2-level inverters, the low on-resistance per unit-area and low output capacitance offer superior reverse recovery charge (Qrr) and low Eoss/Qoss. Besides, the devices exhibit a superior and robust integral diode with low voltage drop VF (<1.75 V).

Figure 3 right chart illustrates the advantage of the 750 V **onsemi** FETs versus their 650 V rated SiC competitors when represented as a hard-switching Figure-of-Merit (FOM) of RDS(on) x Eoss. The UJ4C075018K3S (in TO247-3L package) and UJ4C075018K4S (in TO247-4L package) features a low on-resistance of 18 mΩ at 25 °C, which is 50% less at 25 °C and almost 40% less at 125 °C compared to its closest competitor.

Gen 4 devices also inherit the ease-of-use from previous generations. As shown in Figure 4 all devices can be safely driven with standard 0 V to 12 V or 15 V gate drive voltage. A 5 V Vgs threshold voltage provides good noise immunity during switching transients. Like previous generations, these new SiC Cascode JFETs can be operated from all the typical Si IGBT, Si MOSFET and SiC MOSFET drive voltages and includes a built-in ESD gate protection clamp.

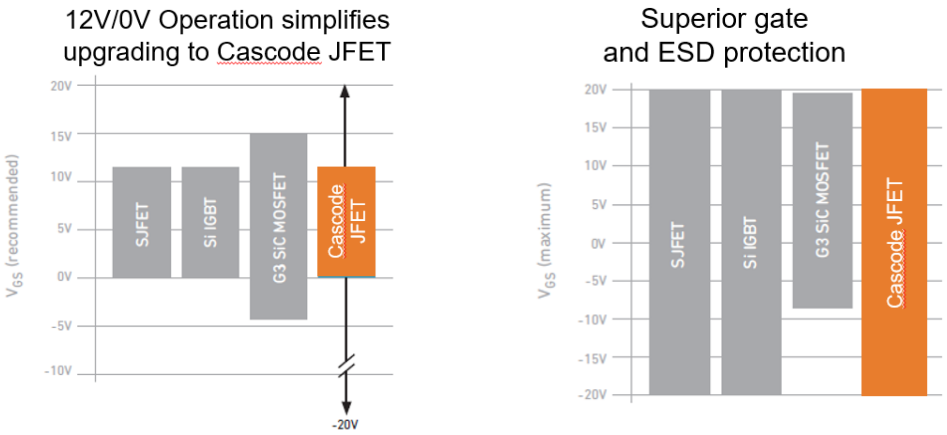


**Figure 4. Gen 4 SiC Cascode JFETs Gate Drive Compatibility with Si and SiC Devices**

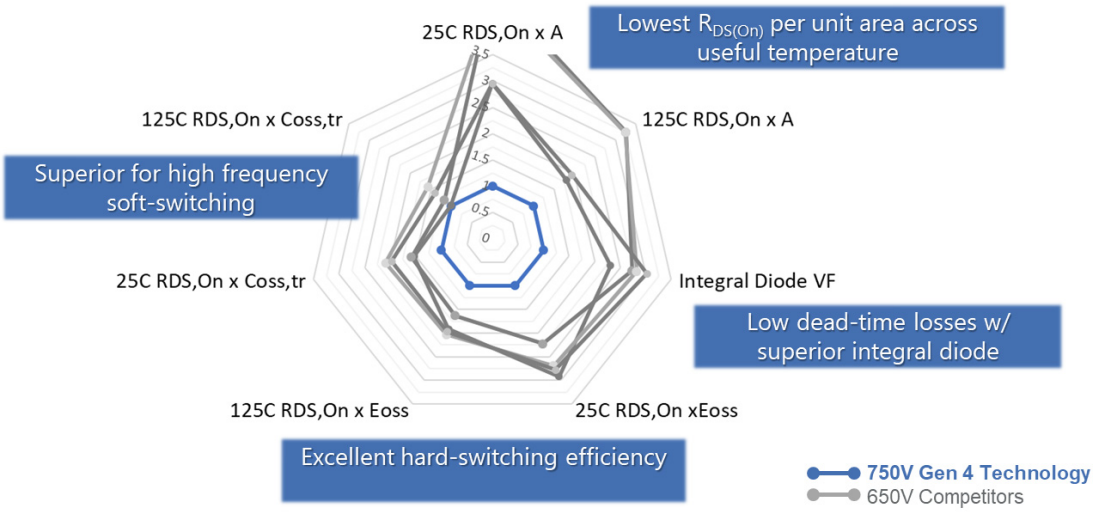


**Figure 5. Radar Plot of onsemi 750 V FETs Comparative Advantage with Key Parameters Normalized (Note: Lower Values are Superior)**

The radar plot shown in Figure 5 summarizes the comparative advantage of Gen 4 750 V FETs. The SiC Cascode JFETs are unmatched when key hard switching and soft-switching parameters are considered. The ultra- low on-resistance per unit area allow standard discrete packages with performances not achievable with existing Si or emerging WBG competing technologies [3].

To sum up, low on-resistance per unit area means for a given die size Gen4 SiC Cascode JFETs have low conduction loss. Low hard-switching FOM means for a given RDS(on) Gen4 SiC Cascode JFETs have low parasitic capacitance and low switching loss.

### Measured Efficiency (SR on Slow Leg)

To demonstrate the excellent performance of Gen 4 FETs, a 3.6 kW CCM TPPFC is built for bit-coin server power supply. Table 1 shows the digital controlled 3.6 kW CCM TPPFC demo board specification and features. With two UJ4C075018K4S (Gen 4 750 V 18 mΩ TO-247-4L) in the fast leg, the peak efficiency achieves 99.37% at 230 Vac input excluding auxiliary power supply loss. This efficiency is measured when slow leg operates in synchronous rectification (SR) mode.

**Table 1. THE 3.6 kW CCM TPPFC DESIGN SPECIFICATION AND FEATURES**

| | | |
|---|---|---|
| AC Input | AC Voltage | 85~264 Vac |
| | AC Line Frequency | 47~63 Hz |
| | Switching Frequency | 60 kHz |
| | AC Connection | L + N + PE |
| DC Output | DC Voltage | 390 Vdc |
| | Output Power | 3600 W (230 Vac), power derating when Vin < 170 Vac |
| | Overload Capability | 105%~140% 1 min |
| Protection | Features | Over voltage, input frequency, overload, over current, over current |
| Mechanical Parameter | Size | 260 mm x 102 mm x 60 mm (L x W x H) |
| | Weight | ~0.87 kg (without case) |
| Power Device | Fast Leg | 4X UJ4C075060K4S vs 2X UJ4C075018K4S |
| | Slow Leg | 4X (28 mΩ Si Superjunction) |

Figure 6 shows the top view of the TPPFC demo board. Each half-bridge leg has two device switch positions, high side (HS) and low side (LS). If two devices are used in parallel for one device position, then a half-bridge (HB) leg requires 4 devices (4X).

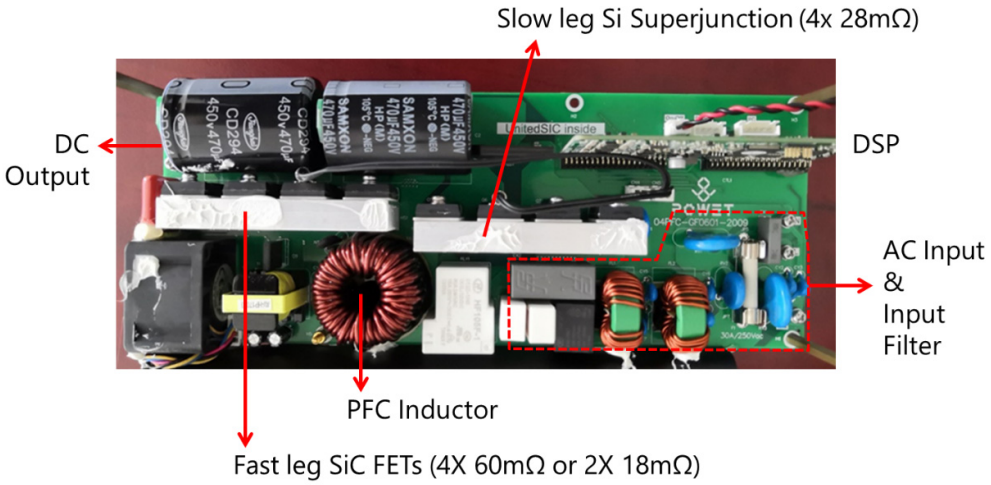


**Figure 6. Left Side Heatsink is Mounted with 4X UJ4C075060K4S or 2X UJ4C075018K4S. Right Side Heatsink is Mounted with 4X (Si Superjunction)**

Figure 7 shows the full load input voltage and current waveforms at high line (230 Vac) and low line (175 Vac). The current follows input voltage very well to achieve high power factor (near 1).

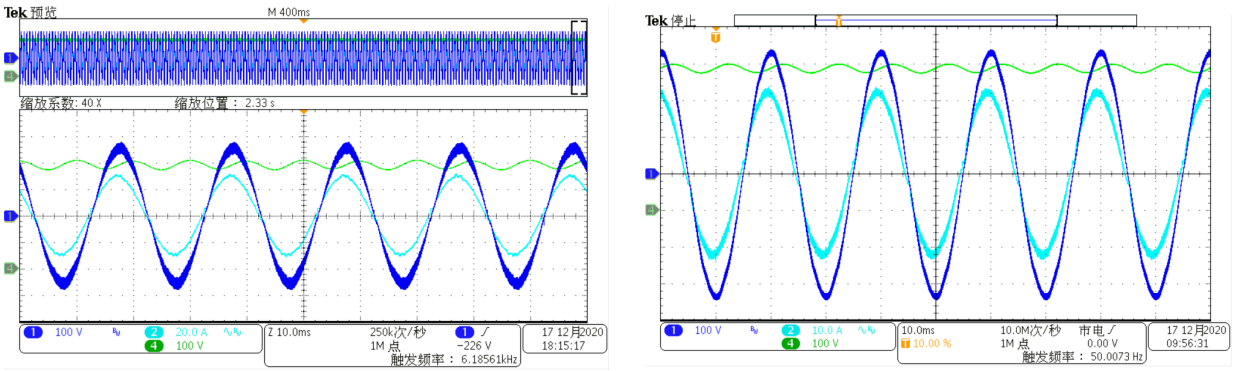

**Figure 7. Input Waveforms at 3.6 kW Full Load, Left Side at Low Line (175 Vac), Right Side at High Line (230 Vac)**

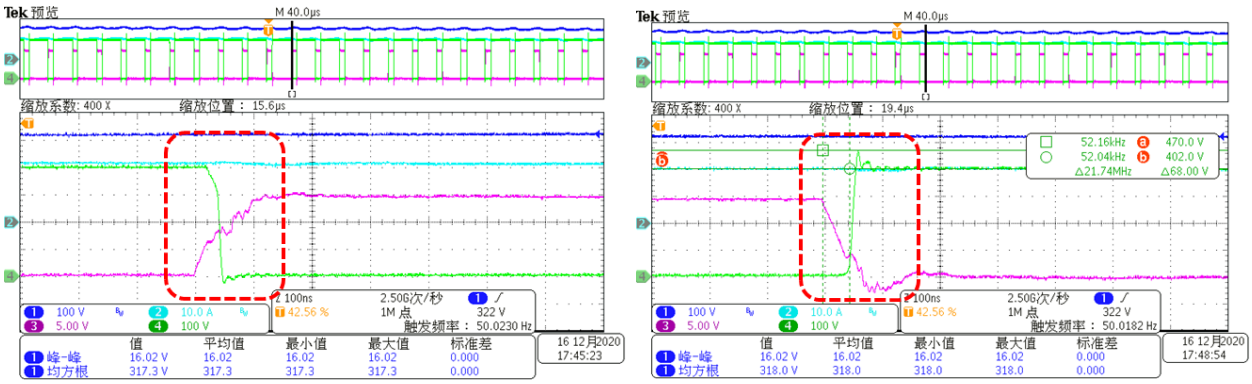

**Figure 8. VGS and VDS Waveforms at 3.6 kW with High Line (230 Vac) Input. Left (Turn-on), Right (Turn-off)**

Figure 8 shows VGS and VDS switching waveforms at full load near the peak of high line input where device switching current is also the highest. Only 68 V overshoot on VDS at full load. Peak VDS spike 470 V is only 60% of 750 V rating. This means highest hard-switching stress on the device. Left waveform shows turn on. Right waveform shows turn off. The waveforms for both VGS and VDS is very smooth and clean.

Figure 9 shows the measured efficiency for 4X UJ4C075060K4S (60 mΩ) per fast leg vs 2X UJ4C075018K4S (18 mΩ) per fast leg at high line (230 Vac) and low line (175 Vac). Figure 10 shows measured power factor. Efficiency and power factor are measured with two TH3331 power analyzers. Auxiliary power supply loss is excluded from the efficiency measurement.

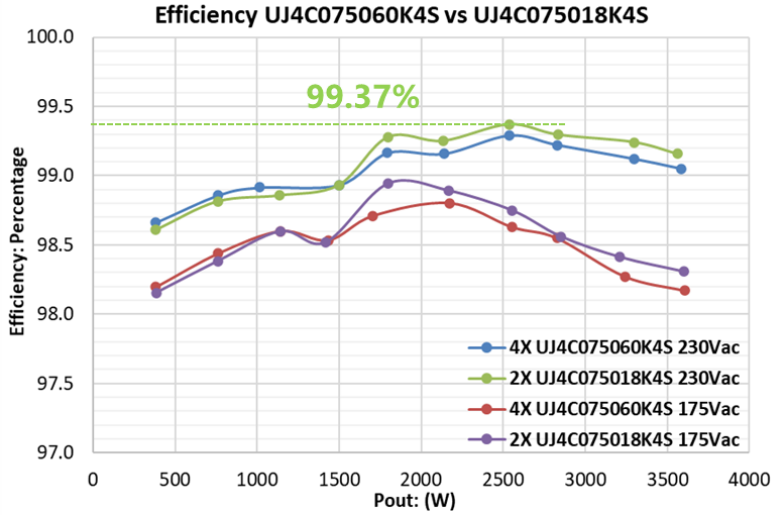


**Figure 9. Left Side Heatsink is Mounted with 4X UJ4C075060K4S or 2X UJ4C075018K4S. Right Side Heatsink is Mounted with 4X (Si Superjunction)**

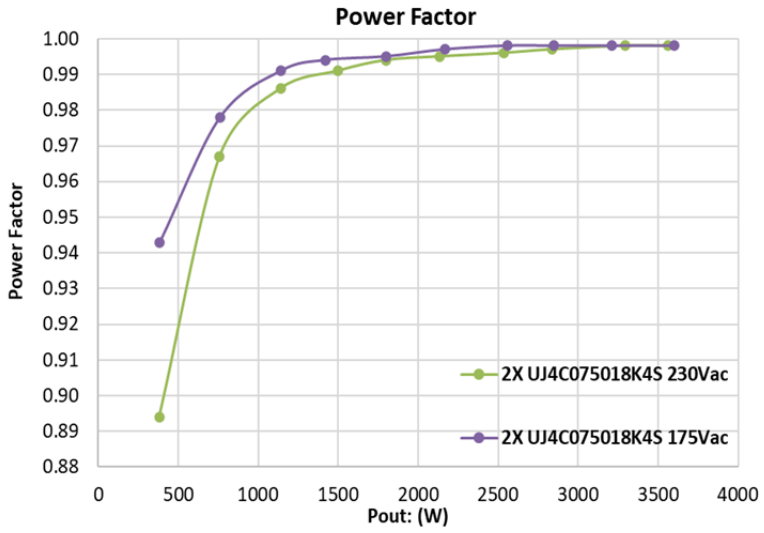


**Figure 10. Measured Power Factor for UJ4C075018K4S at High Line and Low Line**

As shown in Figure 9, for 3.6 kW power we recommend UJ4C075018K4S because at high line its efficiency is always above 99% from 42% to 100% load with only one device per switch position. This further reduces board size and increases power density. Together with Gen 4 unmatched low on-resistance per unit area, UJ4C075018K4S will be a very cost-effective choice.

As shown in Figure 10 power factor is above 0.99 when load is above 40%. Even at 20% of load at high line the power factor is above 0.96. With such high efficiency and power factor performance designers can easily achieve 80 Plus titanium standard.

### Calculation of Device Loss

**onsemi** has recently developed the Elite Power Simulator, an on-line tool that helps designers evaluate their devices in a variety of circuit topologies and quickly and accurately focus in on the optimal solutions. In this analysis, we used the FET-Jet Calculator to better understand the device loss contribution in TPPFC. The conduction loss is based on Tj vs RDS(on) and input and load conditions. The switching loss model comes from curve fitting of measured switching loss on a double pulse tester. The efficiency data compared in this section are based on LF leg in synchronous rectification (SR) mode.

Figure 11 compares the calculated and measured Tj of UJ4C075018K4S. Tj is measured with NTC resistor. Thanks to the high efficiency enabled by the great performance of Gen 4 SiC Cascode JFETs, Tj at full load is only 50 °C. Tj is calculated using the following equation. As shown in Figure 11 FET JET calculator results represent actual measurement very well. Therefore, designers can use the FET JET calculator to choose topology and devices with confidence.

$$T_{j\_calculated} = T_{heatsink} + R_{thJH} * P_{loss} \quad \text{(eq. 1)}$$

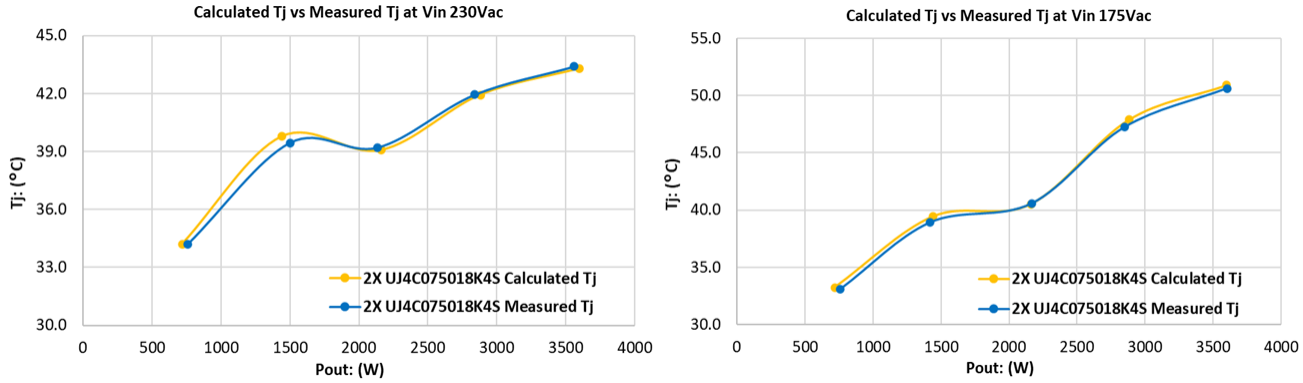


**Figure 11. Measured Tj vs Calculated Tj ( Left at High Line, Right at Low Line)**

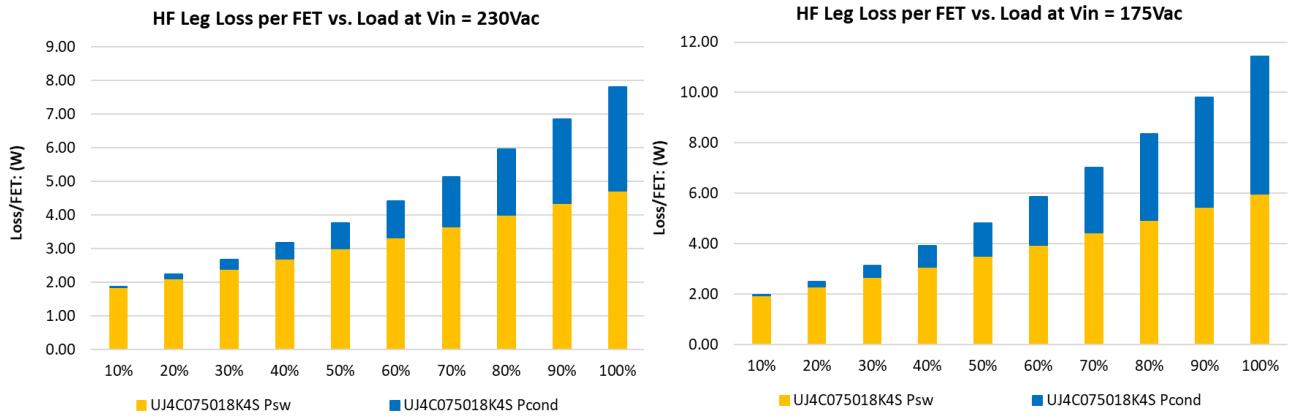


**Figure 12. Calculated Loss per FET for UJ4C075018K4S at High Line (Left), Low Line Right), Psw (Switching Loss), Pcond Conduction Loss)**

As shown in Figure 12 at high line full load the loss per FET is only 7.8 W. Therefore, smaller package and surface mount package can be used to further reduce cost, board size, and increase power density. Thanks to Gen 4 FETs superior on resistance per unit area, we can provide the 750 V 18 m device in TO220 and D2PAK7L.

### More Cost-effective Design (Diode on Slow Leg)

With the excellent performance from Gen 4 FETs the line frequency leg (LF) can use diode rectification and still achieves above 99% peak efficiency as shown in Figure 13 and Figure 14. This will further reduce cost as Si diodes are much cheaper than low RDS(on) Si superjunction MOSFET. Moreover, as shown in Figure 13, we can simplify the circuit by using one diode rectifier bridge for the LF leg diodes D3, D4 and the pre-charge surge diode D1, D2. Therefore, Figure 13 provides a more cost-effective design achieving both cost and board size reduction with above 99% efficiency from 50% to 85% of the load.

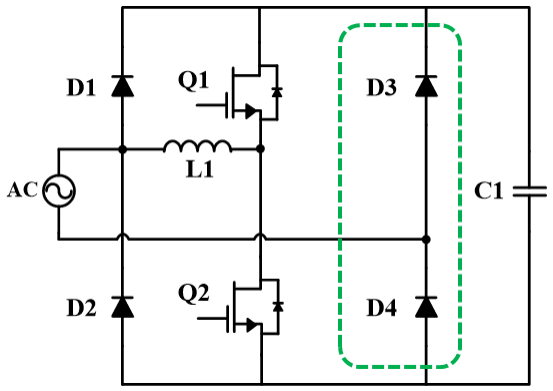


**Figure 13. Cost-effective Solution: Replacing Low Frequency Leg with Si Diodes**

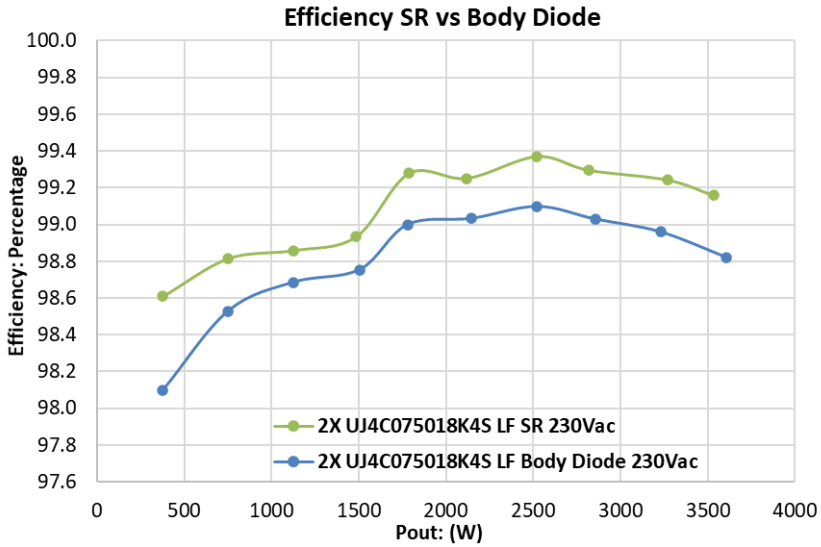


**Figure 14. Compares TPPFC Efficiency Between LF Leg Using Synchronous Rectification (Si Superjunction) and Using Si Superjunction Body Diode**

## Summary

Thanks to the excellent performance from **onsemi**'s Gen 4 FETs, 99.37% peak efficiency is achieved on a 3.6 kW CCM TPPFC with only two UJ4C075018K4S devices. Detailed loss calculation shows very small loss on Gen 4 FETs which suggests viability of using smaller packages that can further increase power density and reduce cost. Moreover, a cost-effective solution is proposed to replace expensive low RDS(on) Si superjunction MOSFET with Si diode rectifier and still achieve above 99% peak efficiency from 50% to 85% load range.

**onsemi**'s Gen 4 FETs provides high efficiency, high power density, low cost, and a very simple power design for hard-switching applications like CCM TPPFC.

## References

[1] Q. Li, M. A. E. Andersen and O. C. Thomsen, “Conduction losses and common mode EMI analysis on bridgeless power factor correction,” 2009 International Conference on Power Electronics and Drive Systems (PEDS), Taipei, 2009, pp. 1255-1260.

[2] Zhu, Ke & O’Grady, Matt & Dodge, Jonathan & Bendel, John & Hostetler, John. (2016). 1.5 kW single phase CCM totem-pole PFC using 650 V SiC cascodes. 10.1109/WiPDA.2016.7799915.



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