How to Slow Down dV/dt During Switching Using SiC Cascode JFETs

AND90323/D

Introduction

For certain applications, such as motor control, it is important to slow dV/dt down during switching. Too fast and it would cause a high voltage spike on the motor, which could damage the winding insulation and so, reduce motor life. In this app note, compares three different dV/dt control methods are compared.

dV/dt Switching

The conventional method for reducing switching dV/dt of silicon MOSFETs, IGBTs and SiC MOSFETs would be increasing the external gate resistor value. Because these devices have relatively high CGD (C_{RSS}), external R_G values can slow down dV/dt without excessive delay times. This method is great for fast switching applications, such as Totem-pole PFC, where faster dV/dt leads to lower switching loss. However, for slower applications, such as a motor, it would require a very high resistance value. To slow it down to 5~8 V/ns would require a gate resistance of several kilo-Ω, which would result in excessively long switching delay time and therefore a low stepping rate. For position control applications, this would be detrimental to performance.

There are methods that can effectively control dV/dt of SiC JFET devices from 45 V/ns to 5 V/ns, without the penalty of excessive delay time. The three methods are: external gate drain capacitor, device RC-snubber and JFET direct drive, using a **onsemi** 9 mΩ 1200 V SiC JFET in a standard TO247-4L package UF3SC120009K4S[1], switched at 75 A/800 V.

External Gate Drain Capacitor

The first method is to add an external gate drain capacitor (C_{GD}) between gate and drain of both high side and low side JFETs of a half-bridge. For chosen SiC JFET, the value of C_{GDEXT} has been selected to be 68 pF. A 20 nH parasitic inductance was deliberately added in series with external capacitor, to illustrate that this method is not sensitive to parasitic inductances in the its path (Figure 1).

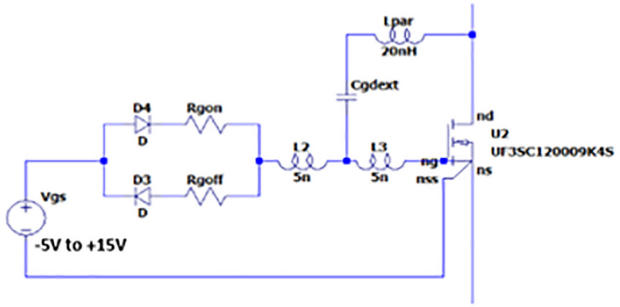

Figure 1. Gate Drive with External CGD (on Both High Side and Low Side JFET) for dV/dt Control

In real applications, where discretes are used, this parasitic inductance should be much less than 20 nH, since the external C_{GD} can be placed close to the JFETs on PCB. However, if the **onsemi** JFET chips are used inside modules with the external C_{GD} placed outside the module, it could be possible to have 20 nH parasitic inductance in its path.

The external C_{GD} method was first optimized with SPICE simulations, using the UF3SC120009K4S SPICE model[2, 3], then verified experimentally using a double pulse testing circuit. The 68 pF external C_{GD} was soldered deliberately between the G and D leads of the TO247-4L, instead of on the PCB board, to increase parasitic inductance in its path.

Turn-off and turn-on waveforms from the experimental measurement and SPICE simulation were overlaid for comparison. In Figure 2, the measured and simulated waveforms matched very well.

1. UF3SC120009K4S detail: https://www.onsemi.com/download/data-sheet/pdf/uf3sc120009k4s-d.pdf
2. Importing **onsemi** Models into LTSPICE, Application Note: AND90315/D
3. Switching Fast SiC JFETs with a Snubber, Application Note: AND90319/D

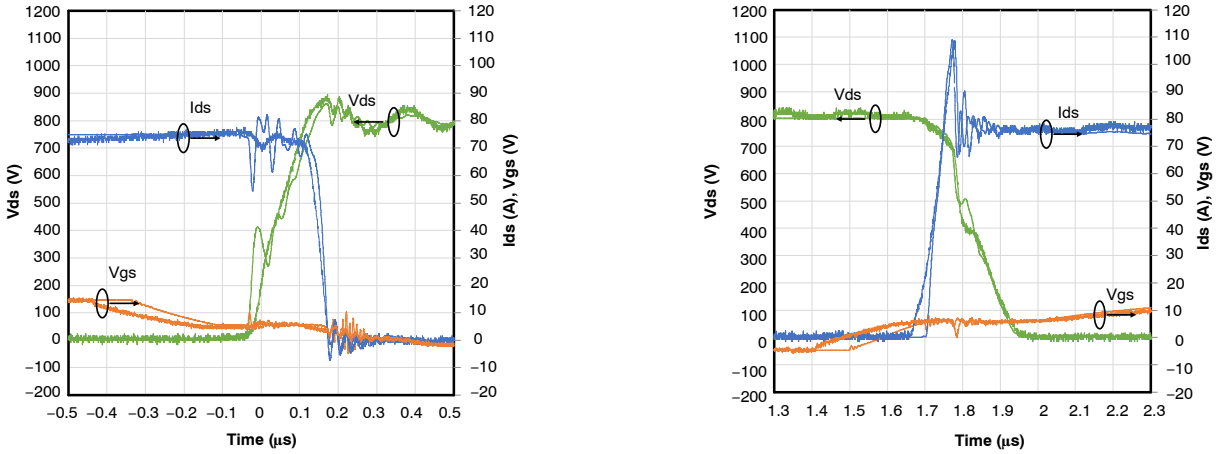

Figure 2. Overlaid Turn-off (Left) and Turn-on Waveforms of Experimental (Solid Lines) and SPICE Simulation (Dash Lines), 75 A 800 V External CGD 68 pF and RG 33 Ω

With the 68 pF external C_{GD}, dV/dt was effectively controlled in the range of 25 V/ns to 5 V/ns, using R_G of 10 Ω to 33 Ω. For both SPICE and experiment, E_{ON} and E_{OFF} were extracted by integrating IDS×VDS during turn-on and turn-off transition, which increased with R_G as expected.

The reason why the external C_{GD} can tolerate high parasitic inductance (20 nH in SPICE) was that the current was quite low during switching. For an external C_{GD} of 68 pF and dV/dt of 8 V/ns, the estimated current was only 0.54 A and was consistent with the current from SPICE simulations. This is, therefore, applicable to modules, where the external C_{GD} is placed outside the module on the gate drive PCB, with some parasitic inductance in its path.

Device RC-Snubber

The second dV/dt control method adds RC snubbers in parallel to the switches for both high side and low side. A 20 nH parasitic inductance was deliberately added in series with the snubber, for the purpose of proving this method can tolerate parasitic inductance in the snubber path (Figure 3).

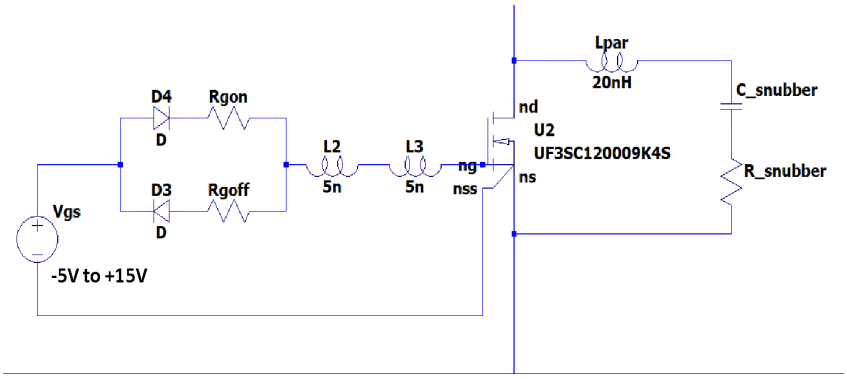

Figure 3. RC Snubber Parallel to JFET (on Both High Side and Low Side JFET) for dV/dt Control

In real applications, when using discretes, the RC snubber can be placed very close to the JFET, and the parasitic inductance would be only a few nH. But if the **onsemi** JFET chips are used inside modules, the RC snubber can be placed outside the module, and it is possible to have 20 nH parasitic inductance in its path.

Turn-off and turn-on waveforms from experimental measurement and SPICE simulation were overlaid for comparison (Figure 4). Note that the I_{DS} current in the plots included the snubber current. Experimental and SPICE showed dV/dt can be effectively controlled from 50 V/ns to 5 V/ns by C_SNUBBER (snubber capacitor) up to 5.6 nF.

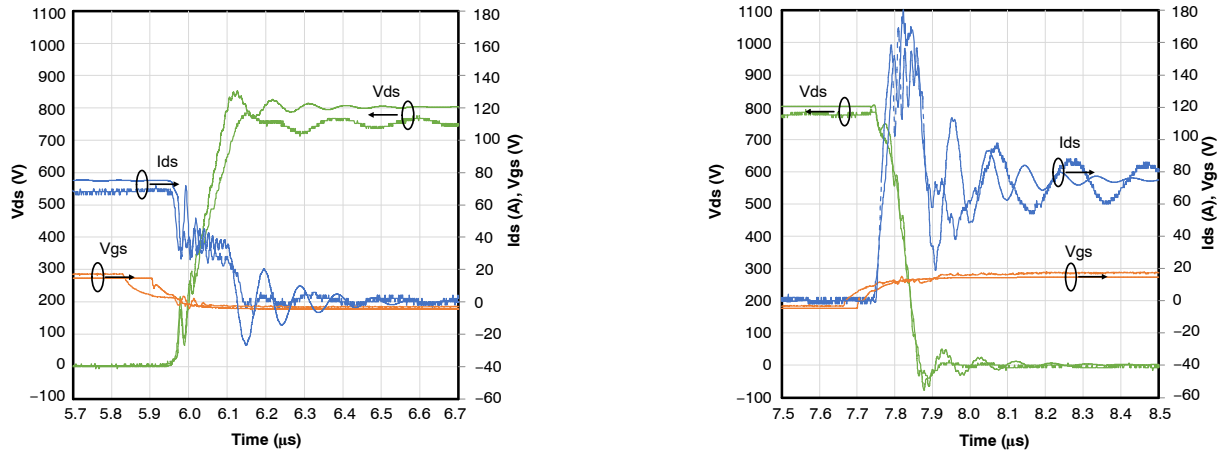

Figure 4. Overlaid Turn-off (Left) and Turn-on Waveforms of Experimental (Solid Lines) and SPICE Simulation (Dash Lines), 75 A 800 V with RC Snubber 0.5 Ω 5.6 nF

The switching losses (E_{ON}, E_{OFF} and E_{SW}) were extracted by integrating IDS×VDS during the switching transitions, where I_{DS} included the snubber current. Therefore, the E_{ON} and E_{OFF} included the losses on the snubbers. However, the snubber loss on the 0.5 Ω R_SNUBBER) was very low, especially at slower dV/dt. With a C_SNUBBER of 4 nF and turn-off dV/dt = 8 V/ns, SPICE showed that the snubber loss was only 0.2 mJ, or 2 Ω for f = 10 kHz switching. It is found that the snubber can also tolerate high parasitic inductance (20 nH in SPICE), and therefore in the case of modules the RC snubber can be placed outside module.

JFET Direct Drive

The third method is direct drive, where the Si MOS is turned on only once at circuit start up, and JFET gate is switched directly between −15 V to 0 V (Figure 5). In this configuration, normally-off operation is preserved, however, the gate PWM and simple Enable signals would be required. The high side JFET is kept off by −15 V during switching transients, and synchronous rectification is necessary for freewheeling JFET to reduce its conduction loss in the third quadrant.

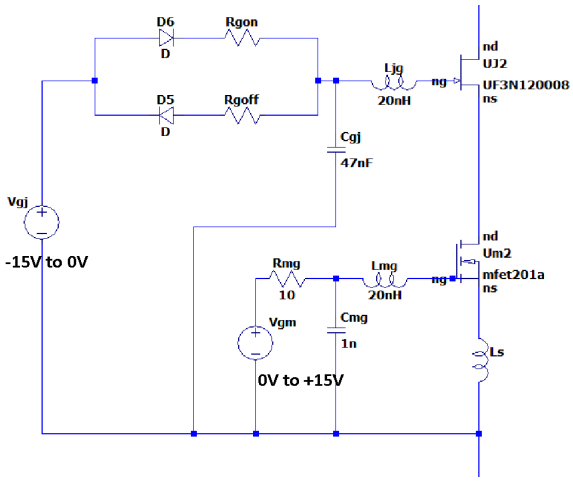

Figure 5. JFET Direct Drive Method (on Both High Side and Low Side JFET) for dV/dt Control

Because the SiC JFET has considerable C_{RSS} (C_{GD}), a small RG of 4.7 Ω would be enough to slow down dV/dt to 5 V/ns. Turn-off and turn-on waveforms from experimental measurement and SPICE simulation were overlaid for comparison (Figure 6).

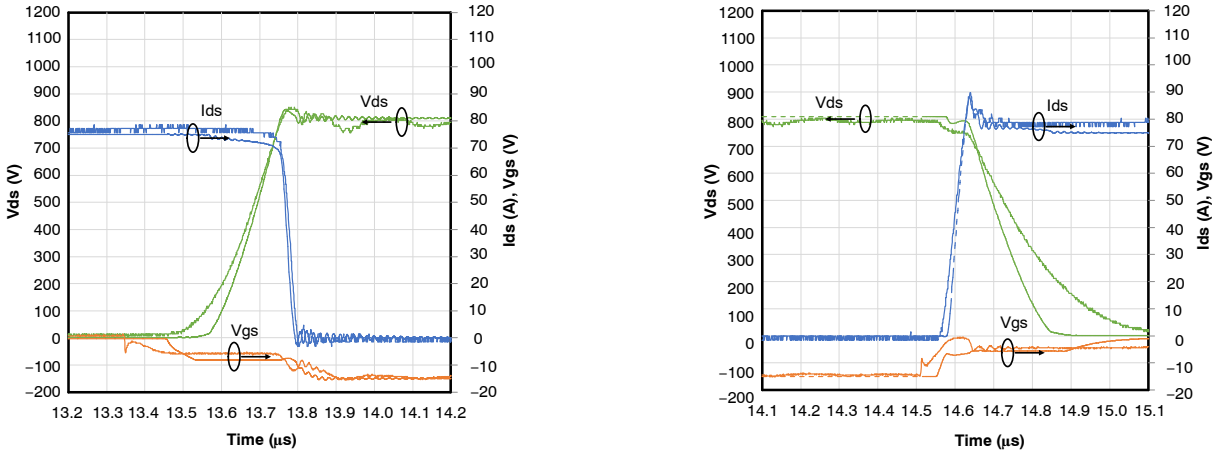

Figure 6. Overlaid Turn-off (Left) and Turn-on Waveforms of Experimental (Solid Lines) and SPICE Simulation (Dash Lines), 75 A 800 V, JFET Direct Drive with RG 4.7 Ω

The I_{DS} current waveforms matched well between SPICE (dash lines) and experimental waveforms (solid lines). But the experimental V_{DS} waveforms showed slower dV/dt than the SPICE waveform. The reason could be that the JFET gate driver used in the experiment was not able to provide enough gate current to charge or discharge the JFET C_{RSS} during the dV/dt transition, causing it to be slowed down.

The resulting dV/dt from SPICE and measurement were compared, showing dV/dt can be well controlled from 15 V/ns to 4 V/ns. The switching losses were extracted using the same way as the previous methods, and E_{ON} and E_{OFF} increased with JFET RG as expected.

Comparison on the Three dV/dt Control Methods

The three methods were compared using SPICE simulations under the same limitation of dV/dt ≤ 8 V/ns (Table 1).

Table 1. COMPARISON OF SPICE SIMULATED PERFORMANCE OF 75 A/800 V SWITCHING WITH MAXIMUM dV/dt = 8 V/ns

Method	Gate Drive Conditions	JFET Gate Access Needed	dV/dt_off (V/ns)	dV/dt_on (V/ns)	dI/dt_on (A/ns)	Vds Peak, Low Side (V)	Vds Peak, High Side (V)	E_off (mJ)	E_on (mJ)	E_sw (mJ)
External Cgd	External Cgd = 68 pF, Rgon = 18 Ω, Rgoff = 22.1 Ω, Vgon = +15 V, Vgoff = −5 V	No	8.0	8.0	4.1	881	853	5.56	5.26	10.82
Snubber	Csn = 8.2 nF, Rsn = 0.5 Ω, Rgon = 5 Ω, Rgoff = 5 Ω, Vgon = +15 V, Vgoff = −5 V	No	4.0	8.0	5.5	842	902	2.99	7.17	10.17
Direct Drive	JFET Rgon = 1.05 Ω, JFET Rgoff = 1.65 Ω, JFET Vgon = 0 V, JFET Vgoff = 15 V, Si MOS Vg = 15 V (stay on)	Yes	8.0	8.0	4.09	862	806	3.47	5.55	9.02

The JFET direct drive method showed the lowest overall switching loss of 9.02 mJ. Compared with the other two methods, this method required negative voltage for driving the SiC JFET, as well as an enable signal for the Si MOS at circuit start up, adding some complexity to the gate drive. The standard **onsemi** JFETs do not provide access to the JFET gate, but a new dual-gate TO247-4L product is under development, which has both SiC JFET gate and Si MOS gate and would be suitable for JFET direct drive. This method would also be suitable for modules, where a separate JFET gate pin can be added. As shown in this study, the JFET gate path can tolerate reasonable amount of parasitic inductance (20 nH in SPICE), so it would be feasible to have the JFET gate driver placed on the gate drive PCB board that is on top of the module.

The external CGD and device RC snubber methods showed higher switching loss, but they did not require access to the JFET gate. Both methods can be easily implemented on the PCB, when using **onsemi** JFETs in discrete packages (e.g. TO247). Since both methods can tolerate a reasonable amount of parasitic inductance (20nH in SPICE), they would also be suitable for modules with **onsemi** chips inside.

One drawback of the RC snubber method was that it cannot adjust turn-off and turn-on dV/dt independently. As shown in Table 1, to achieve turn-on dV/dt of 8 V/ns, the turn-off dV/dt had to be reduced to 4 V/ns, which increased EOFF.

However, they can be adjusted independently using a separate R_{GON} and R_{GOFF} for external C_{GD} and JFET direct drive methods. As shown in Table 1, turn-off and turn-on dV/dt of 8 V/ns was achieved by optimizing R_{GON} and R_{GOFF} separately.

Summary

In summary, with these simple techniques, good dV/dt control can be achieved. The **onsemi** JFET advantages of lower conduction loss and good short-circuit robustness are paramount to efficient and reliable motor drive applications.

References

[1] A. Binder, “High frequency effects in inverter-fed AC electric machinery”

[2] Link to UF3SC120009K4S detail: https://www.onsemi.com/products/discrete−power−modules/silicon−carbide−sic/silicon−carbide−sic−cascode−jfets/UF3SC120009K4S

[3] Zhongda Li: Using SiC JFET Spice Model in LTSPICE, Application Note: AND90315/D

[4] Mike Zhu: Switching Fast SiC Cascode JFETs with a Snubber, Application Note: AND90319/D

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