Switching Characteristics of onsemi Gen3 SiC Cascode JFETs at Elevated Temperatures

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INTRODUCTION

One unique characteristic of **onsemi** Gen 3 SiC Cascode JFETs is that its switching losses and Qrr decrease at elevated temperature, making the device more efficient once it heats up. This paper explains in detail the reason behind this characteristic.

One characteristic of the **onsemi** Gen 3 SiC Cascode JFET is that its switching losses and Qrr decreases at elevated temperatures. As shown in Figure 1, the measured Eon, Eoff, and Qrr of the 1200 V 35 m SiC Cascode JFETs UF3C120040K4S decreased with increasing temperature and flattened out around 100 °C [1].

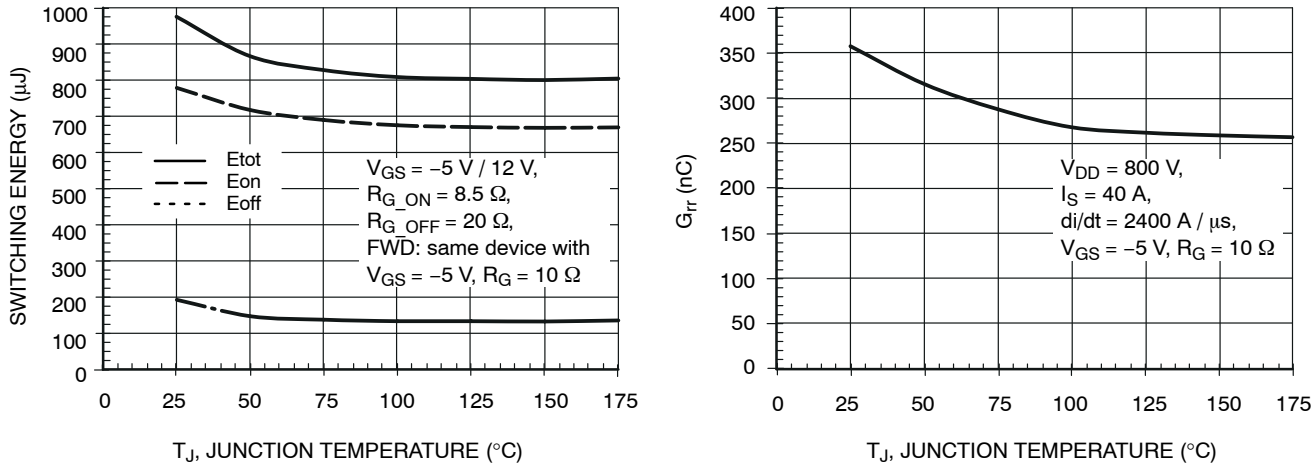

Figure 1. Eon, Eoff and Qrr vs Temperature of UF3C120040K4Sr

The reason is that the Gen 3 SiC Cascode JFET switching became faster at elevated temperature. The SiC Cascode JFET consists of SiC JFET and Si MOSFET connected in the cascode configuration, as shown in Figure 2. The overall switching speed of SiC JFET is affected by both SiC JFET internal Rgj, and the Si MOSFET external gate resister Rg, ext. The Rg, ext can be selected by the user to achieve the desired switching speed, and the recommended Rg,ext values can be found in **onsemi** SiC JFET User Guide [2].

The SiC JFET internal Rgj inherently decreases by a small amount with temperature and stabilizes above 100 °C, which is related to the increase in conductivity of p-type SiC in the gate region of the JFET. The decrease in Rgj leads to faster switching and lower losses.

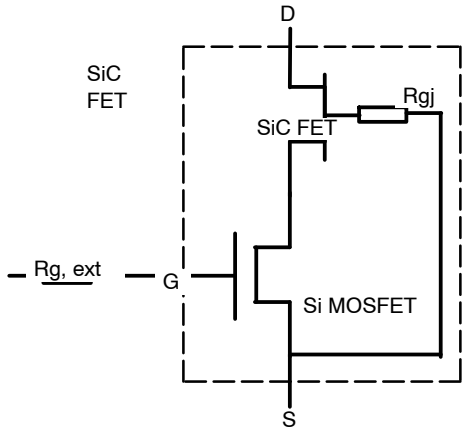

Figure 2. The Internal Cascode Structure of onsemi SiC FET

Using SPICE simulations, we can better understand how JFET Rgj affects the switching speed of the SiC FET. Simulated switching waveforms of two cases with high and low JFET Rgj were overlapped in the same plots for easy comparison. The higher Rgj value represents the JFET Rgj at room temperature, and the lower Rgj represents elevated temperature.

The turn-off I_{DS} and V_{DS} waveforms were shown in Figure 3. With lower JFET Rgj at elevated temperature, the turn-off dv/dt was faster, which resulted in smaller rise time (tr) and shorter overlapping time of I_{DS} and V_{DS}. As a result, the turn-off switching loss Eoff was lower.

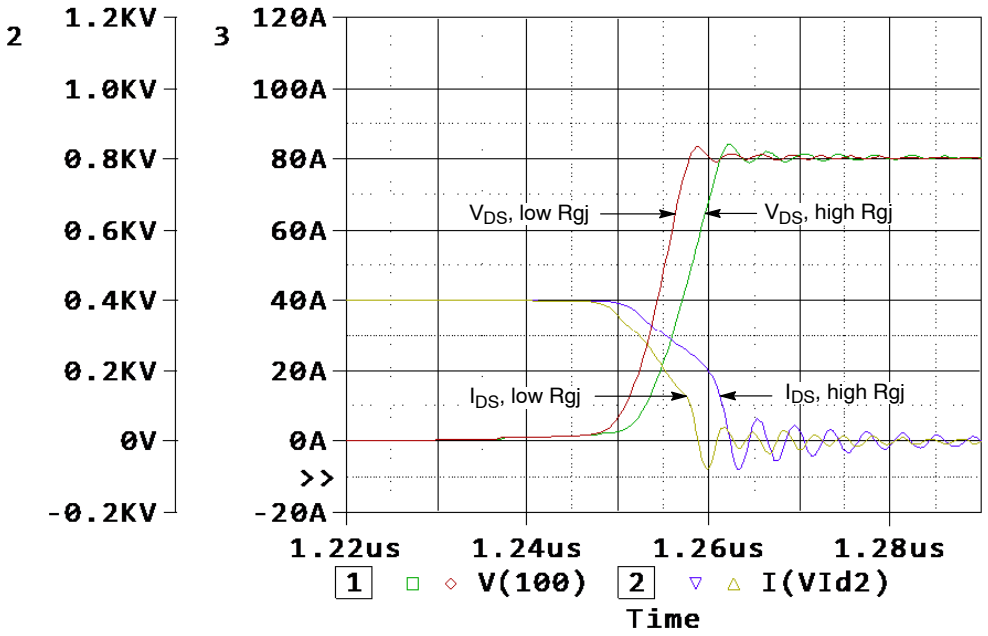

Figure 3. Turn-Off Waveforms of I_{DS} and V_{DS} of Two SiC FETS with High and Low JFET Rgj

The turn-on I_{DS} and V_{DS} waveforms were shown in Figure 4. With lower JFET Rgj at elevated temperature, the turn-on di/dt was about the same, but the dv/dt was faster. The faster dv/dt reduced the overlapping time of I_{DS} and V_{DS}, which reduced the turn-on switching loss Eon. It can be seen from Figure 4 that the lower JFET Rgj at higher temperature reduces the I_{RM} and Q_{RR}.

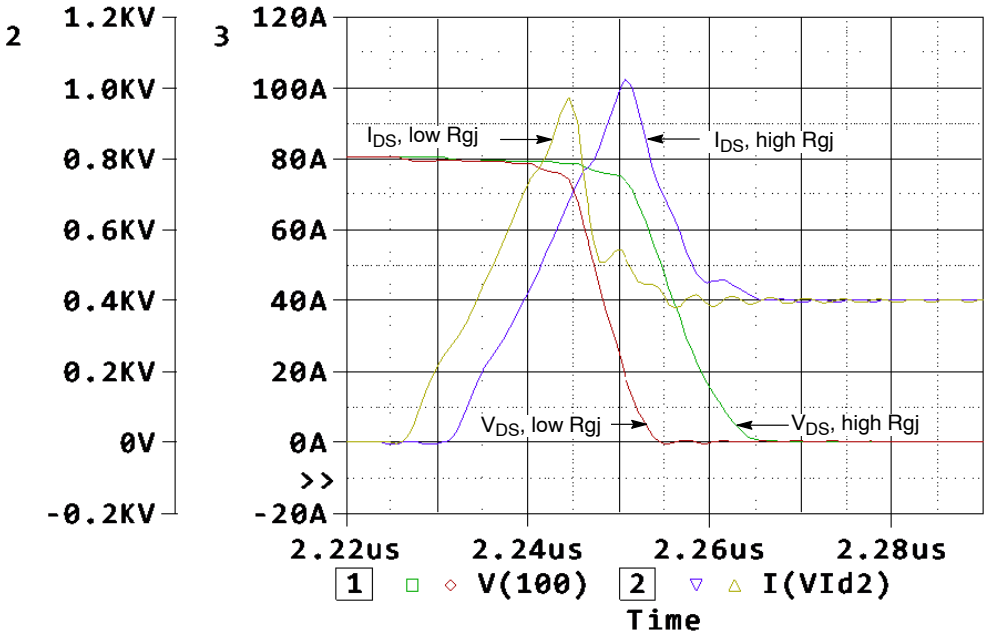

Figure 4. Turn-On Waveforms of I_{DS} and V_{DS} of Two SiC FETS with High and Low JFET Rgj

REFERENCES:

[1] UF3C120040K4S – Data Sheet
[2] UM70114/D – SiC Cascode JFET & Module User Guide

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
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