Migrating from NCN5192 to NCN5193

AND90268/D

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Introduction

The NCN5192 and NCN5192 are single−chip modems for the HART protocol. The ICs are closely related and are mostly compatible. However, the designer needs to account for a few differences, as described in this application note.

In case of doubt, contact your sales representative for a schematic and layout review.

Power Supply and Micro−controller Interface

The NCN5192 is designed to interface with micro−controllers with 3.3–5 V IOs; the NCN5193 for 1.8–3.3 V IOs. Refer to table 1 for details. Note the NCN5193 has slightly more demanding input−voltage requirements (Table 1, V_{IL} and V_{IH}). Both should work with normal 3.3 V IOs.

Table 1. SUPPLY AND PARAMETRIC DIFFERENCES

Parameter	Symbol	NCN5192	NCN5193
Absolute Maximum Rating	V_{DD}	6 V	4 V
Micro−controller Interface		3.3–5 V	1.8–3.3 V
Logic Input Voltage, Low	V_{IL}	0.3 × V_{DD}	0.2 × V_{DD}
Logic Input Voltage, High	V_{IH}	0.7 × V_{DD}	0.8 × V_{DD}
Logic Output Voltage, Low	V_{OL}	0.4 V	0.4 V
Logic Output Voltage, High	V_{OH}	2.4 V	V_{DD} − 0.4 V
Total Supply Current	I_{DD}	600 μA (max.)	500 μA (max.)
DAC Resolution		16 bit (nom.)	17 bit (nom.)
CBIAS Resistor		(V_{AREF} / 2.5 μA) ±5%	(V_{AREF} / 2.5 μA / 4) ±5%
Refresh of Watch−dog Timer		KICK pin	KICK pin; SDR write

The NCN5193 is slightly more power efficient (Table 1, I_{DD}).

The current for the comparator bias has been changed; now V_{CBIAS} equals V_{AREF} / 4, instead of V_{CBIAS} = V_{AREF} in the NCN5192. As a consequence, the resistor on CBIAS needs to have a quarter of the resistance required for the NCN5192.

If during the migration V_{DD} is changed, the resistor divider on the VPOR pin may need to be recalculated to obtain the desired power−on reset (POR) voltage.

The NCN5193 may also be configured to reset the watch−dog timer when the sigma−delta data register (SDR) is written. The bit GCR.WDT_KICK must be set to 2 to enable this.

Clock Source

The NCN5193 still may be used with an external clock or a crystal; however, the MODE pin must now be set to match this.

The NCN5193 supports an additional oscillator−frequency option (3.68 MHz) and is slightly more tolerant to jitter when an external clock input is used.

The CLK2 output is no longer constrained to 460.8 kHz as in the NCN5192; any divider value may be programmed in the CCR register.

IC Pins and External Components

When migrating to the NCN5193, note the pin differences shown in Table 2.

Table 2. PIN DIFFERENCES

Pin Number	NCN5192	NCN5193
12	VSSA	RxAN
19	VSSA	VSS
20	VSS	TEST1
21	VDD	TEST2
27	RxD_ENH	MODE

Pins 19–21 have changed function, but the connections on the printed circuit board (PCB) remain the same: pin 19 and 20 should still be connected to ground, pin 21 to VDD.

Pin 12 no longer connects to analogue ground, but to an additional input to the receive filter. The pin should be connected to a resistor divider network part of the feedback loop of the filter; refer to Figure 2 in the data sheet of the NCN5193. A few additional external passive components are needed for the filter (C5, C6, R8, and R9 in the data sheet, Figure 2).

Pin 27 is no longer a digital output going to the microcontroller, but the MODE clock−selection pin. The MODE pin must be pulled low or high, either by hardwiring it to VSS or VDD on the PCB or controlled by the micro−controller. To use a crystal oscillator, connect MODE to VSS.

The behaviour of NCN5192's RxD_ENB pin is identical to it's RxD pin, except that for the state when idle: when no carrier is detect, the RxD_ENB pin remains high while RxD is by default low.

The NCN5193 does not have an RxD_ENB pin. However, the RxD pin can be configured to behave as RxD_ENB by setting the GCR.RXD_IDLE bit. This changes the idle state of RxD from low to high.

Register Structure

The NCN5192 has a single 8−bit configuration register; instead, the NCN5193 has three registers: CCR, GCR, and ACR. Refer to the data sheet for details.

In addition, the NCN5193 has a 17−bit ΣΔ DAC instead of the 16−bit DAC of the NCN5192. As a consequence, the 16−bit data register has been expanded to a 24−bit data register.

ADDITIONAL INFORMATION

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