NCN26000 – Getting Started Basic Configuration, Communication and Exception Handling

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Introduction

The NCN26000 10BASE−T1S Physical layer (PHY) device has been developed to adhere to the IEEE 802.3cg specifications, with various optional additional capabilities.

For correct and reliable operation, there are a few things to keep in mind when configuring NCN26000, especially since the device cannot participate in communication in a multi−drop segment without correct configuration. Also, there is a risk of permanently disrupting the entire segment in the event of improper configuration.

This application note is intended to provide users with a guideline for configuring NCN26000 for their specific application.

Only the basic settings needed are described here, and these are discussed using configuration examples.

Reference Documents

[1] IEEE802.3cg−2019
"IEEE Standard for Ethernet
Amendment 5:
Physical Layers Specifications and Management Parameters for 10 Mb/s Operation and Associated Power Delivery over a Single Balanced Pair of Conductors"
IEEE Computer Society, ISBN
978−1−5044−6420−8

Operating Modes

NCN26000 offers mandatory and optional operating modes as defined in the IEEE 802.3cg Standard as well as some features that offer extended functionality:

- CSMA/CD as the Basic Operation and Fall Back
- Physical Layer Collision Avoidance (PLCA)
  - Burst Mode
  - Precedence Mode
- Enhanced Noise Immunity (ENI)

As a PHY device, the NCN26000 integrates a 10BASE−T1S Physical Layer Device and needs to be connected to a Clause 4 compliant MAC (Media Access Controller) offering MII (Media Independent Interface) and MIIM (MII Management, often referred to as MDIO) interfaces. Such Media Access Controllers are typically implemented in higher complexity microcontrollers and SoC devices available from various sources.

Some design choices taken by **onsemi** allow NCN26000 to work with standard drivers available from the MCU vendors with very little to no configuration**.**

To illustrate the basic use of the part, this application note starts with discussing how to read and write configuration registers.

Further down in the text a set of basic configurations will be explained.

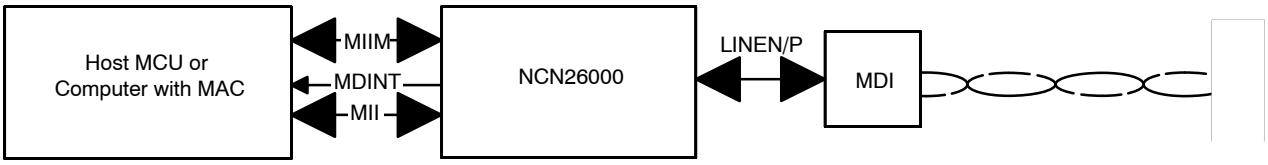

Figure 1. Simplified Block Diagram

MIIM Interface

To query the status of the NCN26000 and for configuration, NCN26000 has a Media Independent Interface Management (MIIM) interface, which is defined by the IEEE. This interface is also referred to as Serial Management Interface (SMI) or Management Data Input/Output (MDIO). For details on MIIM, refer to [1], section 22.

The MDIO protocol distinguishes between access to basic registers and extended registers. Since NCN26000 is a 10BASE−T1S device that also supports PLCA, both base and extended register sets are used. Extended registers are accessed through an indirect access mechanism as explained in Section 22.2.4.3 of the IEEE802.3 standard [1]. In most cases, a host that contains a MAC also has the MIIM. Therefore, this Application Note does not discuss the MIIM interface in detail, but only highlights the points necessary to understand and perform register access for both Basic and Extended Capability registers.

Basic Capability Register Access (Clause 22)

Access to the Basic Capability registers of the NCN26000 is simple, the address space contains 32 registers which can be accessed by direct addressing. We assume that the user knows the MDIO format and how to read and write the registers of clause 22 in the host of own preference (see also 22.2.4.5 in [1]). A list of the available registers can be found in the NCN26000 data sheet.

The management frame format for MIIM according to clause 22 is shown in the table below:

Table 1. MANAGEMENT FRAME FIELDS

	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
Read	1…1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
Write	1…1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

PRE: This is the 32−bit long preamble. Typically, the MDIO is pulled up with an external pull−up resistor so that the STA (the host initiating an MDIO transaction) does not have to actively send the preamble but must wait 32 bits between two consecutive transactions without actively controlling the MDIO bus.

ST: Start Frame Delimiter, driven by the host.

OP: Operation the host wants to perform on the PHY register, either read or write.

PHYADD: the address of the PHY device that the host wants to address. For details on setting the PHYADDRESS through bootstrapping, refer to the NCN26000 datasheet. Note that a Managing Station (STA) can address up to 32 PHY devices. This is useful for hosts with more than one Ethernet port (e.g., switches).

REGADD: the address of the register within the PHY device that the host wishes to read from or write to.

TA: Turnaround. Allows the PHY device a certain time to take control of the MDIO bus (basically a bit time).

DATA: Register contents to be written (controlled by the STA) or read (controlled by the PHY device).

Extended Capability Register Access

Access to the NCN26000 extended capability registers can only be done by indirect addressing as described in Section 22.2.4 in [1]. Indirect access to the Extended Capability Registers is through both Basic Capability Registers 13 and 14.

Clause 45 (802.3ae, 10GBASE−xx) originally introduced the idea of MMD (MII Manageable Device). This must be considered as different functional blocks within PHY devices such as NCN26000. For this reason, the Extended Capability registers are often referred to as Clause 45 registers, while lower speed PHY devices such as NCN26000 do not allow direct access to these registers because the Claus 45 protocol is not implemented (even in 10/100Mbit MACs).

NCN26000 has these MMDs:

MMD 1: PMA functions

MMD 3: PCS functions

MMD 30: Vendor specific registers

MMD 31: PLCA functions and vendor specific registers

For most configurations, MMD 31 (PLCA) and MMD 1 (enhanced noise immunity) are the most important. The NCN26000 data sheet contains a detailed list and description of all available registers and the fields and flags they contain.

Clause 22 Register 13 is used to define the desired operation and MMD, while Register 14 contains the address or data (read or write).

To read an Extended Capability Register (register defined in clause 45), four consecutive transactions must be performed by the host on the MIIM.

1. Write: FN = 00 (address) and desired MMD in register 13.
2. Write register address into register 14
3. Write FN = 01 (data) and desired MMD (as in step 1) into register 13
4. Read the register data from register 14

Similarly, a write of any register is also performed in four steps:

1. Write: FN = 00 (address) and desired MMD into register 13.
2. Writing the register address into register 14
3. Writing FN = 01 (data) and desired MMD (as in step 1) into register 13
4. Write the register data into register 14. This actually writes the data into the register with the MMD and the address specified in step 2.

This allows reading, modifying, and writing to be done in only 5 steps:

1. Write: FN = 00 (address) and desired MMD into register 13.
2. Writing of the register address into register 14.
3. Writing: FN = 01 (data) and desired MMD (as in step 1) into register 13.
4. Reading the register data from register 14.
5. Writing the changed data into register 14.

Example: the user wishes to configure the NCN26000 to run in PLCA mode with the PLCA ID set to 0 (coordinator) and a maximum node count of 16 (0x10).

Consulting the NCN26000 datasheet it becomes apparent that two (clause 45) registers need to be written to:
PLCA Control 1 and PLCA Control 0, located in MMD31 at address 0xCA02 and 0xCA01.

PLCA Control 1 would need to be set to 0x1000
PLCA Control 0 would need to be set to 0x8000

The fastest way to achieve this is taking use of the autoincrement feature for indirect register addressing, built into the Cause22 to clause 45 bridge inside the NCN26000. The OP code in register 13 can therefore be either 0b11 (Data Reg with Post Increment on writes only) or 0b10 (Data Reg with Post Increment on read & write). For this example, we use a PHY address of 0.

1st Step: set the address to CA01 (PLCA CNTLR 0) by writing:

- 0b0000000000011111 (0x 001F) into Register 13. This sets the MMD 31 and prepares register 14 to specify the address
- 0xCA01 into Register 14

2nd Step: write 0x8000 into PLCA CONTROL 0 by writing:

- Write 0x8000 into PLCA CONTROL 0 by writing: 0b0b1100000000011111 (0xC01F) into Register 13, which prepares the NCN26000 to store data into the register specified in step 1.
- 0x8000 into register 14. Noter that we used post write increment, so the next address (0xCA02) after this write will point to MMD31 at 0xCA02

3rd Step: write 0x0F00 into register PLCA CONTROL 1 by writing:

- 0x0F00 to Register 14.

Basic Configuration

This section discusses the minimum configuration settings required to use the NCN26000 as well as some of its optional features. It starts with the simple case of CSMA/CD and then discusses how to enable additional features:

- PLCA
  - Coordinator mode
  - Follower mode
  - Burst mode
- Enhanced Noise Immunity

Configuring NCN26000 for the simplest form of operation means setting it to strictly work in CSMA/CD (carrier sense multiple access / collision detection) mode, this is the default when bootstrapping the NCN26000 to “NORMAL” operation mode.

Hosts would simply set these bits the PHY Control register (clause 22 address 0) to the values shown below:

Bit 14 = 0: loopback mode disabled

Bit 12 = 1: PHY transmit/receive enabled

Bit 10 = 0: PHY set to NORMAL mode.

Bit 9 = 1: reset link status

Bit 7 = 0: Normal Operation

A writing 0x1200 into the PHY Control Register will set all the above bits to their proper state.

A connected host might need to use link information from the PHY to make appropriate setting to its Media Access Controller. To gain the needed information, read the PHY control register. The table below explains the bits and their content.

Table 2.

Bits	Value	Description
13.6	0.0	Link speed is 10 Mb/s
8	0	Link is Half−Duplex

In summary, basic operation can be achieved by using the configuration shown in the table below, when writing the registers in the order shown (we refer to this as the configuration “card”).

Table 3. MINIMUM CSMA/CD CONFIGURATION

Order	MMD	ADDR	DATA	Comment
1	BASIC	0	0x1200	Reset, non−Isolate, PHY TX/RX enabled

Note that the above lists show the bare minimum that needs to be sent to the device after reset to allow the PHY to participate in communication over the single pair Ethernet medium and with the host Computer or MCU MAC.

Adding PLCA

When we want the device to be part of a PLCA enabled network, we need to configure and enable the functions of the PLCA Reconciliation Sublayer (RS) inside the NCN26000 PHY. Please consult [1] Clause 148 for a detailed description of Physical Layer Collision Avoidance (PLCA). In a PLCA enabled collision domain, there needs to be one so−called Coordinator. This is typically the device that is assigned the PLCA ID=0. The Leader is the station that starts PLCA cycles by submitting the BEACON signal on the line.

The leader will also need to be configured with a maximum node number that needs to be equal or higher than the highest ID assigned to any station participating in the local collision domain.

When we want the part to be a Follower node, we must assign it a local ID and enable PLCA.

This is done by setting the appropriate node ID in the PLCACTRL1 register (bits 7:0) and enable PLCA (bit 15) in the PLCACTRL0 register.

As an example, assume we chose ID=7 for the node we configure. The configuration card from the previous example must be extended and will now look like this (lines in red show the added configuration items):

Table 4. MINIMUM PLCA FOLLOWER NODE CONFIGURATION

Order	MMD	ADDR	DATA	Comment
1	BASIC	0	0x1200	Reset, non−Isolate, PHY TX/RX enabled
2	31	0xCA02	0x0007	Set PLCA ID to 7
	31	0xCA01	0x8000	Enable PLCA
3	BASIC	0x0	0x1000	Activate Link

The order of register writes in step two of the above configuration could be reversed (start with 0xCA01) to allow an auto−increment write to the registers, which reduces the number of MDIO transaction as explained earlier.

When instead we want to configure the node to be the PLCA coordinator, the local ID is set to 0 and the maximum node count needs to be set to a reasonable number (8 or larger).

Assume we want to set up a coordinator that supports 8 nodes in the collision domain (the multi−drop sequence). The configuration card will change to the one shown below:

Table 5. MINIMUM PLCA COORDINATOR NODE (NODE COUNT 8)

Order	MMD	ADDR	DATA	Comment
1	BASIC	0x0	0x1600	Reset
2	31	0xCA02	0x0800	PLCA ID = 0 Node Count = 8
	31	0xCA01	0x8000	Enable PLCA
3	BASIC	0x0	0x1000	Activate Link

We can add more configuration options following this principle. For instance, PLCA has additional options that can be enabled to deal with specific situations in applications that have an uneven spread of sent data from different stations. For example, if a particular station needs to send twice the amount of data than all others, it could be allowed to send two or more frames per PLCA transmit opportunity instead of only one. This is supported by enabling the PLCA burst mode (see [1] Clause 148.4.4.2). Burst mode is enabled by setting the maximum burst count (the number of additional Ethernet frames that may be transmitted during a single transmit opportunity) bits 15:8 to the number of additional frames a station can send per transmit opportunity. When we want to allow the station to send two frames per TO (Transmit Opportunity), we need to set the MAXBC inside the PLCABURST register to 1. Hence the configuration card will change to:

Table 6. PLCA COORDINATOR NODE (NODE COUNT 8) WITH BURST ENABLED

Order	MMD	ADDR	DATA	Comment
1	BASIC	0x0	0x1600	Reset
2	31	0xCA02	0x0800	PLCA ID = 0 Node Count = 8
	31	0xCA05	0x0180	Allow one extra frame per TO
	31	0xCA01	0x8000	Enable PLCA
3	BASIC	0x0	0x1000	Activate Link

Enhanced Noise Immunity Mode

In applications that are exposed to an elevated level of noise on the Single Pair Ethernet line (e.g., close to motors or AC lines, or multiple SPE connections bundled in a single multi twisted pair cable) NCN26000 provides superior performance by offering a non−standard feature called Enhanced Noise Immunity (ENI). ENI works without side effects in PLCA enabled network segments. When activating ENI in CSMA/CD operation, the station's ability

to detect collisions will slightly degrade, however ENI will not break communication on the network.

Enabling ENI can be done by simply setting bit 7 in the PHYCFG1 register (MMS 31, address 0x8001).

Along with ENI, Collision Masking allows even better noise performance by avoiding excessive noise being mistakenly considered as collision (only works with PLCA).

Adding this to the previous example will make the configuration card look like this:

Table 7. PLCA COORDINATOR NODE (NODE COUNT 8) WITH BURST ENABLED AND ENI AND COLLISION MASKING

Order	MMD	ADDR	DATA	Comment
1	BASIC	0x0	0x1600	Isolate Mode
2	31	0xCA02	0x0800	PLCA ID = 0 Node Count = 8
	31	0xCA05	0x0180	Allow one extra frame per TO
	31	0xCA01	0x8000	Enable PLCA
	31	0x8001	0x0081	Enable ENI & Collision Masking
3	BASIC	0x0	0x1000	Activate Link

All these examples demonstrate the use of configuration registers, as described in the Datasheet of NCN26000, to set the part into simple and advanced modes of operation. Users are invited to explore more of the part's capabilities by studying the NCN26000 datasheet.

Handling Exceptions

The following is a guide on potential actions to take when the NCN26000 signals errors or exceptions to the host. The content of this section should be regarded as recommendations, as there will be a multitude of different possible action that could result from errors or exceptions reported by NCN26000 depending on the application's needs.

Whenever NCN26000 needs to notify the host of occurring events, it will assert the MDINT pin to trigger an interrupt event in the software running on the host. Depending on the configuration, MDINT can issue notifications for the following exceptions and events:

Table 8.

Name	Description
Physical Collision	When in PLCA, a physical collision should not happen. However, the MAC will see collisions, when the NCN26000 does not hold a Transmit opportunity while the MAC wants to send a packet. This is referred to as a logical collision to make the host defer the transmission to the NCN26000 until a valid transmit opportunity becomes available. A high frequency of Physical Collision may point to: – Excessive noise – Missing or wrong termination – Wrong or incomplete PLCA setup – A CSMA/CD station on the line The use of Enhanced Noise Immunity might help reducing the number of physical collisions in case they are caused by long cables and high noise.
PLCA Recovery	When enabled, a MDINT is issued on every PLCA Recovery event. PLCA recovery is flagged when a false carrier event (e.g., impulse noise) occurs on the line. When a CRS event is not followed by the reception of a packet within a certain amount of time the NCN26000 goes to either of two states, depending on its PLCA settings: When configured as coordinator node, it waits for the line to be quiet for a certain amount of time and then sends a new BEACON. When not configured as a coordinator node, NCN26000 will wait for a BEACON before getting a new transmit opportunity. Consider enabling enhanced noise immunity mode (ENI) if PLCA recovery gets flagged frequently.
Remote Jabber	A remote jabber condition occurs if a station transmits for longer than a maximum length Ethernet frame transmit duration (2000 bytes, including FCS).
Local Jabber	Same as Local Jabber but in TX direction.
PLCA Status Charge	Issued every time that the PLCA status changes. This can be an indication for PLCA activity on the line.
Link Status Change	Indicate a change in the Link Status, ether from up to down or vice versa.

Note that the MIIM IRQ Control Register (address 16) is used to enable or disable MDINT events selectively.

By default, none of the above−mentioned events will trigger MDINT. It will be up to the user of the NCN26000 to determine which of the notifying events are needed in the application.

Once enabled, an event will need to be identified by reading the MIIM IRQ Status Register (address 17) after MDINT triggered. The MIIM IRQ Status Register latches the events until the register is read, this prevents the events of interest (those enabled in the IRQ control register) to go unnoticed.

In all cases MDINT is asserted after a hardware or power−on reset. It is therefore good practice to read the MIIM IRQ status register when initializing the NCN26000 and then write bit 15 of the MIIM IRQ Status register to one after the initialization is done.

Summary

In this application note, we have outlined the basic use and configuration of the IEEE802.3cg 10Base−T1S Multi−Drop Ethernet PHY NCN26000. We also give guidance on how to setup optional and proprietary features as well as some guidance on how to handle / avoid errors and exceptions.

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