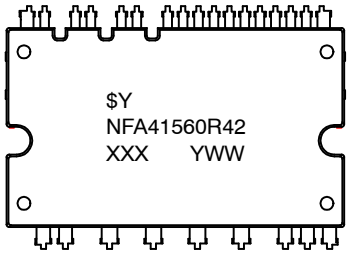
Smart Power Module (SPM), Motion SPM® 45 Version 4 Series Application Note

AND90185/D

3D Package Drawing (Click to Activate 3D Content)

SPMAA−C26 / 26LD, PDD STD CERAMIC TYPE, LONG LEAD DUAL FORM TYPE CASE MODFC

MARKING DIAGRAM



$Y = **onsemi** Logo
NFA41560R42 = Specific Device Code
XXX = Trace Code
Y = Year
WW = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this application note.

Introduction

This application note provides practical guidelines for designing with the Motion SPM 45 Series power modules. This series of Intelligent Power Modules (IPM) for 3−phase motor drives contains a three−phase inverter stage, gate drivers and a thermistor.

Design Concept

The Motion SPM 45 design objective is to provide a minimized package and a low power consumption module with improved reliability. This is achieved by applying a new Insulated−Gate Bipolar Transistor (RC−IGBT) of advanced silicon technology, optimized gate drive ICs and improved ceramics substrate based on transfer mold package. The Motion SPM 45 achieves reduced board size and improved reliability compared to existing discrete solutions. Target applications are inverter motor drives for low and medium power motor drives such as washing machine, air conditioners and pumps. The temperature sensing function of Motion SPM 45 products are implemented in the isolated NTC thermistor to enhance the system reliability. Integrated thermistor temperature in module is provided for monitoring the module temperature and necessary protections against over−temperature situations.

Features

- 600 V 3−Phase Inverter with Integral Gate Drivers and Protection
- Low Thermal Resistance Using Ceramic Substrate
- Advanced Silicon Technology RC−IGBT for Low Power Loss and High Ruggedness
- Built−In Bootstrap Diodes and Dedicated VS Pins Simplify PCB Layout
- Separate Open−Emitter Pins from Low−Side RC−IGBTs for Three−Phase Current Sensing
- Single−Grounded Power Supply
- Isolation Rating: 2000 Vrms / Min.
- This is a Pb−Free Device

Related Source

- NFA41560R42 – *Smart Power Module Motion SPM® 45 V4*
- NFA42060R42 – *Smart Power Module Motion SPM® 45 V4*
- AN−9084 – *Smart Power Module Motion SPM® 45 V3 Series User's Guide*
- AN−9072 – *Smart Power Module Motion SPM® 45 Mounting Guidance*
- AN−9071 – *Smart Power Module Motion SPM® 45 Thermal Performance Information*
- *Motion Control Design Tool at* https://www.onsemi.com/site/design−tools/motion−control/

PRODUCT DESCRIPTION

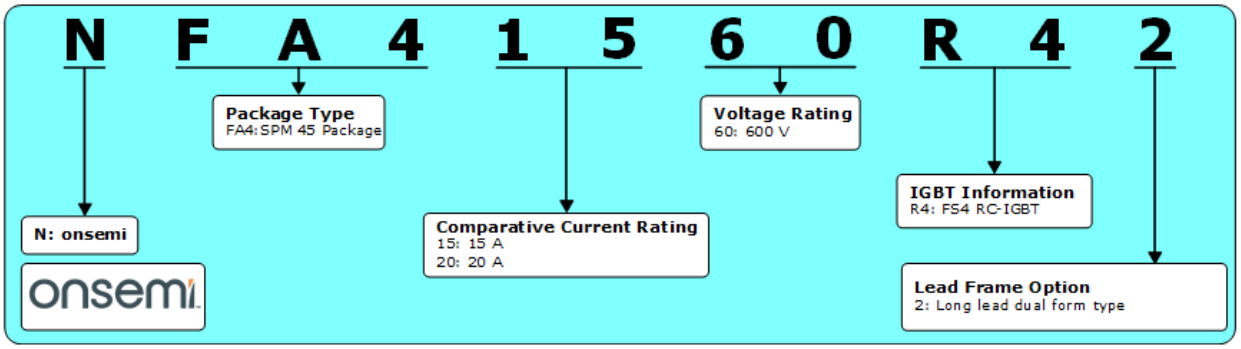


Figure 1. Ordering Information of SPM 45 Version 4

Product Line−Up

The Table 1 PRODUCT LINE−UP AND TARGET APPLICATION shows the SPM 45 version 4 basic line up without package variations. The products are an advanced Motion SPM 45 module providing a fully−featured, high−performance inverter output. Online simulation tool, Motion Control Tool is recommended to find out the right product for the desired application.

Table 1. PRODUCT LINE−UP AND TARGET APPLICATION

Product	Current / Voltage	Recommend Power (Note 1)	Target Application	Isolation Voltage
NFA41560R42	15 / 600	0.75 kW / 220 V_{AC}	Washing Machine, Air Conditioner	Viso = 2000 Vrms (Sine 60 Hz, 1−min between All Shorted Pins and Heat Sink)
NFA42060R42	20 / 600	1.50 kW / 220 V_{AC}		

1. These power ratings are simulated result by specific operating conditions, so it can be change by operating conditions

Internal Circuit and Integrated Function

Figure 2 shows the pin configuration and internal block diagram of Motion SPM 45 version 4 products.

The products adopt internal connection between VS and source terminal of high side RC−IGBTs to improve stray inductance effects. However, source terminal of low side RC−IGBTs is not connected to supply ground or bias voltage ground for current sensing circuit.

The Motion SPM 45 products include NTC thermistor and internal bootstrap diodes to generate the voltage needed for driving the high side RC−IGBTs. The NTC thermistor is the signal output pin for temperature sensing. The HVIC in Motion SPM 45 products have an internal level shift circuit for the high side drive signals allowing all control signals to be driven directly from ground levels such as the microcontroller. The Motion SPM 45 products are not required for additional isolation circuit from ground to high side drive thanks to the internal bootstrap diodes.

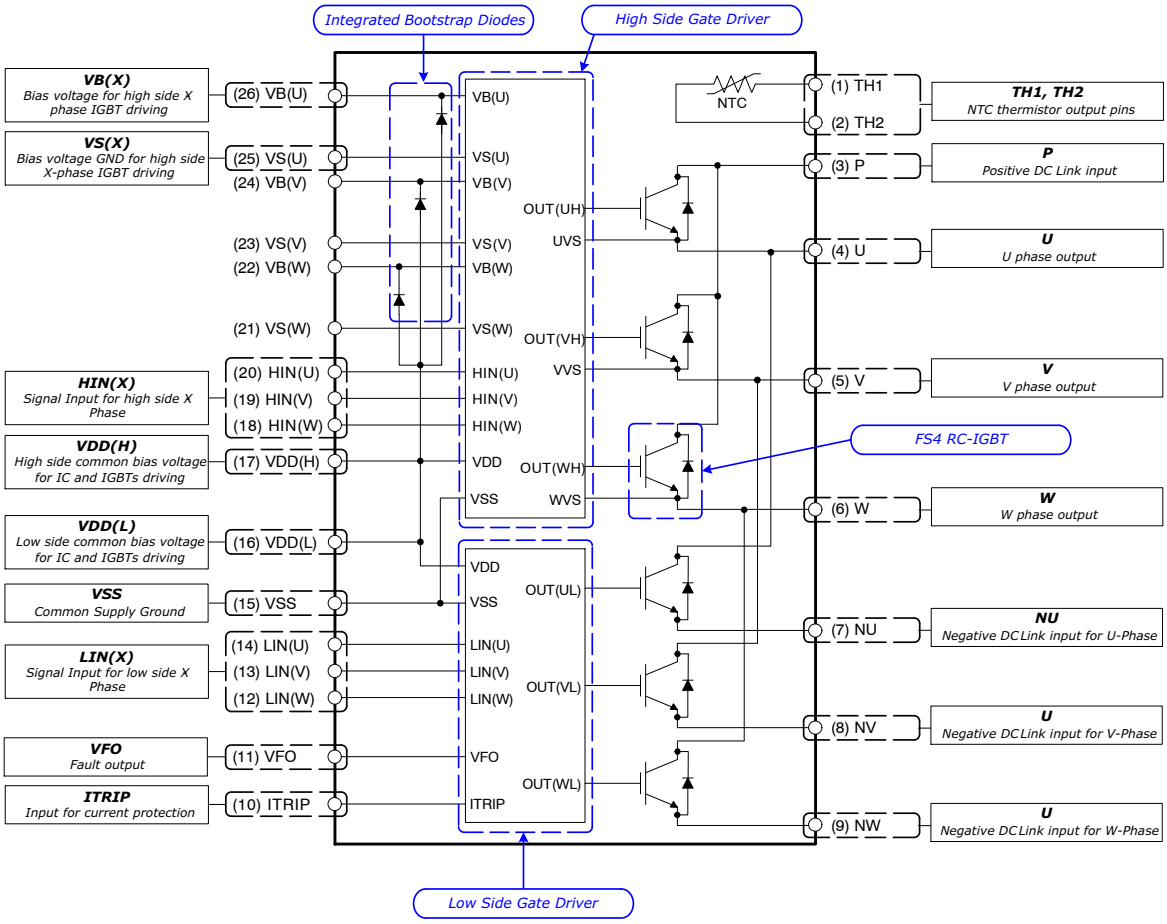


Figure 2. Internal Equivalent Circuit Diagram

Pin Description

Figure 3 shows package top view with pin assignment for MOTION SPM 45 version 4 product. The detailed functional descriptions are provided in Table 2. PIN DESCRIPTION.

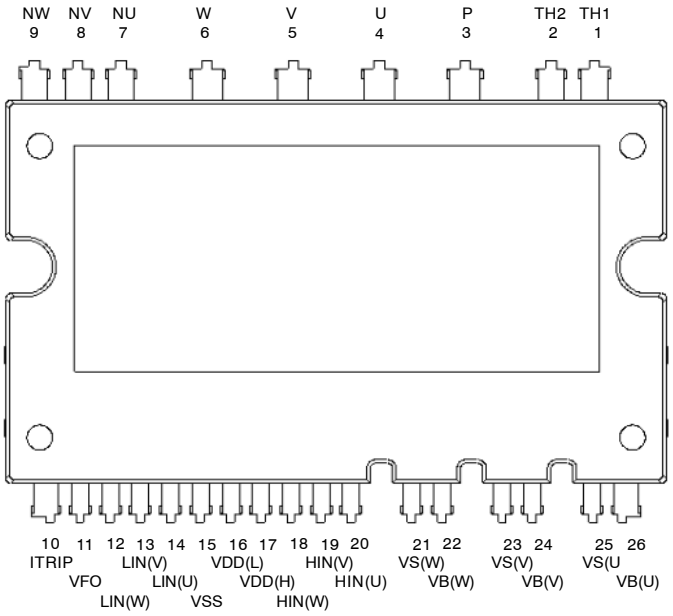


Figure 3. Package Top View with Pin Assignment

Table 2. PIN DESCRIPTION

Pin No.	Pin Name	Description
1	TH1	Thermistor Bias Voltage
2	TH2	Series Resistor for the Use of Thermistor (Temperature Detection)
3	P	Positive DC−Link Input
4	U	Output for U−Phase
5	V	Output for V−Phase
6	W	Output for W−Phase
7	NU	Negative DC−Link Input for U−Phase
8	NV	Negative DC−Link Input for V−Phase
9	NW	Negative DC−Link Input for W−Phase
10	ITRIP	Input for Current Protection
11	VFO	Fault Output
12	LIN(W)	Signal Input for Low−Side W−Phase
13	LIN(V)	Signal Input for Low−Side V−Phase
14	LIN(U)	Signal Input for Low−Side U−Phase
15	VSS	Common Supply Ground
16	VDD(L)	Low−Side Common Bias Voltage for IC and IGBTs Driving
17	VDD(H)	High−Side Common Bias Voltage for IC and IGBTs Driving
18	HIN(W)	Signal Input for High−Side W−Phase
19	HIN(V)	Signal Input for High−Side V−Phase
20	HIN(U)	Signal Input for High−Side U−Phase
21	VS(W)	High−Side Bias Voltage Ground for W−Phase IGBT Driving
22	VB(W)	High−Side Bias Voltage for W−Phase IGBT Driving
23	VS(V)	High−Side Bias Voltage Ground for V−Phase IGBT Driving
24	VB(V)	High−Side Bias Voltage for V−Phase IGBT Driving
25	VS(U)	High−Side Bias Voltage Ground for U−Phase IGBT Driving
26	VB(U)	High−Side Bias Voltage for U−Phase IGBT Driving

Detailed Pin Definition and Notification

- **Pins: VB(U)−VS(U), VB(V)−VS(V), VB(W)−VS(W)**
  - High−Side Bias Voltage Pins for Driving the IGBTs and High−Side Bias Voltage Ground Pins for Driving the IGBTs.
  - These are drive power supply pins for providing gate drive power to the high−side IGBTs.
  - The virtue of the ability to bootstrap the circuit scheme is that no external power supplies are required for the high−side IGBTs.
  - Each bootstrap capacitor is charged from the VDD supply during the on−state of the corresponding low side IGBT and low side diode.
  - To prevent malfunctions caused by noise and ripple in supply voltage, a good quality (low ESR, low ESL) filter capacitor should be mounted close to these pins.

- **Pins: VDD(L), VDD(H)**
  - Low−Side and High−Side Bias Voltage Pins.
  - These are control supply pins for the built−in ICs.
  - These two pins are connected internally.
  - To prevent malfunctions caused by noise and ripple in the supply voltage, a good quality (low ESR, low ESL) filter capacitor should be mounted close to these pins.

- **Pin: VSS**
  - Low−Side Common Supply Ground Pin.
  - The Motion SPM 45 product common pin connects to the control ground for the internal ICs.
  - Important! To avoid noise influences, the main power circuit current should not be allowed to blow through this pin.

- **Pins: LIN(U/V/W), HIN(U/V/W)**
  - Signal input pins.
  - These pins control the operation of the built−in IGBTs.
  - They are activated by voltage input signals. The terminals are internally connected to a Schmitt−trigger circuit composed of 5 V−class CMOS.
  - The signal logic of these pins is active high. The IGBT associated with each of these pins is turned ON when a sufficient logic voltage is applied to these pins.
  - The wiring of each input should be as short as possible to protect the Motion SPM 45 product against noise influences.
  - To prevent signal oscillations, an RC coupling is recommended.

- **Pin: ITRIP**
  - Short circuit and over current detection input pin.
  - The current−sensing shunt resistor should be connected between the low−pass filter before the ITRIP pin and the low−side ground VSS to detect short−circuit or over current.
  - The shunt resistor should be selected to meet the detection levels matched for the specific application. An RC filter should be connected to the ITRIP pin to eliminate noise.
  - The connection length between the shunt resistor and ITRIP pin should be minimized.

- **Pin: VFO**
  - Fault Output Signal Pin.
  - This is the fault output alarm pin. An active low output is given on this pin for a fault state condition.
  - The alarmed conditions are Over−Current Protection (OCP) or low−side bias Under−Voltage Lockout (UVLO) operation.
  - The VFO output is open−drain configured. The VFO signal line should be pulled up to the 5 V logic power supply with approximately 4.7 kΩ resistance.

- **Pin: TH1**
  - Thermistor Bias Voltage.
  - This is the bias voltage pin of the internal thermistor. It should be connected to the 3.3 V or 5 V logic power supply.

- **Pin: TH2**
  - Series Resistor for the Use of Thermistor (Temperature Detection).
  - For case temperature (Tc) detection, this pin should be connected to an external series resistor.
  - The external series resistor should be selected to meet the detection range matched for the specification of each application.

- **Pin: P**
  - Positive DC−Link Pin.
  - This is the DC−link positive power supply pin of the inverter.
  - It is internally connected to the collectors of the high−side IGBTs.
  - To suppress the surge voltage caused by the DC−link wiring or PCB pattern inductance, connect a smoothing filter capacitor close to this pin (typically, metal film capacitors are used).

- **Pins: NU, NV, NW**
  - Negative DC−Link Pin.
  - These are the DC−link negative power supply pins (power ground) of the inverter.
  - These pins are connected to the low−side IGBT emitters of the each phase.

- **Pins: U, V, W**
  - Inverter Power Output Pin.
  - Inverter output pins for connecting to the inverter load (e.g. motor).

PRODUCT SYNOPSIS

Absolute maximum ratings, electric characteristics, recommended operating conditions and mechanical characteristics are focused on in this section. Please refer to respective datasheets for the detailed description of each product.

Table 3. ABSOLUTE MAXIMUM RATINGS (Tj = 25°C, unless otherwise noted)

Symbol	Parameter	Conditions		Rating	Unit
INVERTER PART					
VPN	Supply Voltage	Applied between P – NU, NV, NW		450	V
VPN(surge)	Supply Voltage (Surge)	Applied between P – NU, NV, NW		500	V
Vces	Collector – Emitter Voltage			600	V
±Ic	Each IGBT Collector Current	Tc = 25°C, Tj < 150°C	NFA41560R42	15	A
			NFA42060R42	20	
±Icp	Each IGBT Collector Current (Peak)	Tc = 25°C, Tj < 150°C, Under 1 ms Pulse Width	NFA41560R42	30	A
			NFA42060R42	40	
Pc	Collector Dissipation	Tc = 25°C Per One Chip (Note 2)	NFA41560R42	45	W
			NFA42060R42	58	
Tj	Operating Junction Temperature			– 40~150	°C
CONTROL PART					
VDD	Control Supply Voltage	Applied between VDD(H), VDD(L) – VSS		20	V
VBS	High–Side Control Bias Voltage	Applied between VB(X) – VS(X)		20	V
VIN	Input Signal Voltage	Applied between HIN(U/V/W), LIN(U/V/W) – VSS		–0.3~VDD + 0.3	V
VFO	Fault Output Supply Voltage	Applied between VFO – VSS		–0.3~VDD + 0.3	V
IFO	Fault Output Current	Sink Current at VFO pin		1.0	mA
VITRIP	Current–Sensing Input Voltage	Applied between ITRIP – VSS		–0.3~VDD + 0.3	V
BOOTSTRAP PART					
VRRM	Maximum Repetitive Reverse Voltage			600	V
If	Forward Current	Tc = 25°C, Tj < 150°C		0.5	A
Ifp	Forward Current (Peak)	Tc = 25°C, Tj < 150°C, Under 1 ms Pulse Width (Note 2)		2.0	A
Tj	Operating Junction Temperature			–40~150	°C
TOTAL SYSTEM					
VPN(PROT)	Self–Protection Supply Voltage Limit (Short–Circuit Protection Capability)	VDD = VBS = 13.5~16.5 V, Tj = 150°C, Vces < 600 V, Non–Repetitive, < 2 μs		400	V
Tstg	Storage Temperature			–40~125	°C
Viso	Isolation Voltage	60 Hz, Sinusoidal, AC 1 minute, Connection Pins to Heat Sink Plate		2000	V_{rms}

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. These values had been made an acquisition by the calculation considered to design factor.

Table 4. ABSOLUTE MAXIMUM RATINGS (Tj = 25°C, unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
THERMAL RESISTANCE							
Rth(j−c)Q	Junction to Case Thermal Resistance (Note 3)	Inverter IGBT Part (per 1/6 module)	NFA41560R42	–	–	2.75	°C/W
			NFA42060R42	–	–	2.13	
Rth(j−c)F		Inverter FWDi Part (per 1/6 module)	NFA41560R42	–	–	4.20	°C/W
			NFA42060R42	–	–	3.20	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. For the measurement point of case temperature Tc, please refer to Figure 4.

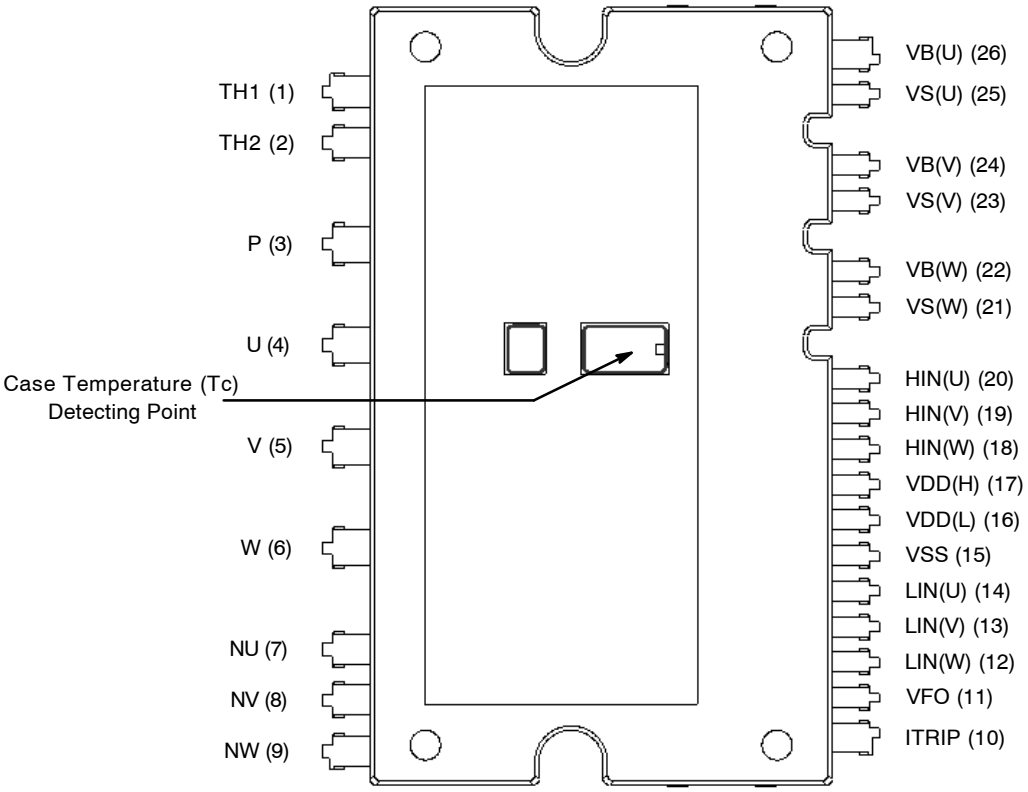


Figure 4. Case Temperature (T_C) Detecting Point

Electrical Characteristics

Table 5. ELECTRICAL CHARACTERISTICS (Tj = 25°C, unless otherwise noted)

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
INVERTER PART (Base on NFA41560R42)							
VCE(sat)		Collector−Emitter Saturation Voltage	VDD = VBS = 15 V, VIN = 5 V, Ic = 15 A, Tj = 25°C	–	1.50	2.10	V
VF		FWDi Forward Voltage	VIN = 0 V, Ic = −15 A, Tj = 25°C	–	1.75	2.35	V
HS	ton	Switching Times	VPN = 300 V, VDD(H/L) = VBS = 15 V, Ic = 15 A, Tj = 25°C, HIN(X) = 0 V ↔ 5 V, Inductive Load (Note 4)	–	0.75	–	μs
	tc(on)			–	0.12	–	μs
	toff			–	0.85	–	μs
	tc(off)			–	0.14	–	μs
	trr			–	0.13	–	μs
LS	ton		VPN = 300 V, VDD(H/L) = VBS = 15 V, Ic = 15 A, Tj = 25°C, LIN(X) = 0 V ↔ 5 V, Inductive Load (Note 4)	–	0.80	–	μs
	tc(on)			–	0.15	–	μs
	toff			–	0.90	–	μs
	tc(off)			–	0.14	–	μs
	trr			–	0.18	–	μs
Ices		Collector−Emitter Leakage Current	Vce = Vces	–	–	1	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. ton and toff include the propagation delay time of the internal drive IC. tc(on) and tc(off) are the switching time of IGBT itself under the given gate driving condition internally. For the detailed information, *please see Figure 5*.

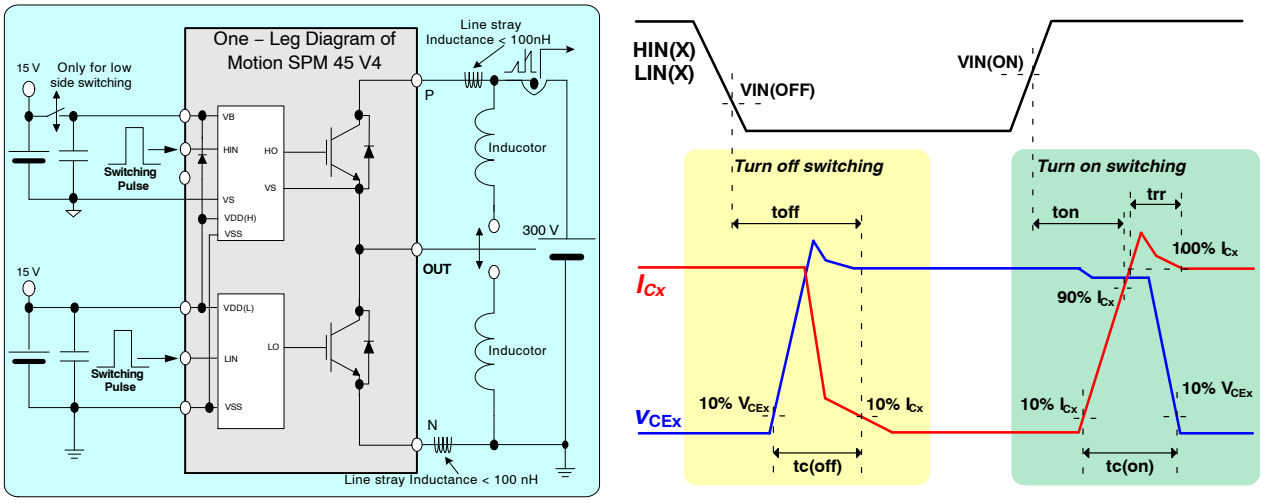


Figure 5. Switching Evaluation Circuit and Switching Time Definition

Table 6. ELECTRICAL CHARACTERISTICS (Tj = 25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BOOTSTRAP PART						
VF	Forward Voltage	If = 0.1 A, Tc = 25°C	–	2.5	–	V
trr	Reverse−Recovery Time	If = 0.1 A, dIf/dt = 50 A/μs, Tc = 25°C	–	80	–	ns
CONTROL PART						
IQDDH	Quiescent VDD Supply Current	VDD(H) = 15 V, HIN = 0 V, VDD(H) − VSS	–	–	0.10	mA
IQDDL		VDD(L) = 15 V, LIN = 0 V, VDD(L) − VSS	–	–	2.65	mA
IPDDH	Operating VDD Supply Current	VDD(H) = 15 V, fPWM = 20 kHz, Duty = 50%, Applied to One PWM Signal Input for High−Side	–	–	0.15	mA
IPDDL		VDD(L) = 15 V, fPWM = 20 kHz, Duty = 50%, Applied to One PWM Signal Input for Low−Side	–	–	4.00	mA
IQBS	Quiescent VBS Supply Current	VBS = 15 V, HIN = 0 V, Applied Btw. VB(X) − VS(X)	–	–	0.30	mA
IPBS	Operating VBS Supply Current	VDD(H) = VBS = 15 V, fPWM = 20 kHz, Duty = 50%, Applied to One PWM Signal Input for High−Side	–	–	2.00	mA
VFOH	Fault Output Voltage	VDD = 15 V, ITRIP = 0 V, VFO Circuit: 10 kΩ to 5 V Pull−up	4.5	–	–	V
VFOL		VDD = 15 V, ITRIP = 1 V, VFO Circuit: 10 kΩ to 5 V Pull−up	–	–	0.50	V
VSC(ref)	Over Current (Including Short Circuit) Trip Level	VDD = 15 V, ITRIP − VSS (Note 5)	0.45	0.50	0.55	V
UVDDD	Supply Circuit for VDD, Under−Voltage Protection	Detection Level	10.5	–	13.0	V
UVDDR		Reset Level	11.0	–	13.5	V
UVBSD	Supply Circuit for VBS, Under−Voltage Protection	Detection Level	10.0	–	12.5	V
UVBSR		Reset Level	10.5	–	13.0	V
tFOD	Fault−Output Pulse Width		30	–	–	μs
VIN(ON)	ON Threshold Voltage	Applied between HIN(X), LIN(X) − VSS	–	–	2.6	V
VIN(OFF)	OFF Threshold Voltage		0.8	–	–	V
RTH	Resistance of Thermistor	@ TTH = 25°C (Note 6)	–	47	–	kΩ
		@ TTH = 100°C	–	2.9	–	kΩ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Short−circuit current protection is functioning only at the low−sides.
6. TTH is the temperature of thermistor itself. To know case temperature (Tc), please make the experiment considering your application.

Recommended Operating Conditions

Table 7. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VPN	Supply Voltage	Applied between P − NU, NV, NW	−	300	400	V
VDD	Control Supply Voltage	Applied between VDD(H/L) − VSS	13.5	15.0	16.5	V
VBS	High−Side Bias Voltage	Applied between VB(X) − VS(X)	13.0	15.0	18.5	V
dVDD/dt, dVBS/dt	Control Supply Variation		−1	−	1	V/μs
tdead	Blanking Time for Preventing Arm−Short	For each input signal	1.0	−	−	μs
fPWM	PWM Input Signal	−40°C < Tc < 125°C, −40°C < Tj < 150°C	−	−	20	kHz
VSEN	Voltage for Current Sensing	Applied between NU, NV, NW − VSS (Including Surge−Voltage)	−4	−	4	V
PWIN(ON)	Minimum Input Pulse Width	VDD = VBS = 15 V, Ic ≤ 30 A, Wiring Inductance between NU, NV, NW and DC Link N < 10 nH (Note 7)	1.2	−	−	μs
PWIN(OFF)			1.2	−	−	
Tj	Junction Temperature		−40	−	150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

7. This product might not make response if input pulse width is less than the recommended value.

Mechanical Characteristics

MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Conditions		Min	Typ	Max	Unit
Device Flatness	*See Figure 6*		–	–	+120	μm
Mounting Torque	Mounting Screw: M3 *See Figure 7*	Recommended 0.7 N · m	0.6	0.7	0.8	N · m
		Recommended 7.1 kg · cm	6.2	7.1	8.1	kg · cm
Weight			–	11.0	–	g

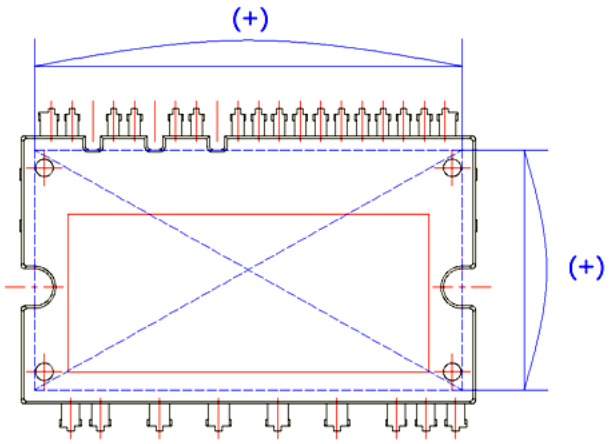
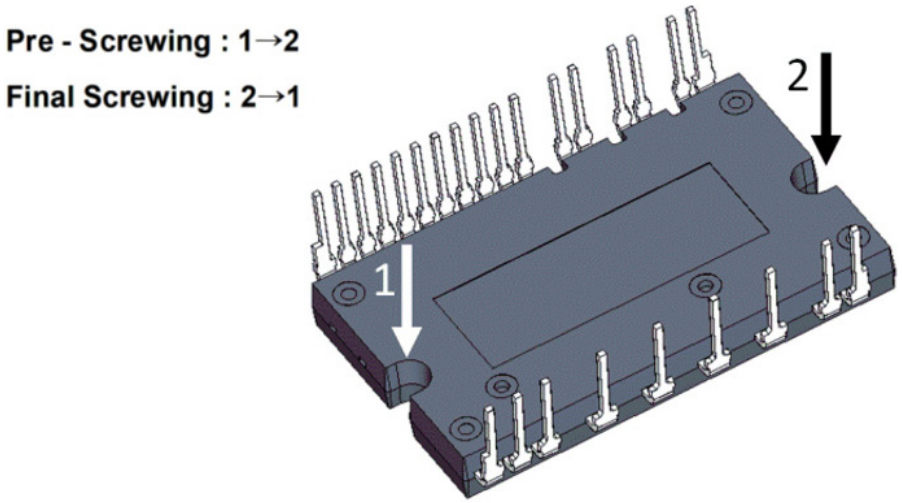


Figure 6. Flatness Measurement Position



NOTES:

8. Do not make over torque when mounting screws. Much mounting torque may cause ceramic cracks, as well as bolts and Al heat−sink destruction.
9. Avoid one−sided tightening stress. Figure 7 shows the recommended torque order for mounting screws. Uneven mounting can cause the ceramic substrate of package to be damaged. The pre−screwing torque is set to 20~30% of maximum torque rating.

Figure 7. Mounting Screws Torque Order

PACKAGE

Isolation Distance and Package Structure

Since heat dissipation is an important factor that limits the power module's current capability, the heat dissipation characteristics are critical in determining the Motion SPM 45 V4 series performance. A trade−off exists among heat dissipation characteristics, package size, and isolation characteristics. The key to a good package technology lies in the accomplishment of optimization package size while maintaining outstanding heat dissipation characteristics without compromising the isolation rating.

In the Motion SPM 45 V4 series, technology was developed in which bare ceramic with good heat dissipation characteristic is attached directly to the lead frame. This technology made it possible to achieve improved reliability and heat dissipation, while maintaining cost effectiveness. Distances for an isolation are shown in Figure 8. And Figure 9 shows the cross−sections of the Motion SPM 45 V4 series package.

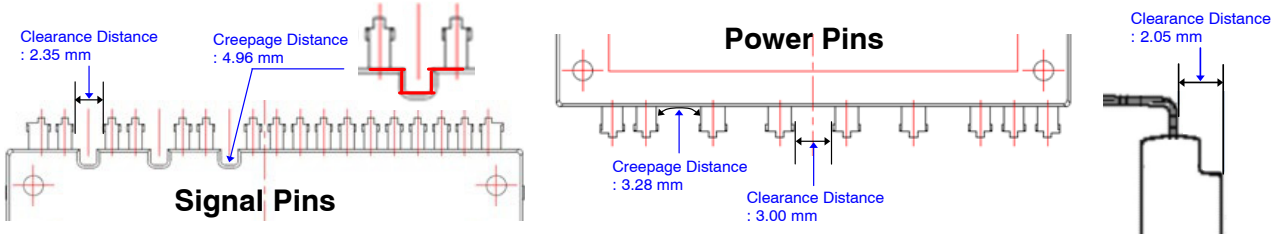


Figure 8. Isolation Distance for Signal Pins, Power Pins and Pins to Heat Sink

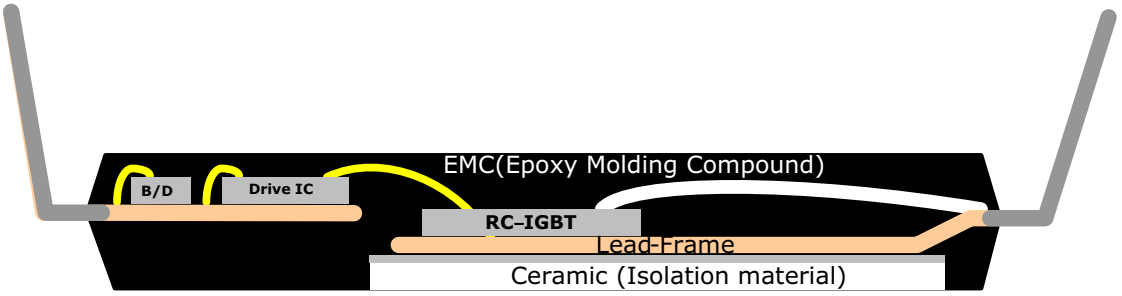


Figure 9. Package Structure and Cross Section for SPM 45 Version 4

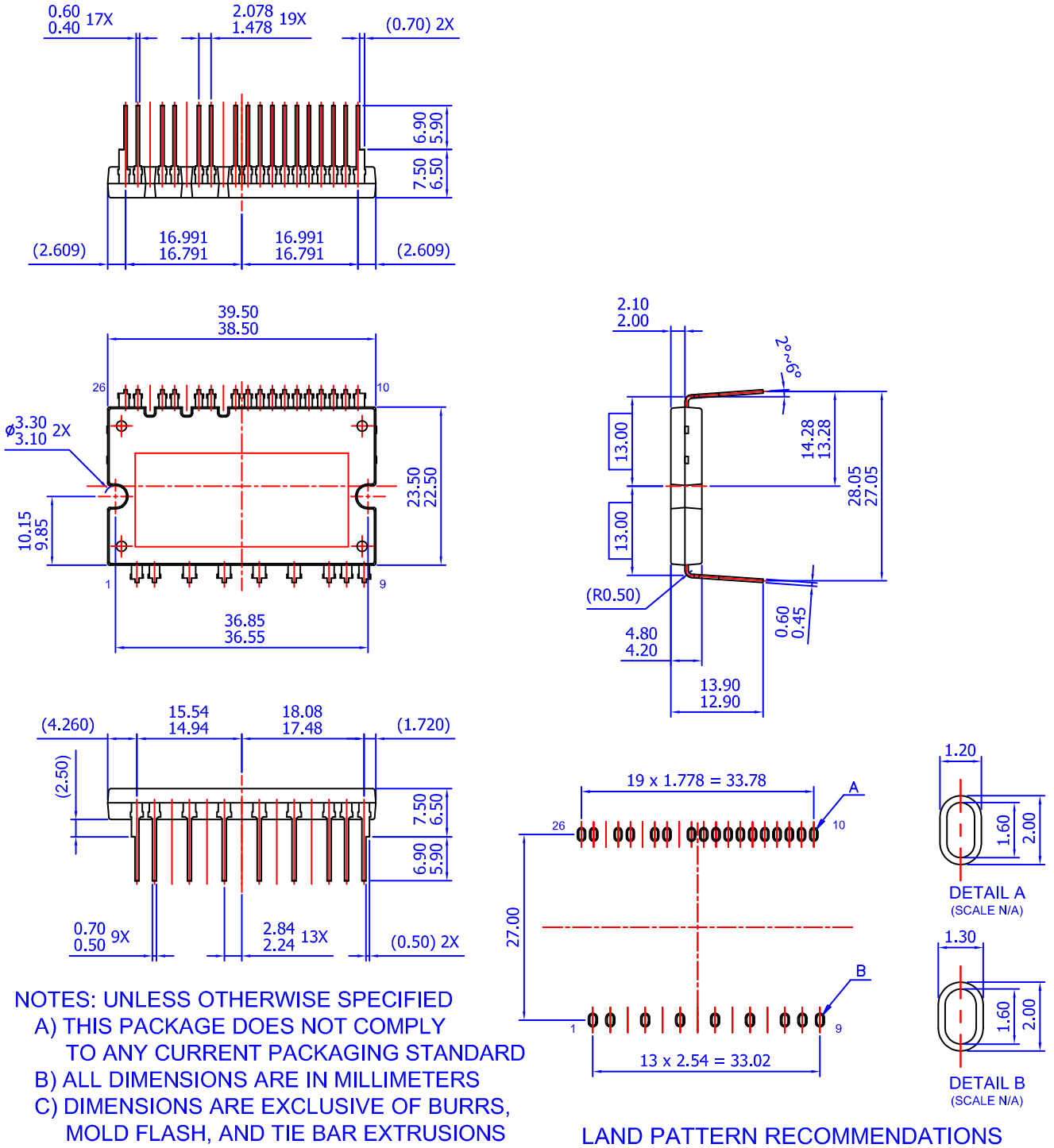
Ordering Information

Table 8. ORDERING INFORMATION

Device	Device Marking	Package	Shipping
NFA41560R42	NFA41560R42	SPMAA−C26 / 26LD, PDD STD CERAMIC TYPE, LONG LEAD DUAL FORM TYPE (Pb−Free)	12 Units / Rail
NFA42060R42	NFA42060R42		

Package Outline

SPMAA−C26 / 26LD, PDD STD CERAMIC TYPE, LONG LEAD DUAL FORM TYPE
CASE MODFC
ISSUE O



NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE DOES NOT COMPLY TO ANY CURRENT PACKAGING STANDARD
B) ALL DIMENSIONS ARE IN MILLIMETERS
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D) ( ) IS REFERENCE

LAND PATTERN RECOMMENDATIONS

OPERATION SEQUENCE FOR PROTECTIONS

Over Current Protection (OCP)

Motion SPM 45 V4 series use an external shunt resistor for the over−current detection, as shown in Figure 10. The LVIC has built−in over current protection that senses the voltage to the ITRIP pin and, if this voltage exceeds the VSC(ref) (the threshold voltage trip level of protection function) specified in the device datasheets (VSC(ref), Typ. is 0.5 V), a fault signal is asserted and all three lower arm IGBTs are turned off. Short circuit is included to over current situation. Typically, the maximum short−circuit current magnitude is gate voltage dependent. A higher gate voltage (VDD & VBS) is resulted in a larger short circuit current. To avoid this potential problem, the maximum short−circuit trip level is generally set to below 1.5 times the nominal rated collector current. The over−current protection−timing chart is shown in Figure 11.

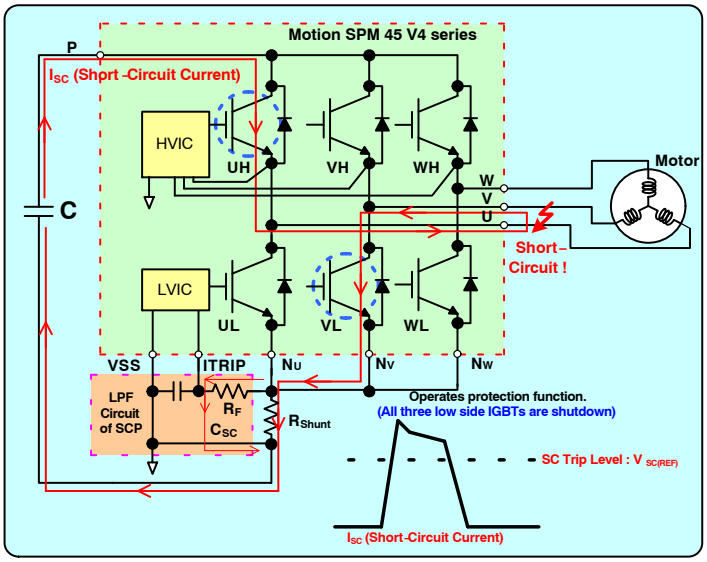
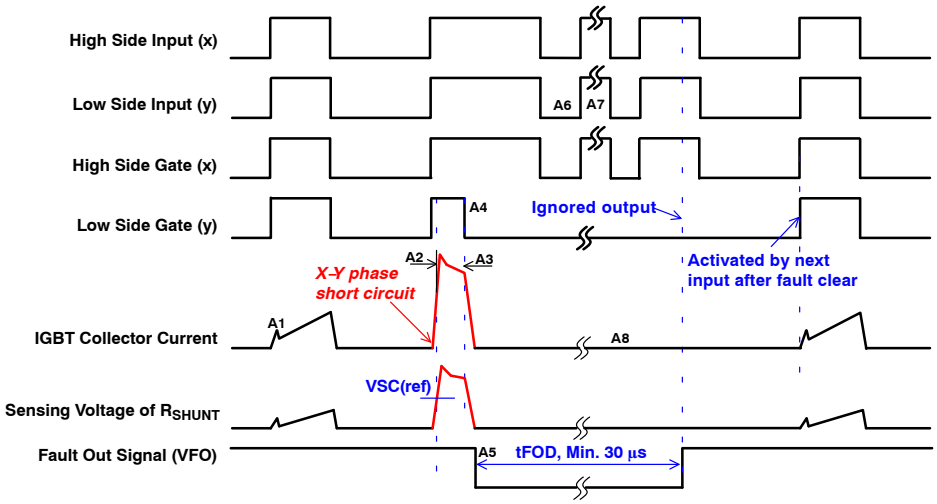


Figure 10. Operation of Short Circuit Protection

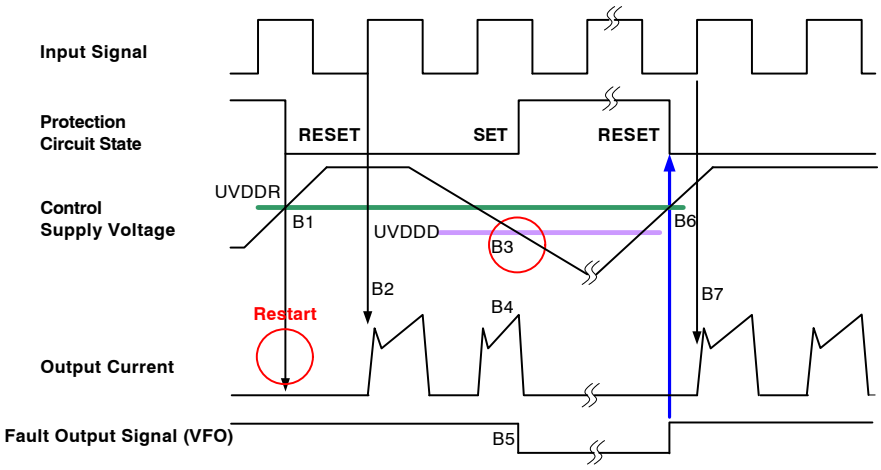


NOTES:
10. A1−Normal operation: IGBTs on and carrying current.
11. A2−Over−current detection (OC trigger).
12. A3−Hard IGBTs gate interrupt.
13. A4−Low side IGBTs turn off.
14. A5−Fault output timer operation start with internal delay, tFOD = Min. 30 µs.
15. A6−Input “L”: Low side IGBTs OFF state.
16. A7−Input “H”: Low side IGBTs input ON state, but during the active period of fault output the IGBT doesn’t turn ON.
17. A8−Low side IGBTs keeps OFF state.

Figure 11. Timing Chart of Over Current Protection

Under−Voltage Lockout Protection (UVLO)

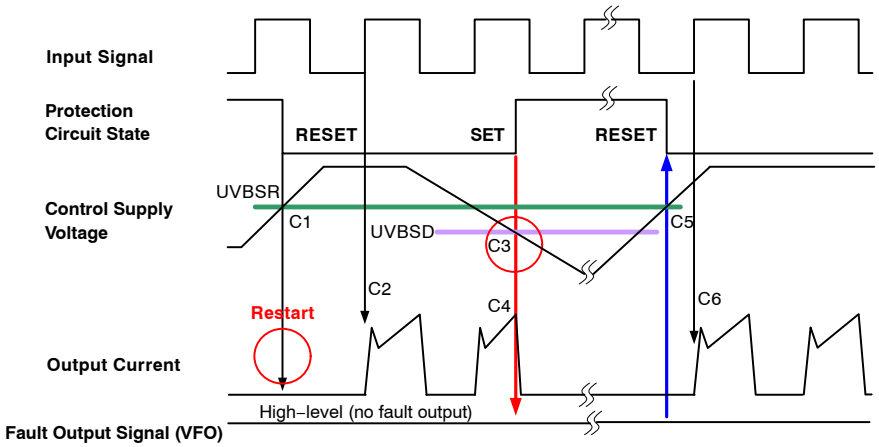
The low side gate drive IC has an under−voltage lockout protection (UVLO) function to protect the low−side IGBTs from operation with insufficient gate driving voltage. A timing chart for this protection is shown in Figure 12.



NOTES:
18. B1−control supply voltage rise: after the voltage rises UVDDR, the circuits start to operate when the next input is applied.
19. B2−normal operation: IGBT ON and carrying current.
20. B3−under−voltage detection (UVDDD).
21. B4−IGBT OFF in spite of control input is alive.
22. B5−fault output signal starts.
23. B6−under−voltage reset (UVDDR).
24. B7−normal operation: IGBT ON and carrying current.

Figure 12. Timing Chart of Low Side Under−Voltage Protection Function

The high side gate drive IC has an under−voltage lockout function to protect the high−side IGBT from insufficient gate driving voltage. A timing chart for this protection is shown in Figure 13. A fault−out alarm is not given for low at high side bias conditions.



NOTES:
25. C1−control supply voltage rises: after the voltage reaches UVBSR, the circuit starts when the next input is applied.
26. C2−normal operation: IGBT ON and carrying current.
27. C3−under−voltage detection (UVBSD).
28. C4−IGBT OFF in spite of control input is alive, but there is no fault output signal.
29. C5−under−voltage reset (UVBSR).
30. C6−normal operation: IGBT ON and carrying current.

Figure 13. Timing Chart of High Side Under−Voltage Protection Function

KEY PARAMETER DESIGN GUIDANCE

For stable operation, there are recommended parameters for passive components, bias conditions and considering operating characteristics of Motion SPM 45 V4 series. This section focuses on the key parameter design guidance.

Shunt Resistor Selection Guide

The external RC time constant from the N−terminal shunt resistor to ITRIP must be lower than 2 μs when overload condition is detected for a stable shutdown. Figure 14 and Figure 15 show an example circuit of the SC protection using one shunt resistor and three shunt resistors. The line current on the N side DC−ink is detected and the protective operation signal is passed through the RC filter. If the current exceeds the SC reference level, all the gates of the N−side three−phase IGBTs are switched to the off state and the VFO fault signal is transmitted to MCU. Since SC protection is non−repetitive, IGBT operation should be immediately halted when the VFO fault signal is given.

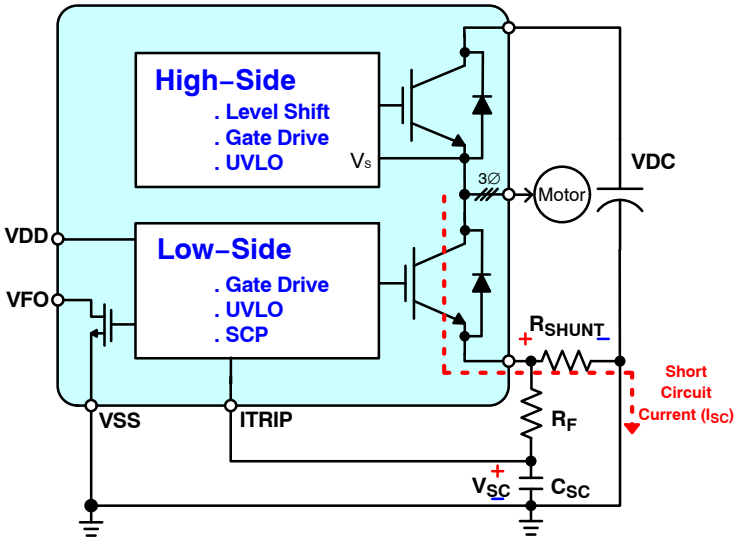


Figure 14. Recommended Circuitry of One Shunt Resistors Type for Over Current Protection

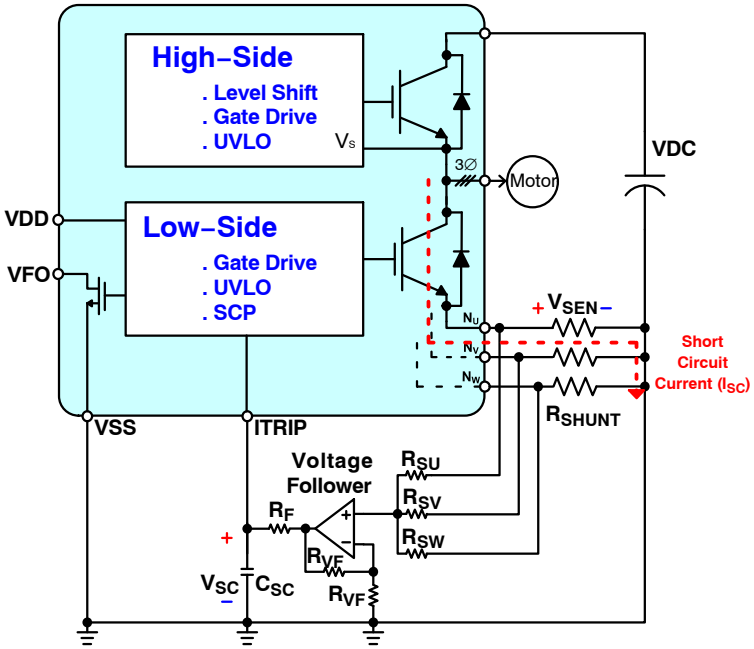


Figure 15. Recommended Circuitry of Three Shunt Resistors Type for Over Current Protection

Table 9. DETECTED OVER CURRENT PROTECTION LEVEL

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VSC(ref)	Over current (including short circuit) Trip Level	Tj = 25°C, VDD = 15 V, ITRIP − VSS	0.45	0.50	0.55	V

The shunt resistance is calculated by the following equation.

- **Maximum Current Trip Level:**
  - Depends on user selection

  $I_{SC(max)} = 1.5 \times I_{C(max)}$

- **SC trip reference voltage:**
  - Depends on datasheet

  $VSC(ref) = min.\ 0.45\ V,\ typ.\ 0.5\ V,\ max.\ 0.55\ V$

- **Shunt resistance:**

  $I_{SC(max)} = VSC(max) / R_{SHUNT(min)} \rightarrow R_{SHUNT(min)} = VSC(max) / I_{SC(max)}$

- **If the deviation of the shunt resistor is limited below ±5%:**

  $R_{SHUNT(typ)} = R_{SHUNT(min)} / 0.95,$
  $R_{SHUNT(max)} = R_{SHUNT(typ)} \times 1.05$

- **Actual SC trip current level becomes:**

  $I_{SC(typ)} = VSC(typ) / R_{SHUNT(typ)},\ I_{SC(min)} = VSC(min) / R_{SHUNT(max)}$

- **Inverter output power:**

$$P_{OUT} = \frac{\sqrt{3}}{\sqrt{2}} \times MI \times V_{DC\_Link} \times I_{RMS} \times PF$$

where

MI	*is Modulation Index;*
V_{DC_Link}	*is DC link voltage;*
I_{RMS}	*is Maximum load current of inverter; and*
PF	*is Power Factor*

- **Average DC current:**

$$I_{DC\_AVG} = (P_{out} / Eff) / V_{DC\_Link}$$

where

Eff	*is Inverter efficiency*

- **The power rating of shunt resistor is calculated by the following equation:**

$$P_{SHUNT} = (I^2_{DC\_AVG} \times R_{SHUNT} \times Margin) / Derating\ Ratio$$

where

R_{SHUNT}	*is Shunt resistor typical value at Tc = 25 ℃*
Derating Ratio	*is Derating ratio of shunt resistor at* T_{SHUNT} *= 100 ℃ (From datasheet of shunt resistor);*
And, Margin	*is Safety margin (Determined by user)*

- **Shunt Resistor Calculation Examples:**
  - Calculation Conditions:
  - DUT: NFA41560R42
  - Tolerance of shunt resistor: ±5%
  - SC Trip Reference Voltage:
  - VSC(min) = 0.45 V, VSC(typ) = 0.50 V, VSC(max) = 0.55 V
  - Max. Load Current of Inverter (I_{RMS}): 7.5 A_{rms}
  - Max. Peak Load Current of Inverter ($I_{C(max)}$): 15 A
  - Modulation Index (MI): 0.9
  - DC Link Voltage (V_{DC_Link}): 300 V
  - Power Factor (PF): 0.8
  - Inverter Efficiency (Eff): 0.95
  - Shunt Resistor Value at Tc = 25°C (R_{SHUNT}): 30 mΩ
  - Derating Ration of Shunt Resistor at T_{SHUNT} = 100°C: 70% (Refer to Figure 14.)
  - Safety Margin: 20%

- **Calculation Results:**
  - $I_{SC(max)}$:
    $1.5 \times I_{C(max)} = 1.5 \times 15\ A = 22.5\ A$
  - $R_{SHUNT(min)}$:
    $VSC(max) / I_{SC(max)} = 0.55\ V / 22.5\ A = 24.4\ m\Omega$
  - $R_{SHUNT(typ)}$:
    $R_{SHUNT(min)} / 0.95 = 24.4\ m\Omega / 0.95 = 25.7\ m\Omega$
  - $R_{SHUNT(max)}$:
    $R_{SHUNT(typ)} \times 1.05 = 25.7\ m\Omega \times 1.05 = 27.0\ m\Omega$
  - $I_{SC(min)}$:
    $VSC(min) / R_{SHUNT(max)} = 0.45\ V / 27.0\ m\Omega = 16.7\ A$
  - $I_{SC(typ)}$:
    $VSC(typ) / R_{SHUNT(typ)} = 0.5\ V / 25.7\ m\Omega = 19.5\ A$
  - $P_{OUT} = \frac{\sqrt{3}}{\sqrt{2}} \times MI \times V_{DC\_Link} \times I_{RMS} \times PF =$
    $\frac{\sqrt{3}}{\sqrt{2}} \times 0.9 \times 300 \times 7.5 \times 0.8 = 1984\ W$
  - $I_{DC\_AVG} = (P_{OUT}/Eff) / V_{DC\_Link} = 6.96\ A$
  - $P_{SHUNT} = (I^2_{DC\_AVG} \times R_{SHUNT} \times Margin) / Derating\ Ratio = (6.96^2 \times 0.025 \times 1.2) / 0.7 = 2.08\ W$ (Therefore, the proper power rating of shunt resistor is over 2.5 W)

Table 10. OVER−CURRENT (OC) PROTECTION TRIP LEVEL

Device	RSHUNT	Over−Current Trip Level	Remark
FNA41560R42	21.3 mΩ	22.5 A	Typical Value
FNA42060R42	16.0 mΩ	30.0 A	

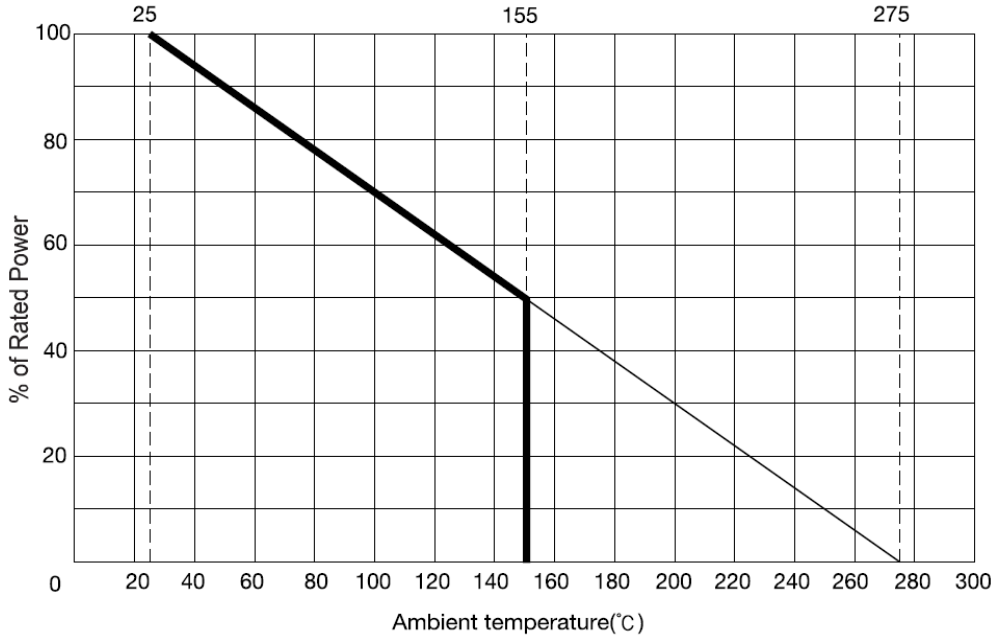
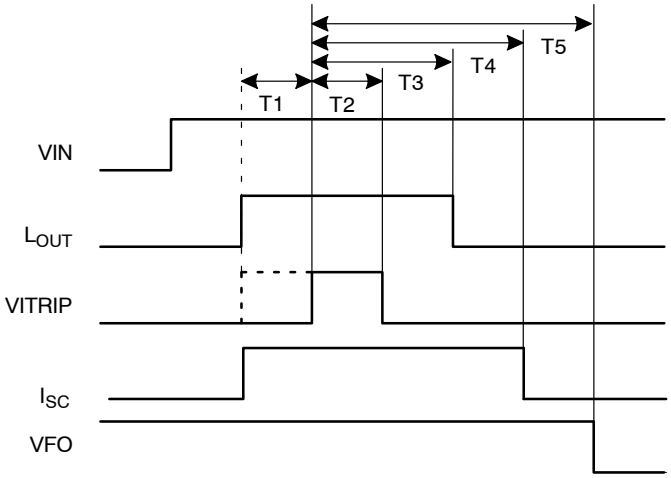


Figure 16. De−rating Curve Example of Shunt Resistor (from RARA Elec.)

Time Constant of Internal Delay

An RC filter prevents unexpected malfunction by noise−related signal like reverse recovery current of FWDi. The RC time constant is determined by the applied noise time and the Short−Circuit Current Withstanding Time (SCWT) of Motion SPM 45 V4 series. When the R_{SHUNT} voltage exceeds the OCP level, this is applied to the ITRIP pin via the RC filter. The RC filter delay (T1) is the time required for the ITRIP pin voltage to rise to the referenced OCP level. The gate drive IC has an internal filter time (logic filter time for noise elimination: T2). Consider this filter time when designing the RC filter of VITRIP.



NOTES:
31. VIN: Voltage of input signal.
32. L_{OUT}: V_{GE} of low−side IGBT.
33. VITRIP: Voltage of ITRIP pin.
34. I_{SC}: Over current or short−circuit current.
35. VFO: Voltage of VFO pin.
36. T1: Filtering time of RC filter of VITRIP.
37. T2: Filtering time of ITRIP. If VITRIP width is less than T2, SCP does not operate.
38. T3: Delay from ITRIP triggering to gate−voltage down.
39. T4: Delay from ITRIP triggering to IGBT shutdown.
40. T5: Delay from ITRIP triggering to fault−out signal.

Figure 17. Timing Chart of High Side Under−Voltage Protection Function

Table 11. TIME TABLE ON SHORT−CIRCUIT CONDITIONS: VITRIP to L_{OUT}, I_{SC} and VFO

Device	Typ. Time at Tj = 25°C	Remark
FNA41560R42	T2 = 0.4 μs	Max. Time at Tj = 25°C, Considering ±20% Distribution, T3 and T4
	T3 = 0.6 μs	
	T4 = 1.3 μs	
	T5 = 1.5 μs	

41. To guarantee safe short−circuit protection under all operating conditions, ITRIP should be triggered within 0.4 μs after short−circuit occurs. (Recommendation: SCWT < 2.0 μs, Conditions: VDC = 400 V, VDD = 16.5 V, Tj = 150°C).
42. It is recommended that delay from short−circuit to ITRIP triggering should be minimized

Fault Output Function

VFO terminal is an open−drain type from MOSFET, this pin should be pulled up with a resistor to control internal MOSFET. The resistor should be calculated from the above specifications.

Table 12. FAULT OUTPUT MAXIMUM RATINGS

Item	Symbol	Conditions	Rating	Unit
Fault Output Voltage	VFO	Applied between VFO − VSS	−0.3 ~ VDD + 0.3	V
Fault Output Current	I_{FO}	Sink Current at VFO Pin	1.0	mA

Table 13. ELECTRIC CHARACTERISTICS

Item	Symbol	Conditions	Min	Max	Unit
Fault Output Voltage	VFOH	ITRIP = 0 V, VFO Circuit: 4.7 kΩ to 5 V Pull−up	4.5	−	V
	VFOL	ITRIP = 1 V, VFO Circuit: 4.7 kΩ to 5 V Pull−up	−	0.5	

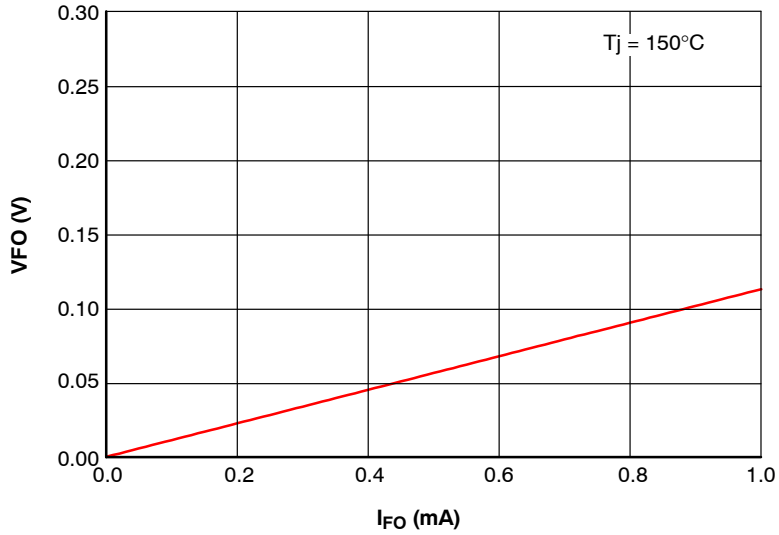


Figure 18. Voltage−Current Characteristics of VFO Terminal

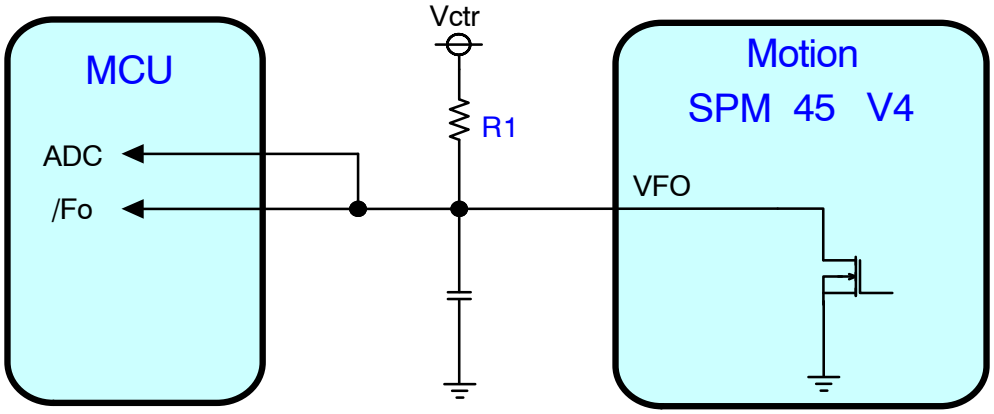


Figure 19. Propose Circuit for Fault Output Function

Circuit of Input Signal (HIN(X), LIN(X))

Figure 20 shows the I/O interface circuit between the MCU and Motion SPM 45 V4 series. Because the input logic of the Motion SPM 45 V4 series is active high and there are built−in pull−down resistors, external pull−down resistors are not needed

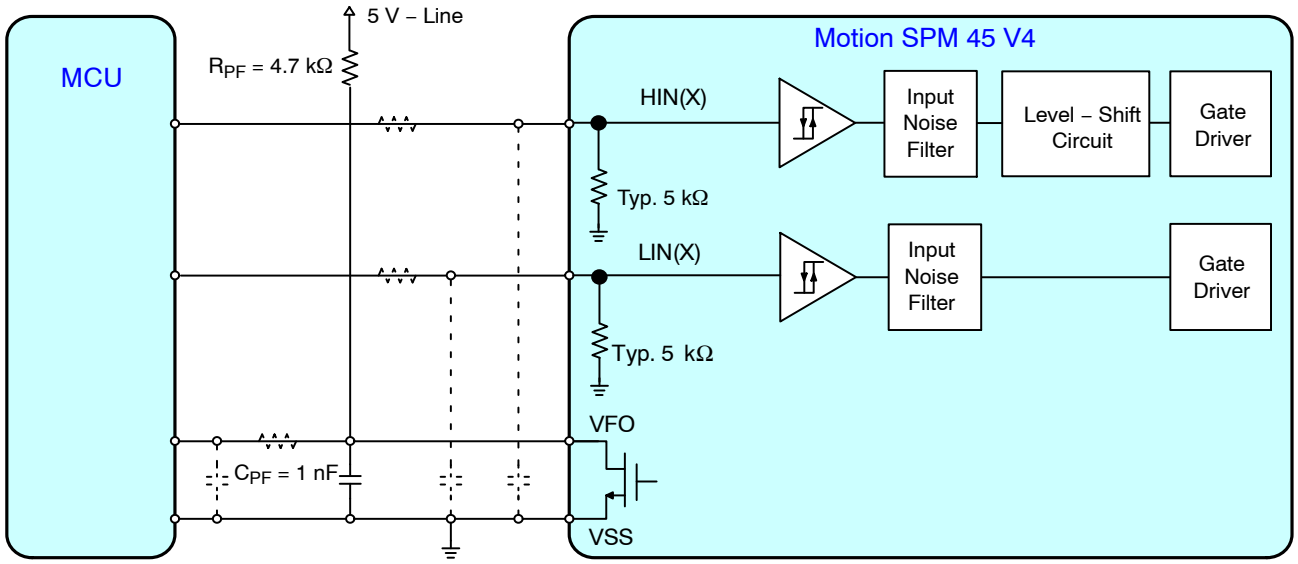


Figure 20. Recommended MCU I/O Interface Circuit

Since the fault output is open drain, its rating is VDD +0.3 V, 15 V supply interface is possible. However, it is recommended that the fault output be configured with the 5 V logic supplies, which is the same as the input signals. It is also recommended that the de−coupling capacitors be placed at both the MCU and Motion SPM 45. To avoid unexpected operation by fault signal, it is recommended to connect bypass capacitor to ends of the signal line for VFO pin and MCU as close as possible to each device. The RC coupling at each input (parts shown dotted in Figure 20) can be changed depending on the PWM control scheme used in the application and the wiring impedance of the PCB layout. The input signal section of the Motion SPM 45 V4 series integrate 5 kΩ (typical) pull−down resistors. Therefore, when using an external filtering resistor between the MCU output and the Motion SPM 45 V4 series input, attention should be given to the signal voltage drop at the Motion SPM 45 V4 series input terminals to satisfy the turn−on threshold voltage requirement. For instance, R = 100 Ω and C = 1 nF can be used for the parts shown dotted in Figure 20.

Table 14. MAXIMUM RATINGS OF INPUT AND VF PINS

Item	Symbol	Conditions	Rating	Unit
Input Signal Voltage	VIN	Applied between HIN(X) − VSS	−0.3 ~ VDD + 0.3	V
		Applied between LIN(X) − VSS	−0.3 ~ VDD + 0.3	

Table 15. INPUT THRESHOLD VOLTAGE RATINGS (VDD = 15 V, Tj = 25°C)

Item	Symbol	Conditions	Min	Max	Unit
Turn−ON threshold Voltage	VIN(ON)	HIN(X) − VSS	−	2.6	V
Turn−OFF threshold Voltage	VIN(OFF)	LIN(X) − VSS	0.8	−	V

Bootstrap Circuit Design

Operation of Bootstrap Circuit

The VBS voltage, which is the voltage difference between VB (U, V, W) and VS (U, V, W), provides the supply to the HVIC within the Motion SPM 45 V4 series. This supply must be in the range of 13.0 V~18.5 V to ensure that the HVIC can fully drive the high−side IGBT. The under−voltage lockout protection for VBS ensures that the HVIC does not drive the high−side IGBT if the VBS voltage drops below a specific voltage. This function prevents the IGBT from operating in a high−dissipation mode.

There are a number of ways in which the VBS floating supply can be generated. One of them is the bootstrap method described here (refer to Figure 21). This method has the advantage of being simple and inexpensive. However, the duty cycle and on−time are limited by the requirement to refresh the charge in the bootstrap capacitor. Motion SPM 45 V4 series provide integrated bootstrap circuitry in driver. The bootstrap supply is formed by a combination of bootstrap diode, resistor, the current flow path of the bootstrap circuit is show in Figure 21. When VS is pulled down to ground (low−side IGBT turn−on or low−side FWDi freewheeling), the bootstrap capacitor (C_{BOOT}) is charged through the integrated bootstrap diode from the VDD supply.

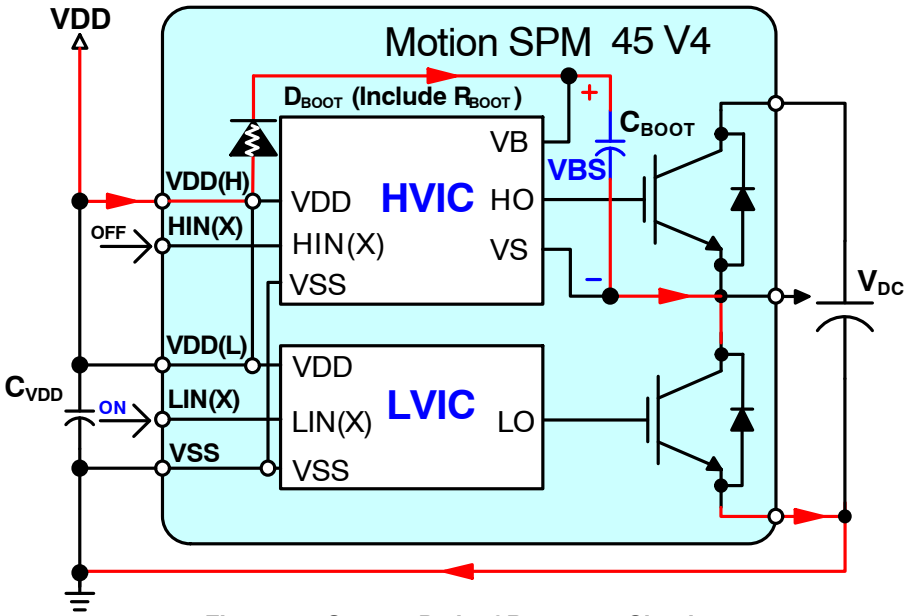


Figure 21. Current Path of Bootstrap Circuit

Selection of Bootstrap Capacitor Considering Initial Charging

Adequate on−time duration of the low−side IGBT to fully charge the bootstrap capacitor is required for initial bootstrap charging. The initial charging time (t_{charge}) can be calculated from the following equation:

$$t_{charge} = C_{BOOT} \times R_{BOOT} \times \frac{1}{\delta} \times \ln \frac{VDD}{VDD - VBS_{(Min.)} - VF - V_{LS}} \quad \text{(eq. 1)}$$

where

VF is forward voltage drop across the bootstrap diode;

$VBS_{(Min.)}$ is minimum value of the bootstrap capacitor;

V_{LS} is voltage drop across the low−side IGBT or load; and

δ is duty ratio PWM.

Enough on−time duration of the low−side IGBT to fully charge the bootstrap capacitor is initially required before normal operation of PWM starts for the Motion SPM 45 V4 series. When the bootstrap capacitor is charged initially; VDD drop voltage is generated based on initial charging method, VDD line SMPS output current, VDD source capacitance, and bootstrap capacitance. If VDD drop voltage reaches UVDDD level, the low side is shut down and a fault signal is activated.

To avoid this malfunction, related parameter and initial charging method should be considered. To reduce VDD voltage drop at initial charging, a large VDD source capacitor and selection of optimized low−side turn−on method are recommended. Adequate on−time duration of the low−side IGBT to fully charge the bootstrap capacitor is initially required before normal operation of PWM starts. Figure 22 shows an example of initial bootstrap charging

sequence. Once VDD establishes, VBS needs to be charged by turning on the low−side IGBTs. PWM signals are typically generated by an interrupt triggered by a timer with a fixed interval, based on the switching carrier frequency. Therefore, it is desired to maintain this structure without creating complementary high−side PWM signals. The capacitance of VDD should be sufficient to supply necessary charge to VBS capacitance in all three phases. If a normal PWM operation starts before VBS reaches UVLO reset level, the high−side IGBTs cannot switch without creating a fault signal. It may lead to a failure of motor start in some applications. If three phases are charged synchronously, initial charging current through a single shunt resistor may exceed the over−current protection level. Therefore, initial charging time for bootstrap capacitors need to be separated, as shown in Figure 23 if amount of initial current during short time should be minimized. The effect of the bootstrap capacitance factor and charging method (low−side IGBT driving method) is shown in Figure 24.

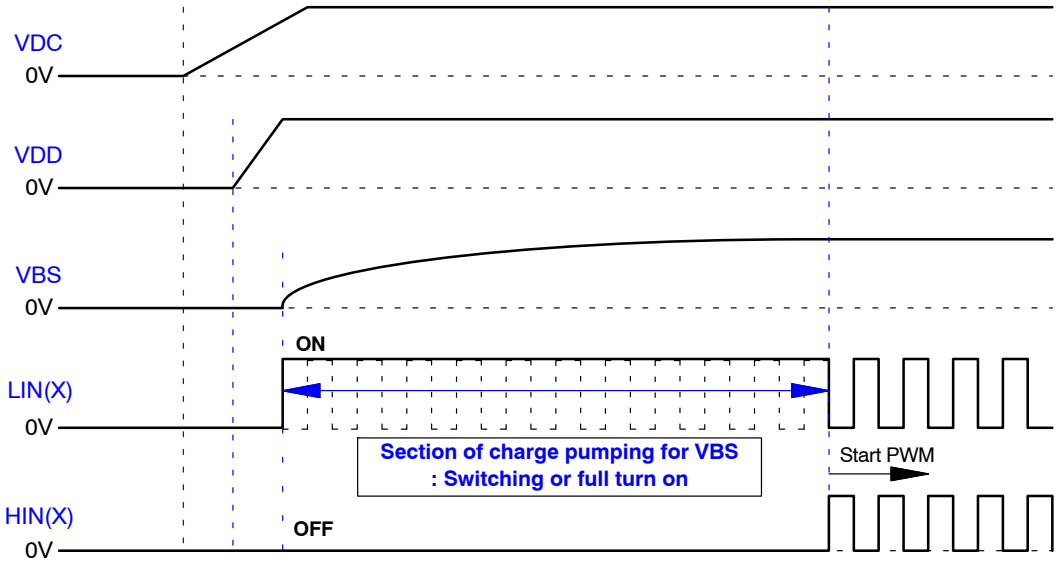


Figure 22. Timing Chart of Initial Bootstrap Charging

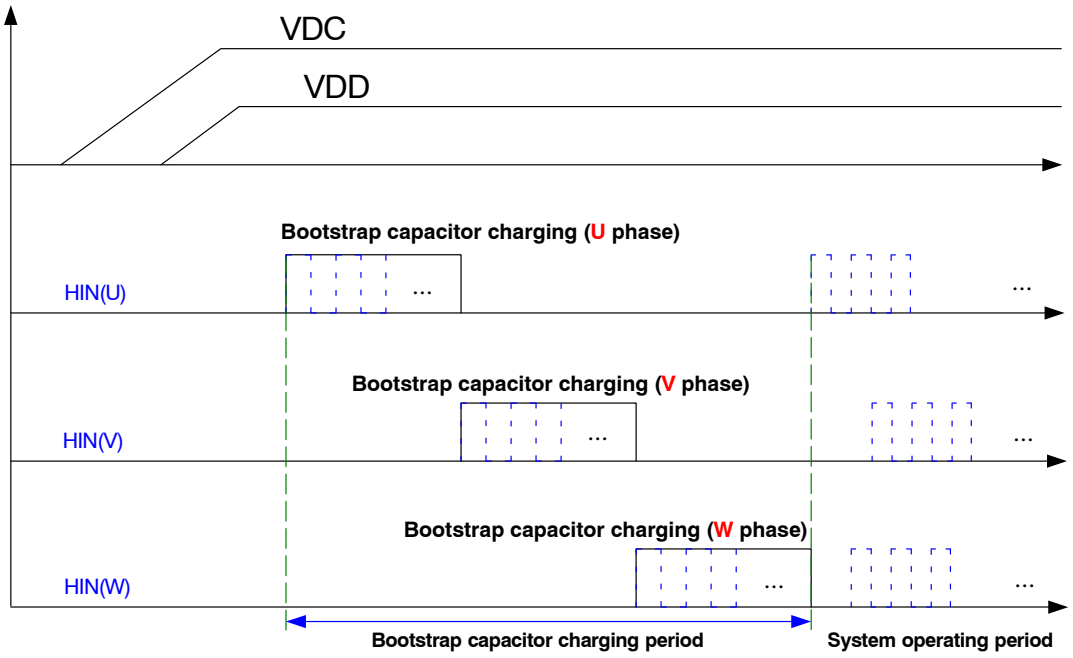


Figure 23. Recommended Initial Bootstrap Capacitors Charging Sequence

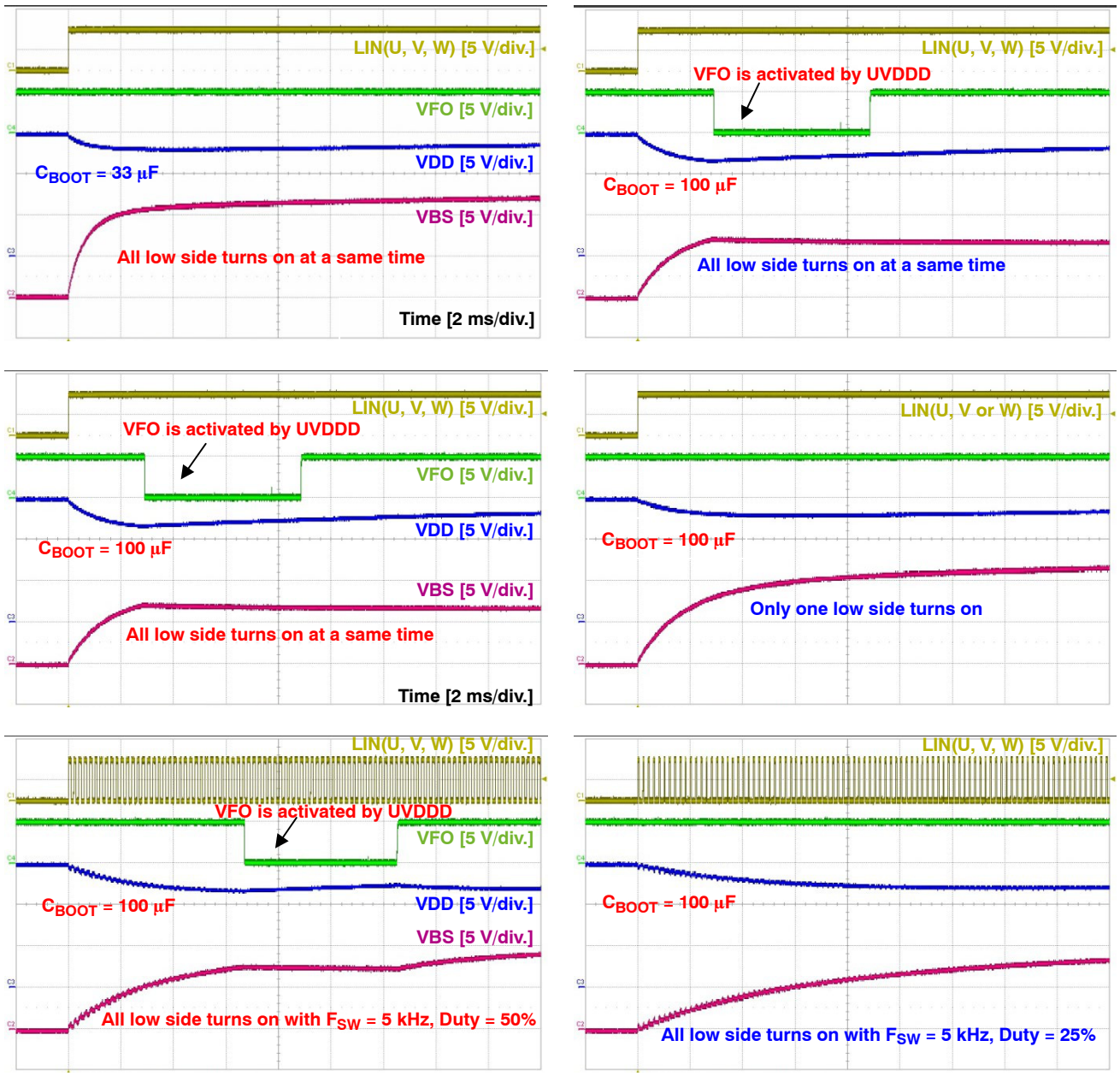


Figure 24. Initial Charging According to Bootstrap Capacitance and Charging Method (Ref. Conditions: VDD = 15 V / 300 mA, VDD Capacitor = 200 µF, C_{BOOT} = 100 µF, 20 Ω)

Selection of Bootstrap Capacitor Considering Operation

The bootstrap capacitance can be calculated by:

$$C_{BOOT} = \frac{I_{Leak} \times \Delta t}{\Delta VBS} \qquad \text{(eq. 2)}$$

where

Δt is maximum on pulse width of high−side IGBT;

ΔVBS is the allowable discharge voltage of the C_{BOOT} (voltage ripple); and

I_{Leak} is maximum discharge current of the C_{BOOT}.

Mainly via the following mechanisms:

- Gate charge for turning the high−side IGBT on.
- Quiescent current to the high−side circuit in the HVIC.
- Level−shift charge required by level−shifters in HVIC.
- Leakage current in the bootstrap diode.
- C_{BOOT} capacitor leakage current (ignored for non−electrolytic capacitors).
- Bootstrap diode reverse recovery charge.

Practically, 2 mA of I_{Leak} is recommended for Motion SPM 45 V4 series. By taking consideration of dispersion and reliability, the capacitance is generally selected to be 2~3 times of the calculated one. The C_{BOOT} is only charged when the high−side IGBT is off and the VS voltage is pulled down to ground. Therefore, the on−time of the low−side IGBT must be sufficient to ensure that the charge drawn from the C_{BOOT} capacitor can be fully replenished. Hence, there is an inherent minimum on−time for the low−side IGBT (or off−time of the high−side IGBT).

Calculation Examples of Bootstrap Capacitance

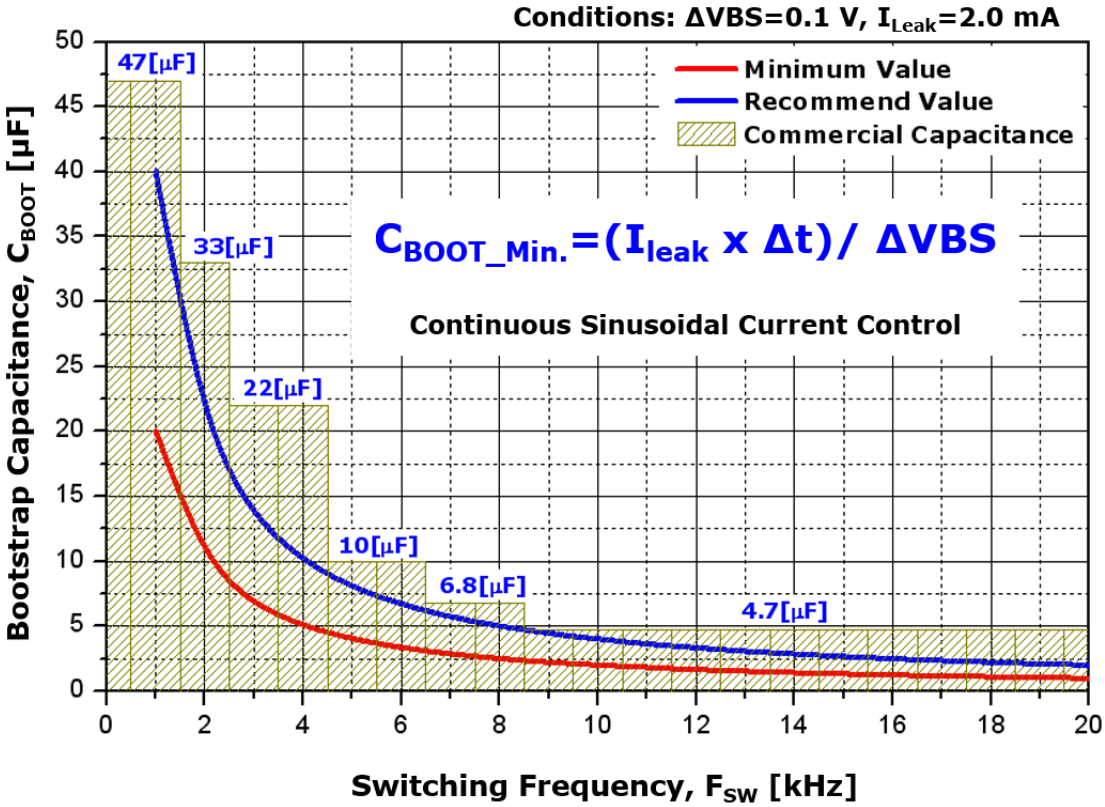
Calculation examples of bootstrap capacitance are based on recommended I_{Leak} and recommended ΔVBS.

- I_{Leak} = 2.0 mA (recommendation value)
- ΔVBS = 0.1 V (recommendation value)
- Δt = 0.2 ms (depends on user system)

$$- \; C_{BOOT\_Min.} = \frac{I_{Leak} \times \Delta t}{\Delta VBS} = \frac{2\,mA \times 0.2\,ms}{0.1\,V} = 4.0 \times 10^{-6}$$

where

→ More than 2 ~ 3 times → 8 μF.



NOTE:

43. This capacitance value can be changed according to the switching frequency, capacitor used, and recommended VBS voltage of 13.0~18.5 V (from datasheet). The above result is just a calculation example. This value can be changed according to the actual control method and lifetime of component.

Figure 25. Capacitance of Bootstrap Capacitor on Variation of Switching Frequency

Built−in Bootstrap Circuit

When the low−side IGBT or diode conducts, the bootstrap diode (D_{BOOT}) supports the entire bus voltage. Hence, a diode with withstand voltage of more than 600 V is recommended. It is important that this diode has a fast recovery (recovery time < 100 ns) characteristic to minimize the amount of charge fed back from the bootstrap capacitor into the VDD supply. The bootstrap resistor (R_{BOOT}) is to slow down the dVBS/dt and limit initial charging current (I_{charge}) of bootstrap capacitor.

Normally, a bootstrap circuit consists of bootstrap diode (D_{BOOT}), bootstrap resistor (R_{BOOT}), and bootstrap capacitor (C_{BOOT}). As shown in Figure 26, the built−in bootstrap diode of Motion SPM 45 V4 product has special V_F characteristics to be used without additional bootstrap resistor. Therefore, only external bootstrap capacitors are needed to make bootstrap circuit.

The characteristics of the built−in bootstrap diode in the Motion SPM 45 V4 products are:
Fast recovery diode: more than 600 V / 2 A
Resistive characteristic: equivalent resistor of approximately 15 Ω.

Table 16. SPECIFICATION FOR INTEGRATED BOOTSTRAP CIRCUIT shows the specification of bootstrap circuit. Figure 26 shows forward voltage drop of the bootstrap diode.

Table 16. SPECIFICATION FOR INTEGRATED BOOTSTRAP CIRCUIT

Symbol	Item	Conditions	Typ	Unit
VF	Forward Voltage	I_F = 0.1 A, Tc = 25°C	2.5	V
trr	Reverse − Recovery Time	I_F = 0.1 A, dI_F/dt = 50 A/μs, Tc = 25°C	80	ns

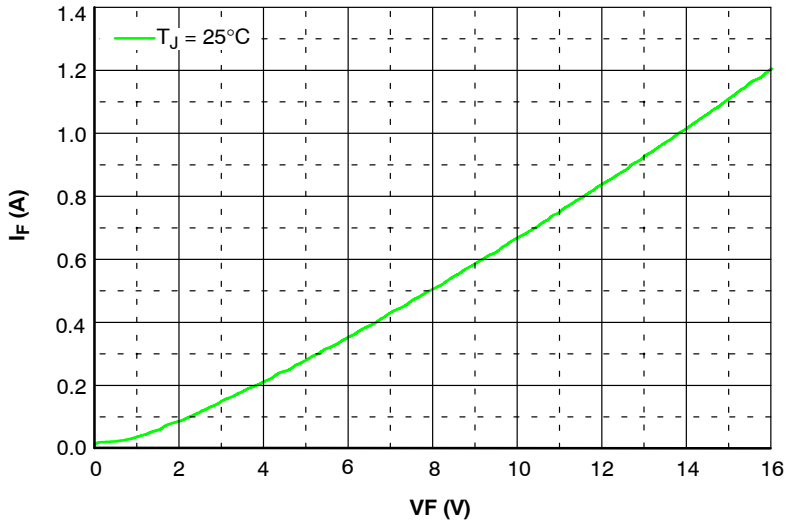


Figure 26. V – I Characteristics of Bootstrap Circuit in SPM 45 V4 Series Products

Temperature Monitoring Method

The Motion SPM 45 V4 series includes a Negative Temperature Coefficient (NTC) thermistor for module internal temperature sensing. This thermistor is located in ceramic substrate with the power chip (RC–IGBT).

Therefore, the thermistor can accurately reflect the temperature of the power chip (see Figure 27).

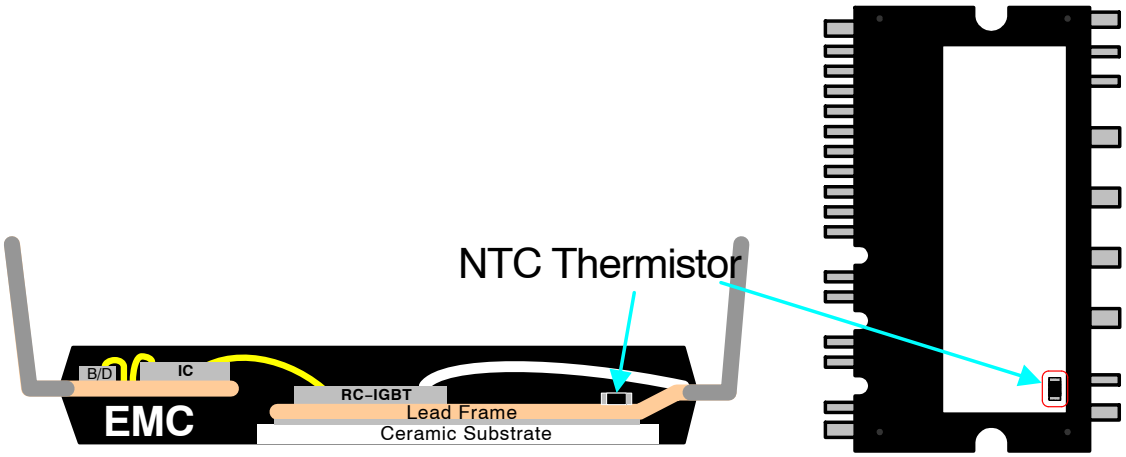


Figure 27. Location of NTC Thermistor in Motion SPM 45 V4 Series Package

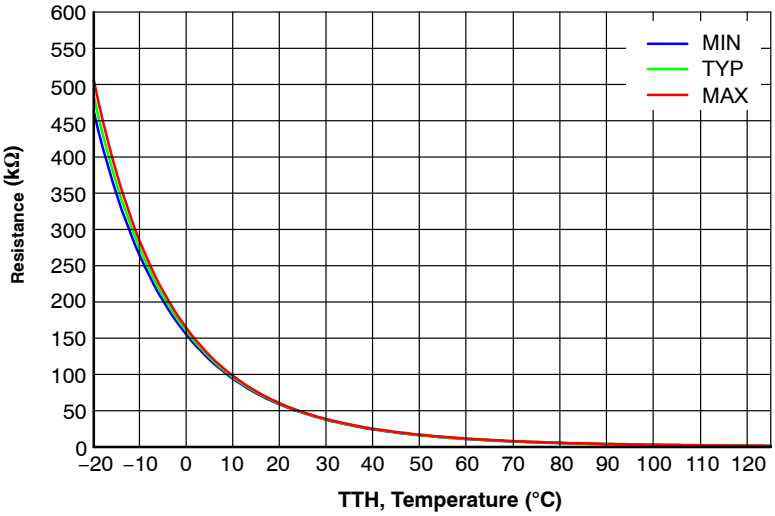


Figure 28. R – T Curve of NTC Thermistor in Motion SPM 45 V4 Series Package

Normally, circuit designers use two kinds of circuit for temperature protection (monitoring) by NTC thermistor. One is circuit by Analog–Digital Converter (ADC). The other is circuit by comparator. Figure 29 shows examples of application circuits with an NTC thermistor.

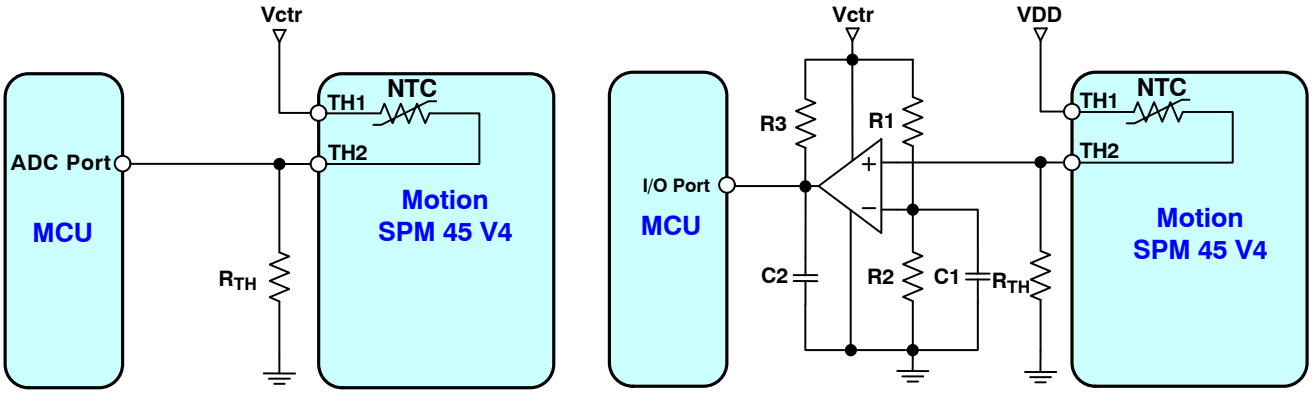


Figure 29. Over Temperature Protection Circuit by MCU and Comparator

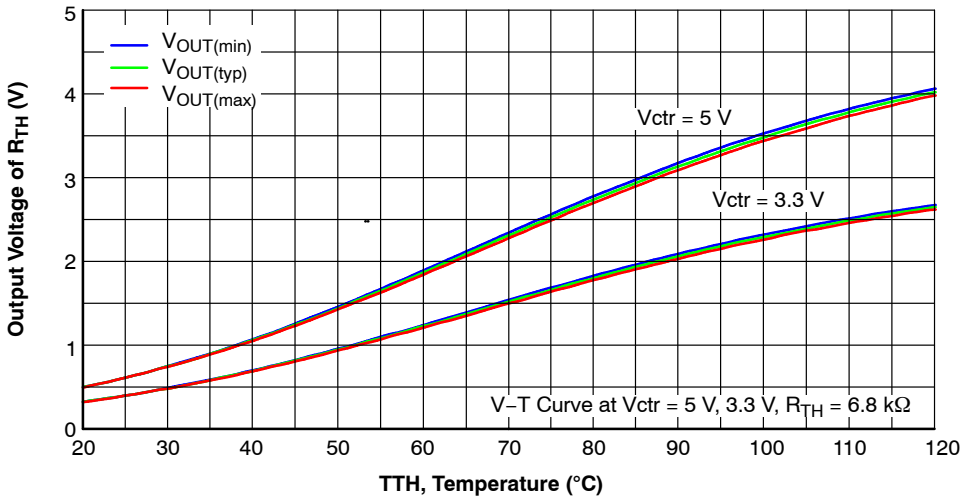


Figure 30. V – I Curve of Recommended NTC Thermistor Circuit

Table 17. THERMISTOR CHARACTERISTICS

Item	Symbol	Conditions	Min	Typ	Max	Unit
Resistance	R25	T_C = 25°C	46.530	47.000	47.470	kΩ
Resistance	R125	T_C = 125°C	1.320	1.406	1.497	kΩ
B–Constant (25–50°C)	–	B	4009.5	4050.0	4090.5	K
Temperature Range	–	–	–40	–	+125	°C

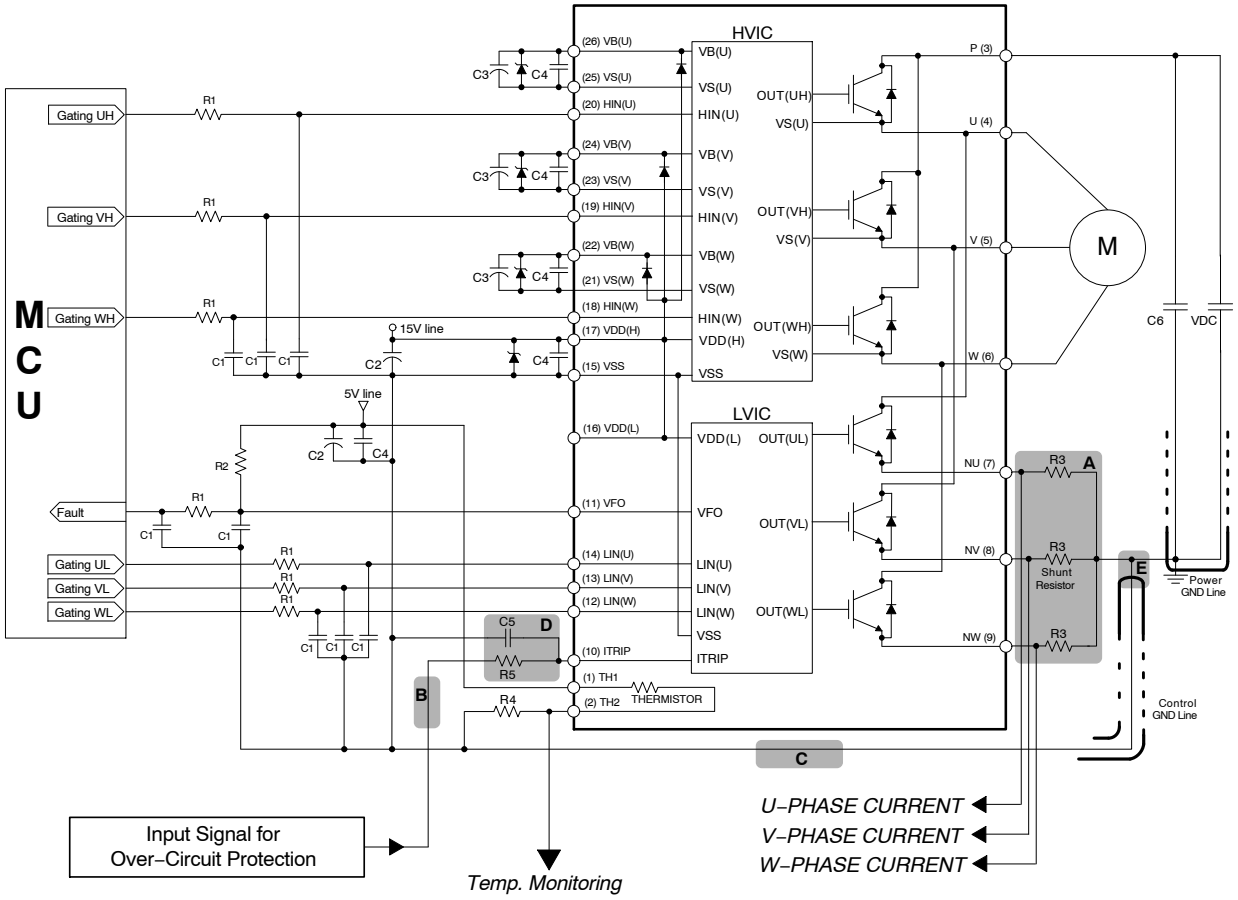
Table 18. R−T TABLE OF NTC THERMISTOR

T_{NTC} (°C)	R_{min} (kΩ)	R_{cent} (kΩ)	R_{max} (kΩ)	T_{NTC} (°C)	R_{min} (kΩ)	R_{cent} (kΩ)	R_{max} (kΩ)	T_{NTC} (°C)	R_{min} (kΩ)	R_{cent} (kΩ)	R_{max} (kΩ)
0	153.8063	158.2144	162.7327	42	22.1759	22.6466	23.1249	85	4.4694	4.6736	4.8866
1	146.0956	150.1651	154.3326	43	21.2753	21.7401	22.2129	86	4.3228	4.5226	4.731
2	138.8168	142.5725	146.4152	44	20.4158	20.8746	21.3416	87	4.1817	4.3771	4.5811
3	131.9431	135.4081	138.9502	45	19.5953	20.0478	20.5088	88	4.0459	4.2369	4.4366
4	125.4497	128.6453	131.9091	46	18.812	19.258	19.7126	89	3.915	4.1019	4.2973
5	119.3135	122.2594	125.2655	47	18.0638	18.5032	18.9514	90	3.789	3.9717	4.1629
6	113.5129	116.2273	118.9947	48	17.3492	17.7818	18.2234	91	3.6675	3.8463	4.0334
7	108.0276	110.5275	113.0739	49	16.6663	17.0921	17.5269	92	3.5505	3.7253	3.9084
8	102.8388	105.1398	107.4814	50	16.0137	16.4325	16.8605	93	3.4377	3.6087	3.7879
9	97.9288	100.0454	102.1974	51	15.3899	15.8016	16.2227	94	3.329	3.4963	3.6716
10	93.2812	95.2267	97.2031	52	14.7934	15.1981	15.6122	95	3.2242	3.3878	3.5593
11	88.8803	90.6673	92.481	53	14.223	14.6205	15.0277	96	3.1235	3.2836	3.4515
12	84.7119	86.3519	88.0148	54	13.6773	14.0677	14.4678	97	3.0264	3.183	3.3473
13	80.7624	82.2661	83.7894	55	13.1552	13.5385	13.9316	98	2.9328	3.086	3.2468
14	77.019	78.3963	79.7903	56	12.6556	13.0318	13.4178	99	2.8425	2.9923	3.1497
15	73.47	74.7302	76.0043	57	12.1774	12.5465	12.9255	100	2.7553	2.9019	3.0559
16	70.1042	71.2558	72.4189	58	11.7195	12.0815	12.4536	101	2.6712	2.8146	2.9654
17	66.9112	67.962	69.0224	59	11.281	11.6361	12.0011	102	2.5901	2.7303	2.8779
18	63.8812	64.8386	65.8039	60	10.861	11.2091	11.5673	103	2.5117	2.6489	2.7933
19	61.005	61.8759	62.753	61	10.4594	10.8007	11.152	104	2.436	2.5703	2.7117
20	58.2739	59.0647	59.8601	62	10.0746	10.4091	10.7536	105	2.363	2.4943	2.6327
21	55.6798	56.3961	57.116	63	9.7058	10.0336	10.3714	106	2.2921	2.4206	2.556
22	53.2152	53.8628	54.5127	64	9.3522	9.6734	10.0046	107	2.2236	2.3493	2.4819
23	50.8732	51.4569	52.0422	65	9.0133	9.3279	9.6525	108	2.1575	2.2805	2.4102
24	48.6469	49.1715	49.6969	66	8.6882	8.9963	9.3145	109	2.0936	2.2139	2.3409
25	46.5300	47.0000	47.4700	67	8.3764	8.6782	8.9899	110	2.0319	2.1496	2.2739
26	44.4567	44.936	45.4159	68	8.0773	8.3727	8.6782	111	1.9725	2.0877	2.2094
27	42.4868	42.9737	43.4618	69	7.7902	8.0795	8.3787	112	1.9151	2.0278	2.147
28	40.6147	41.1075	41.6021	70	7.5147	7.7979	8.091	113	1.8596	1.9699	2.0866
29	38.8351	39.3323	39.8319	71	7.2496	7.5268	7.8138	114	1.806	1.9139	2.0282
30	37.1428	37.6431	38.1463	72	6.995	7.2663	7.5474	115	1.7541	1.8598	1.9716
31	35.5329	36.0351	36.5408	73	6.7505	7.016	7.2913	116	1.7042	1.8076	1.9171
32	34.0011	34.5041	35.0111	74	6.5157	6.7755	7.045	117	1.6559	1.7572	1.8644
33	32.5433	33.0462	33.5534	75	6.2901	6.5443	6.8082	118	1.6092	1.7083	1.8134
34	31.1555	31.6573	32.164	76	6.0739	6.3227	6.581	119	1.564	1.6611	1.7639
35	29.834	30.3339	30.8392	77	5.8662	6.1096	6.3624	120	1.5203	1.6153	1.7161
36	28.576	29.0734	29.5764	78	5.6665	5.9046	6.1521	121	1.4777	1.5707	1.6694
37	27.3776	27.8717	28.372	79	5.4745	5.7075	5.9498	122	1.4365	1.5276	1.6242
38	26.2356	26.726	27.2228	80	5.2899	5.5178	5.7549	123	1.3966	1.4858	1.5804
39	25.1472	25.6332	26.1261	81	5.1129	5.3358	5.568	124	1.358	1.4453	1.538
40	24.1094	24.5907	25.0792	83	4.7788	4.9921	5.2145	125	1.3206	1.406	1.4969
41	23.1198	23.596	24.0796	84	4.6211	4.8299	5.0475				

PRINT CIRCUIT BOARD(PCB) DESIGN

General Application Circuit Example

Figure 31 shows a general application circuitry of interface schematic with control signals connected directly to MCU. Figure 32 shows guidance of PCB layout for the SPM 45 V4 series.



NOTES:

44. To avoid malfunction, the wiring of each input should be as short as possible (less than 2 − 3 cm).
45. VFO output is open−drain type. This signal line should be pulled up to the positive side of the MCU or control power supply with a resistor that makes I_{FO} up to 1 mA.
46. Input signal is active−HIGH type. There is a 5 kΩ resistor inside the IC to pull down each input signal line to GND. RC coupling circuits is recommended for the prevention of input signal oscillation. R1C1 time constant should be selected in the range 50~150 ns (recommended R1 = 100 Ω, C1 = 1 nF).
47. Each wiring pattern inductance of point A should be minimized (recommend less than 10 nH). Use the shunt resistor R3 of surface mounted (SMD) type to reduce wiring inductance. To prevent malfunction, wiring of point E should be connected to the terminal of the shunt resistor R3 as close as possible.
48. To insert the shunt resistor to measure each phase current at NU, NV, NW terminal, it makes to change the trip level I_{SC} about the short−circuit current.
49. To prevent errors of the protection function, the wiring of point B, C, and D should be as short as possible.
50. In the short−circuit protection circuit, please select the R5C5 time constant in the range 1.5~2 μs. Do enough evaluation on the real system because short−circuit protection time may vary wiring pattern layout and value of the R5C5 time constant.
51. Each capacitor should be mounted as close to the pins of the Motion SPM 45 product as possible.
52. To prevent surge destruction, the wiring between the smoothing capacitor C6 and the P & GND pins should be as short as possible. The use of a high−frequency non−inductive capacitor of around 0.1~0.22 μF between the P and GND pins is recommended.
53. Relays are used in almost every system of electrical equipment in home appliances. In these cases, there should be sufficient distance between the MCU and the relays.
54. The zener diode or transient voltage suppressor should be adopted for the protection of ICs from the surge destruction between each pair of control supply terminals (recommended zener diode is 22 V / 1 W, which has the lower zener impedance characteristic than about 15 Ω).
55. C2 of around seven times larger than bootstrap capacitor C3 is recommended.
56. Please choose the electrolytic capacitor with good temperature characteristic in C3. Also, choose 0.1~0.2 μF R−category ceramic capacitors with good temperature and frequency characteristics in C4.

Figure 31. General Application Circuit for Motion SPM 45 V4 Series

PCB Layout Guidance

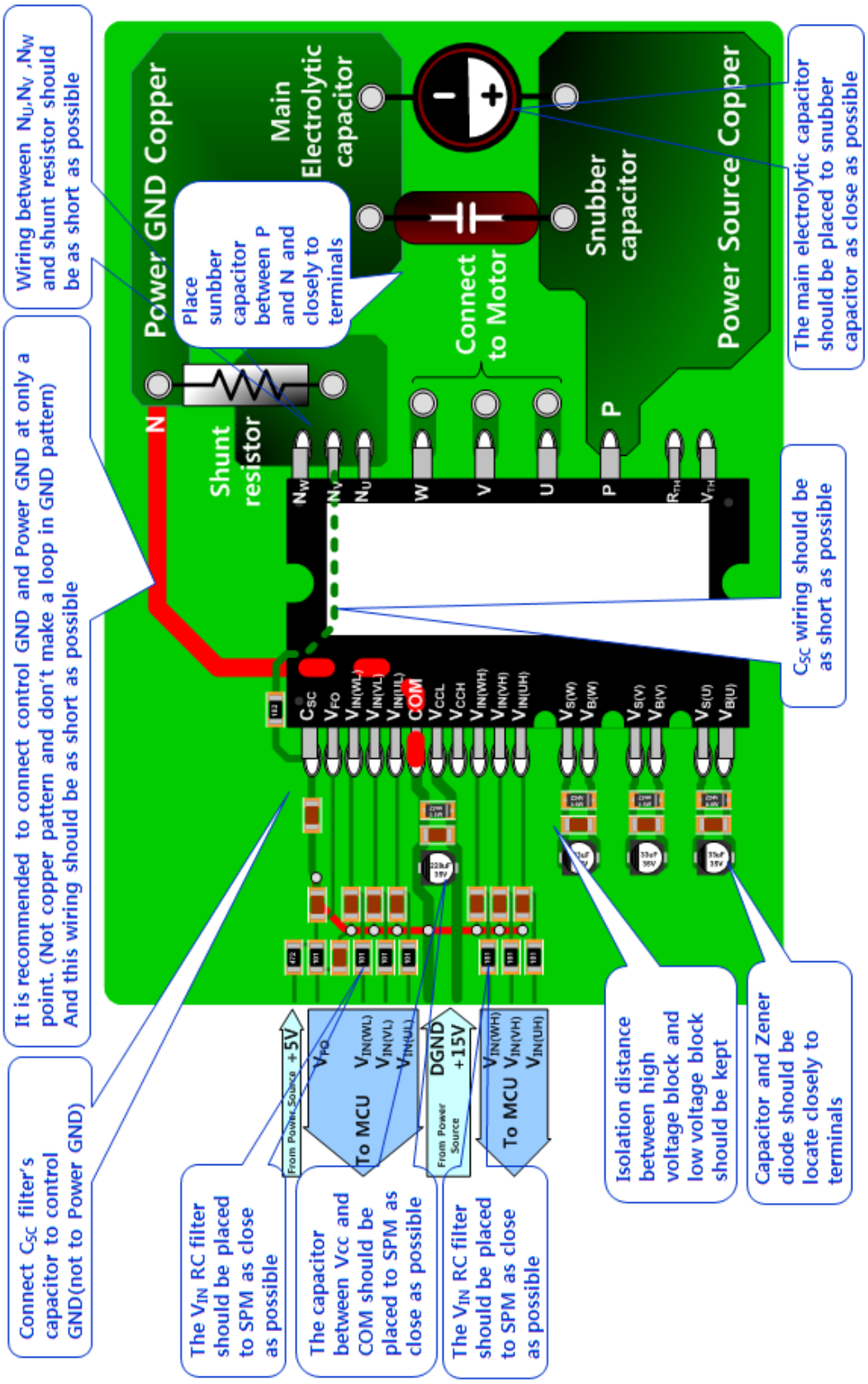


Figure 32. Print Circuit Board (PCB) Layout Guidance for Motion SPM 45 V4 Series

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