NB7NQ621M Single I2C Setting for HDMI1.4/2.1/FRL Mode Compliance

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INTRODUCTION

This application note gives an insight to the method of using NB7NQ621M HDMI redriver by using single I2C setting to pass the HDMI1.4 and HDMI2.1 TMDS and FRL mode compliance.

The application note is to be used along with the NB7NQ621M Datasheet. This application note looks at a method of implementation. It also gives a method of passing EMI.

Background

A typical customer application setup will call for usage with different external monitor display modes like 640 * 480p, 720 * 480p and 720 * 576p ‘no deep color mode’ at ≥ 27 MHz frequency.

The system will require multiple settings to meet 7−2 VL compliance and HF1−9 differential impedance test.

Redriver Setting

When the PCH sets our NB7NQ621M in one mode ‘Line to Line Hi−Z’ and when switched to other modes like ‘Line to Line 200 Ω’ or ‘Line to Line 100 Ω’, it is observed that compliance 7−2 VL passes for only the Hi−Z setting and calls for a change of settings to meet other modes.

Refer to Figure 10. Annexure 1 for HDMI 1.4 VL specification. For passing HF1−9 Differential impedance test the setting must be for ‘line to line 100 Ω’.

Hence there is a need for changes from host to support dynamically and control with multiple setting. With the new single setting, there will be no need for host assistance control for the redriver different operation mode.

To avoid this conflicting requirement, we provide a way to use a single I2C setting to pass both 7−2 VL and HF1−9 compliance.

It is to be noted that pin−strap mode will not provide a single setting solution and hence only I2C mode must be used.

Given below Table 1 showing an example of Pass/Fail seen for VL under two different modes for understanding.

Table 1.

Line to Line 100 Ω							Line to Line Hi−Z					
Pass	# Failed	# Trials	Test Name	Actual Value	Margin	P	Pass	# Failed	# Trials	Test Name	Worst Actual	Worst Margin
✗	1	1	7-2: VL Clock +	2.691 V	-4.5 %	L	✓	0	2	7-2: VL Clock +	2.751 V	25.5 %
✗	1	1	7-2: VL Clock -	2.679 V	-10.5 %	L	✓	0	2	7-2: VL Clock -	2.740 V	20.0 %
✗	1	1	7-2: VL D0+	2.688 V	-6.0 %	L	✓	0	2	7-2: VL D0+	2.748 V	24.0 %
✗	1	1	7-2: VL D0-	2.677 V	-11.5 %	L	✓	0	2	7-2: VL D0-	2.732 V	16.0 %

NOTE: To pass VL, > 2.7 V is required with Line to Line Hi−Z.

To understand the above scenario of the failure, we have shown in the Tables below (Table 2 to Table 5) the variations in the redriver variable control for line to line termination with respect to the output swing settings and the mapping of the electrical parameters of data channel – output common mode voltage VCM, VH and VL limit values. It is to be noted that for passing the 7−2 VL compliance, both the termination control and the output swing are at variance.

Table 2. LINE TO LINE 100 Ω OF REDRIVER OUTPUT CHANNEL COMMON MODE VOLTAGE VCM AND VH/ VL INFORMATION

Output Swing	Max Spec	Min Spec	800 mV	1000 mV	1200 mV	1400 mV
VCM			2.90 V	2.80 V	2.70 V	2.60 V
VH	3.30 V	2.90 V	3.10 V	3.05 V	3.00V	2.95 V
VL	2.90 V	2.30 V	2.70 V	2.55 V	2.40V	2.25 V
Single Ended Swing			400 mV	500 mV	600 mV	700 mV

Table 3. LINE TO LINE 200 Ω OF REDRIVER OUTPUT CHANNEL COMMON MODE VOLTAGE VCM AND VH/ VL INFORMATION

Output Swing	Max Spec	Min Spec	800 mV	1000 mV	1200 mV	1400 mV
VCM			3.00 V	2.925 V	2.85 V	2.775 V
VH	3.30 V	2.90 V	3.20 V	3.175 V	3.15V	3.125 V
VL	2.90 V	2.30 V	2.80 V	2.675 V	2.55V	2.425 V
Single Ended Swing			400 mV	500 mV	600 mV	700 mV

Table 4. LINE TO LINE 300 Ω OF REDRIVER OUTPUT CHANNEL COMMON MODE VOLTAGE VCM AND VH/ VL INFORMATION

Output Swing	Max Spec	Min Spec	800 mV	1000 mV	1200 mV	1400 mV
VCM			3.033 V	2.967 V	2.9 V	2.834 V
VH	3.30 V	2.90 V	3.233 V	3.217 V	3.2 V	3.183 V
VL	2.90 V	2.30 V	2.834 V	2.717 V	2.6 V	2.484 V
Single Ended Swing			400 mV	500 mV	600 mV	700 mV

Table 5. LINE TO LINE Hi−Z OF REDRIVER OUTPUT CHANNEL COMMON MODE VOLTAGE VCM AND VH/ VL INFORMATION

Output Swing	Max Spec	Min Spec	800 mV	1000 mV	1200 mV	1400 mV
VCM			3.10 V	3.05 V	3.00 V	2.95 V
VH	3.30 V	2.90 V	3.30 V	3.30 V	3.30 V	3.30 V
VL	2.90 V	2.30 V	2.90 V	2.80 V	2.70 V	2.60 V
Single Ended Swing			400 mV	500 mV	600 mV	700 mV

The below Figure 1 shows the redriver output structure. The ‘R line to line’ is the 100 Ω / 200 Ω / 300 Ω termination between the signal output of positive and negative side.

The ‘R line to line’ Hi−Z means no termination between signal output of positive and negative. The VDD sink is the external power +3.3 V. Practically in the system, the sink side will have 50 Ω to +3.3 V pull up at signal output side.

The redriver output stage current source increases or decreases based on the different output swing settings.

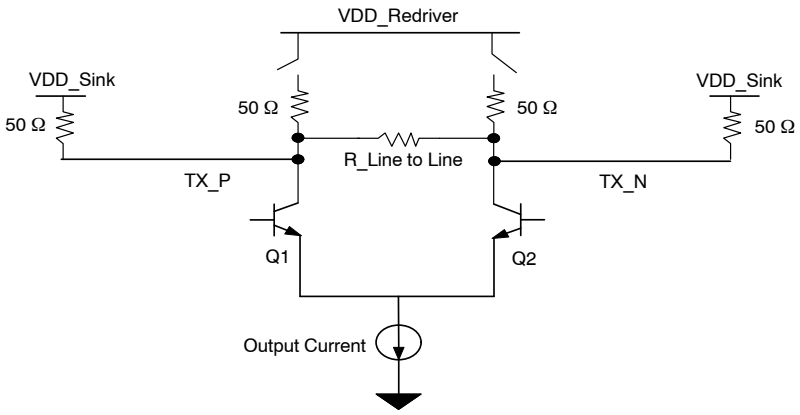


Figure 1. Redriver Output Structure

When doing this test, it must also be ensured that the Impendence Test HF1−9 as given in Figure 2 below also can meet max/min of 100 Ω ± 25% requirement. The source of termination impedance range is 75 Ω to 150 Ω.

The HF1−9 differential measurement result compares the ‘line to line 100 Ω’ and ‘line to line 200 Ω’ of different setting, refer below Figure 3. It shows the smooth curve of the redriver output stage of termination impedance 100 Ω / 200 Ω and also the photo shows an impedance bleed due to the connector used. The line to line 100 Ω condition is into the pass requirement of termination impedance range between 75 Ω to 150 Ω.

The redriver is not impacted by the connector of termination, it is dependent on connector for the performance.

Objective

Confirm that the TMDS impedance of the Source DUT is within the specified limits.

Table 7-17 Source TMDS Electrical - 6G – Differential Impedance Requirements

Reference	Requirement
[HDMI 2.1: Table 6-3] Source Impedance Characteristics for (3.4 Gbps < R_{bit} ≤ 6.0 Gbps) at TP1	- Through Connection Impedance Δ: 100 Ω +/- 15%◊ (recommended) ◊ single excursion is permitted out to a max/min of 100 Ω +/- 25% and of a duration less than 250 ps. Δ Impedance from TP1 to Source Termination - Source Termination Impedance: 75 to 150 Ω

Figure 2. Impedance Table

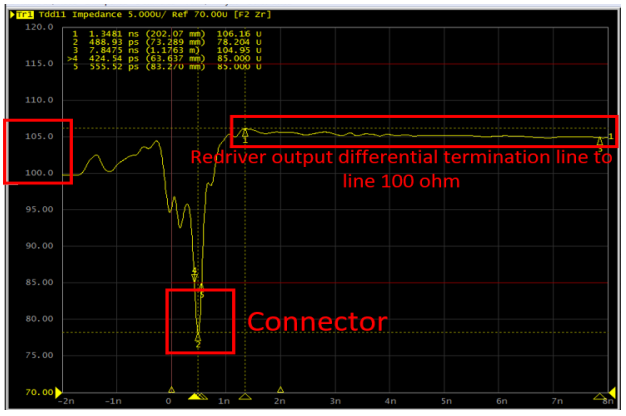
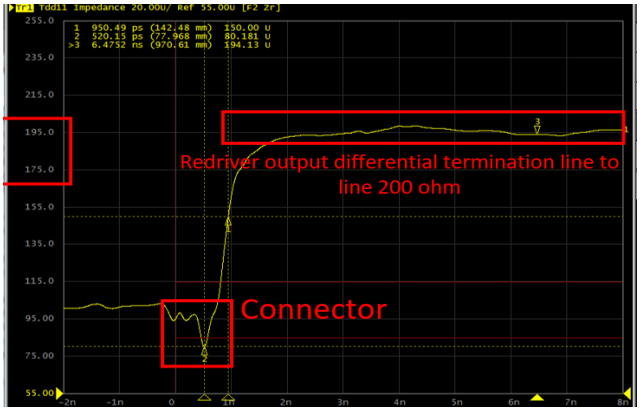
Line to Line 100 Ω	Line to Line 200 Ω
	

Figure 3. Differential Impedance Results

The datasheet provides mapping of the settings for each suitable data rate as shown in Table 6 below:

Table 6. MODE OF OPERATION SETTINGS TABLE FOR I²C MODE, See Register 0x0A

MODE of Operation	Standard	Configuration	Termination	Data Rate [Gbps]	Output Swing
0 (Default)	HDMI	TMDS (DC Coupled Outputs)	High−Z, line to line	0.25 – 1.65	1000 mV
1	HDMI	TMDS (DC Coupled Outputs)	300 Ω, line to line	1.65 – 3.4	1000 mV
2	HDMI	TMDS (DC Coupled Outputs)	200 Ω, line to line	1.65 – 3.4	1000 mV
3	HDMI	TMDS (DC Coupled Outputs)	100 Ω, line to line	3.4 – 6	1000 mV
4	HDMI	FRL (DC Coupled Outputs)	100 Ω, line to line	3 – 12	1000 mV
5	HDMI	FRL (AC Coupled Outputs)	50 Ω to VCC	3 – 12	1000 mV
6	DisplayPort	ML (AC Coupled Outputs)	50 Ω to VCC	2.7 – 8.1	1000 mV

Single I2C Setting to Pass Compliance

Details are given in this section that provides an engineering setting that can pass the HDMI1.4 and HDMI2.1 TMDS compliance.

One of output stage termination control solution is to increase the NB7NQ621M Redriver output common mode voltage and have the termination impedance of 100 Ω. With this, we can use single setting pass HDMI1.4 7−2 VL test requirement over 2.7 V and can meet the HDMI2.1 HF1−9 differential impedance test requirement.

Figure 4 shows an application diagram of using NB7NQ621M in HDMI TMDS and FRL Modes.

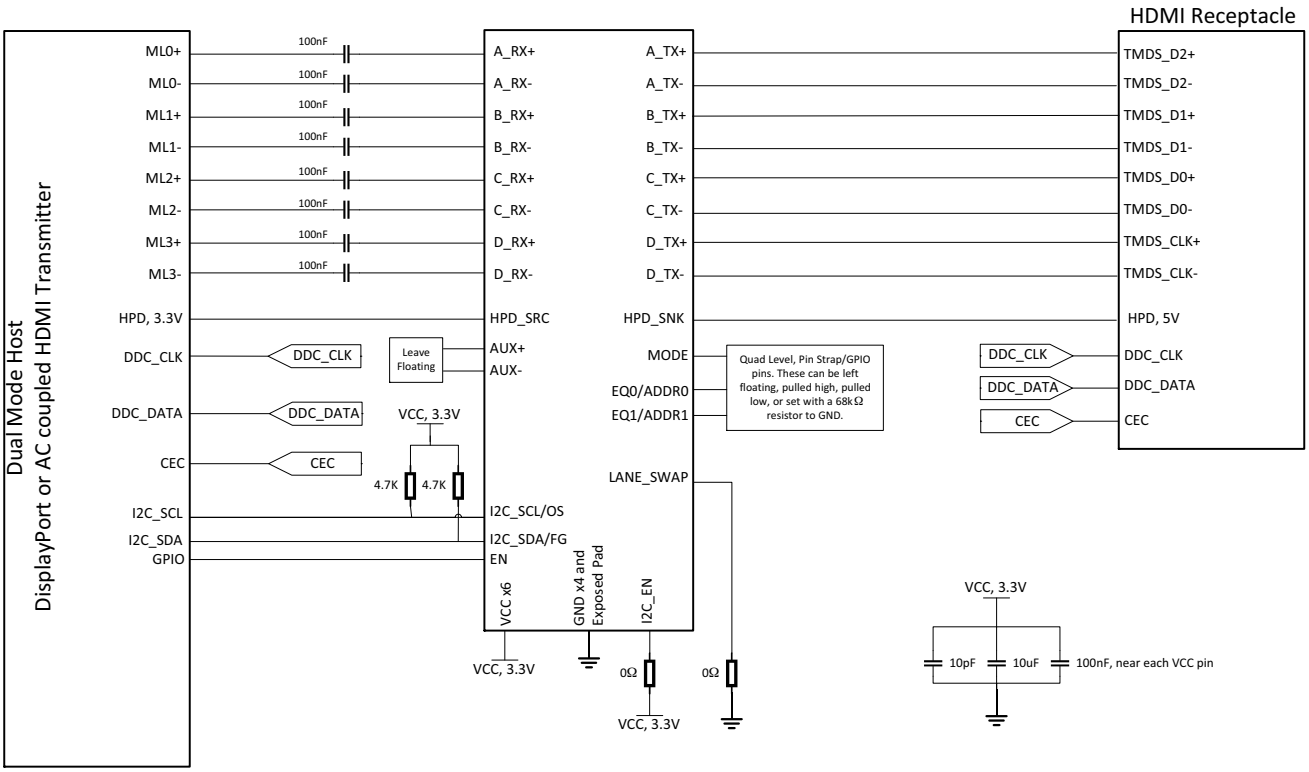


Figure 4. Typical Source Side HDMI Application Circuit Utilizing I2C Communication

Engineering Mode of Output Architecture

The redriver output architecture below shows the positive and negative of signal have 200 Ω line to line impedance and will have engineering mode of the termination output structure that will be equivalent with differential 100 Ω termination. Table 7 shows the engineering mode of common mode voltage and VH/VL limit information.

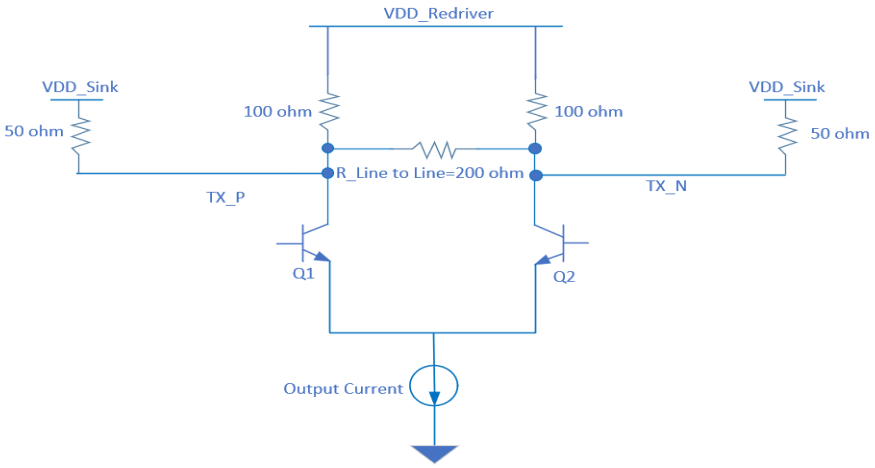


Figure 5. Output Architecture

Single I2C Setting

Given below the I2C register settings for meeting the compliance:

Register – 0X0C −−− Value → x0E
Register – 0X15 −−− Value → x0E
Register – 0X18 −−− Value → x0E
Register – 0X1B −−− Value → x0E
Register – 0X1E −−− Value → x0E

Table 7.

Output Swing	Max Spec	Min Spec	800 mV	1000 mV	1200 mV	1400 mV
VCM			3.033 V	2.967 V	2.90 V	2.833 V
VH	3.30 V	2.90 V	3.233 V	3.217 V	3.20 V	3.183 V
VL	2.90 V	2.30 V	2.833 V	2.717 V	2.60 V	2.483 V
Single Ended Swing			400 mV	500 mV	600 mV	700 mV

Table 7 above shows the engineering mode of redriver output channel common mode voltage VCM and VH / VL information with one of the source systems passing HDMI1.4/2.1 TMDS compliance. Figure 6 and Table 8 below shows I2C setting of values for passing compliance.

The Table 8 given below with bold mark highlight of the values should be followed for redriver engineering termination control setting.

The redriver channel A / B / C / D of EQ, flat gain, output swing and slew rate control is dependent on channel loss and based on Table 8, setting the redriver output swing to 800 mV or 1000 mV enables passing the 7−2 VL specification up to 2.7 V.

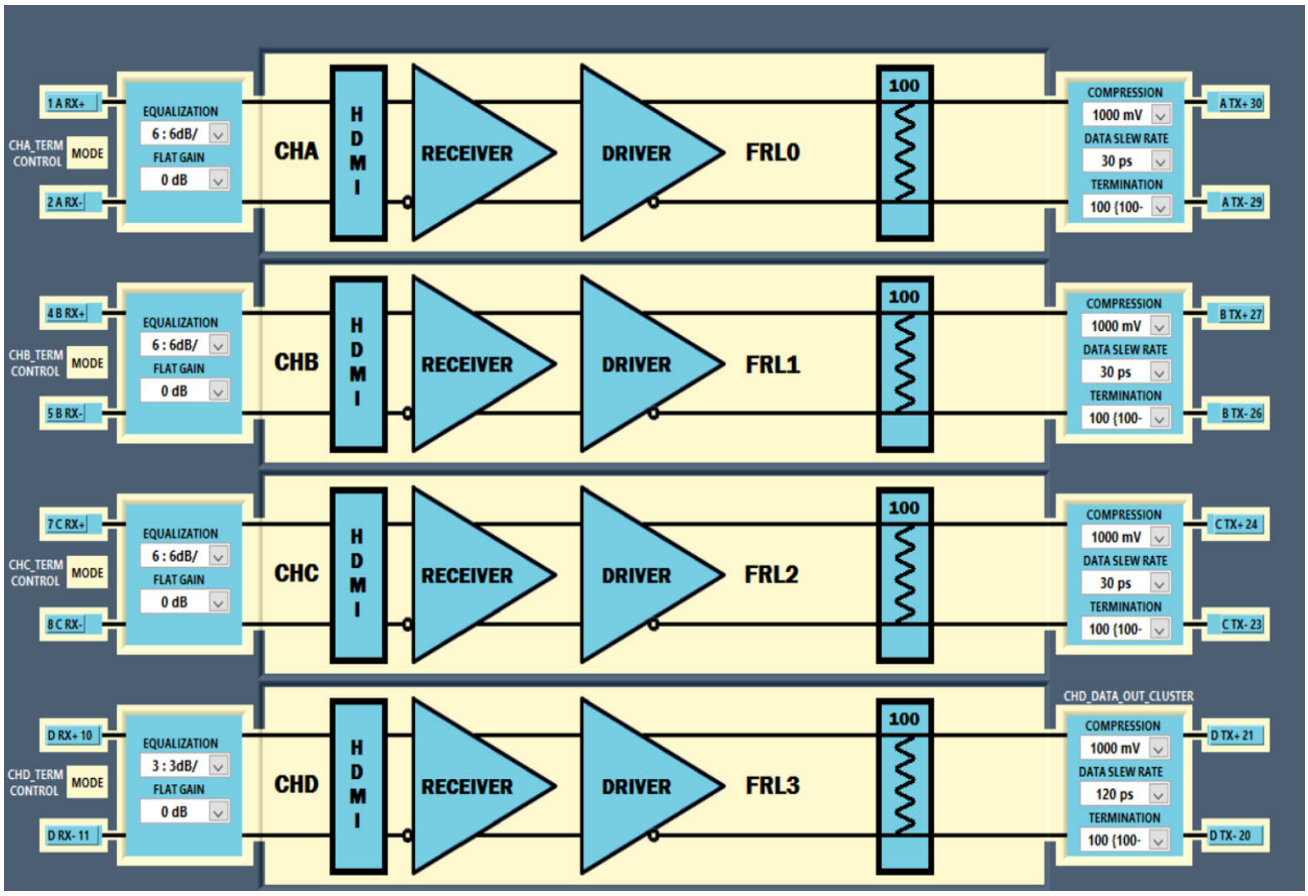


Figure 6. I2C Setting Interface

Table 8. ENGINEERING MODE OF I2C REFERENCE SETTING OF VALUE

Engineering Mode of I2C Reference Setting of Value
0xA; 10100000; xA0 // Induvial and Global control of mode selection
0xB; 00011111; x1F
0xC; 00001110; xE// Global channel termination control
0xD; 00000000; x0
0xE; 00000011; x3
0xF; 00000000; x0
0x10; 00000011; x3
0x11; 00001111; xF
0x12; 10101010; xAA
0x13; 00000000; x0 //Channel A Flat Gain and Output Swing
0x14; 00000110; x6 //Channel A Slew rate and EQ
0x15; 00001110; xE // Channel A Termination control
0x16; 00000000; x0 //Channel B Flat Gain and Output Swing
0x17; 00000110; x6 //Channel B Slew rate and EQ
0x18; 00001110; xE // Channel B Termination control
0x19; 00000000; x0 //Channel C Flat Gain and Output Swing
0x1A; 00000110; x6 //Channel C Slew rate and EQ
0x1B; 00001110; xE // Channel C Termination control
0x1C; 00000000; x0 //Channel D Flat Gain and Output Swing
0x1D; 00000011; x3 // Channel D Termination control
0x1E; 00001110; xE // Channel D Termination control

With one of the customer systems boards, HDMI1.4 7−2 measurement data has been captured and the details are presented below. With this one engineering mode setting, we can pass the HDMI1.4 7−2 VL and HDMI2.0 HF1−9 differential impedance test.

Engineering Termination Control for VL Test

Table 9.

Mode control “100” (FRL DC coupled) and Register address 0x0C / 0x15 / 0x18 / 0x1B / 0x1C = X0E, Output Swing = 1000 mV

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	7−2: VL Clock +	2.780 V	40.0%	Lower Limit V ≤ VALUE ≤ 2.900 V
✓	0	1	7−2: VL Clock −	2.780 V	40.0%	Lower Limit V ≤ VALUE ≤ 2.900 V
✓	0	1	7−2: VL D0 +	2.781 V	40.5%	Lower Limit V ≤ VALUE ≤ 2.900 V
✓	0	1	7−2: VL D0 −	2.779 V	39.5%	Lower Limit V ≤ VALUE ≤ 2.900 V

Engineering Termination Control of Differential Impedance Test HF1−9 Differential Impedance Test

Pass the differential impedance requirement $100\,\Omega \pm 25\%$

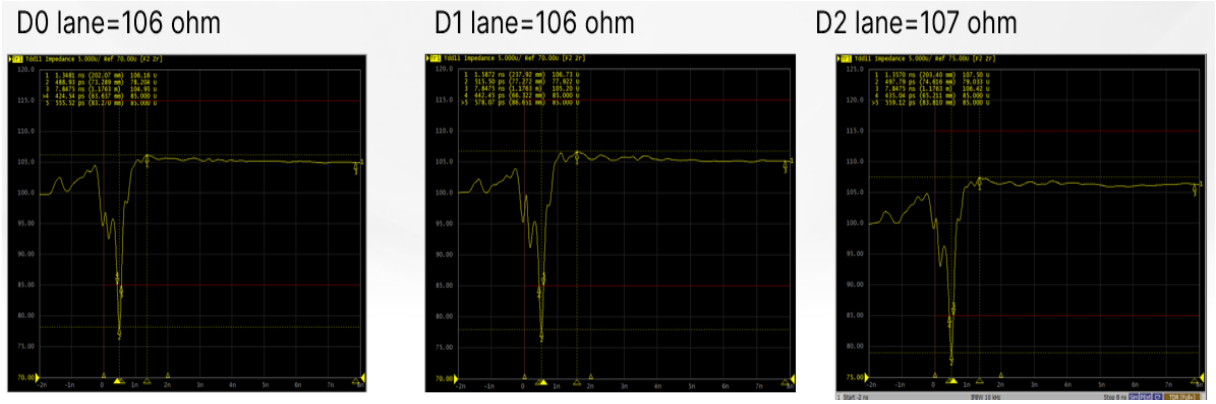


Figure 7. Impedance Test Results

The pass results are shown below in Table 10.

Table 10. HDMI2.1/FRL ELECTRICAL TESTS

Port No.		2nd
Test Item		Remark
HDMI Source Electrical (Phy)	HDMI1.4b Electrical	Pass
	HDMI2.1 TMDS/FRL Electrical	Pass
	HDMI2.1 Impedance	Pass
	Voltage	Pass
HDMI Source non−Electrical (Non−Phy)	EDID	Pass

Eye−Diagram

Tables 11 and 12 give the eye diagram for HDMI2.1 TMDS and FRL. It shows good signal quality with **onsemi** NB7NQ621M HDMI2.1 redriver.

Table 11. HDMI2.1 TMDS 6 Gbps EYE DIAGRAM

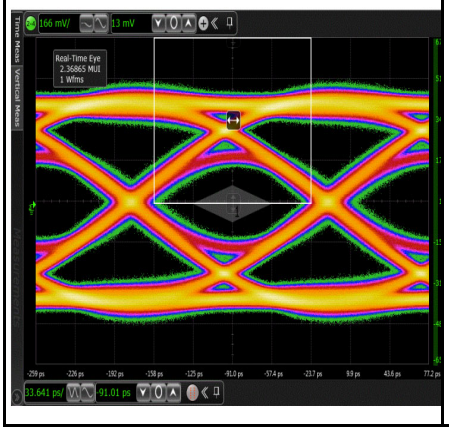
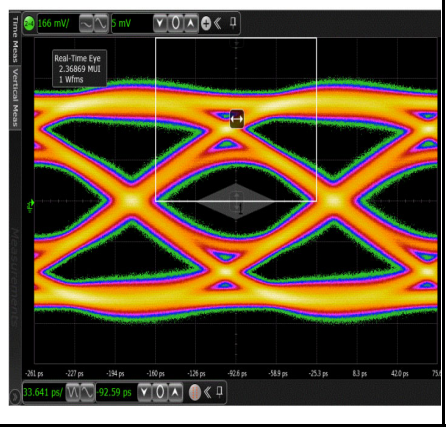
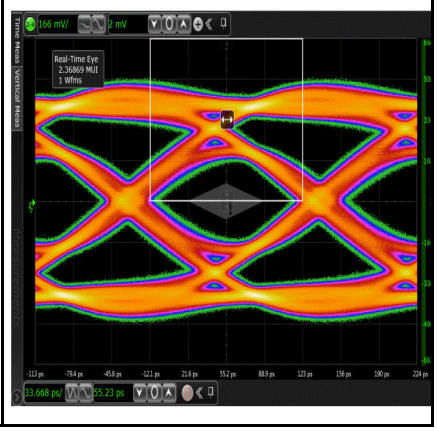
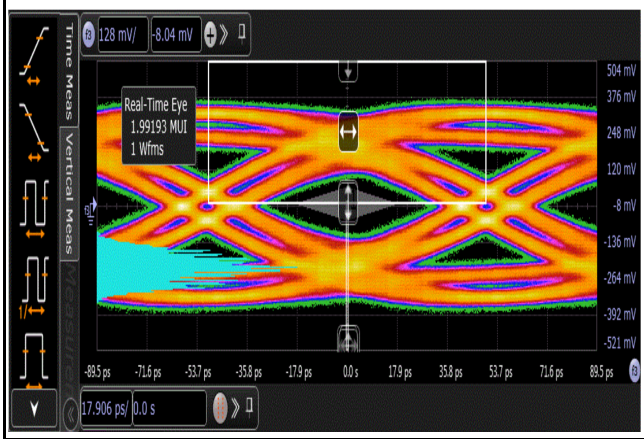
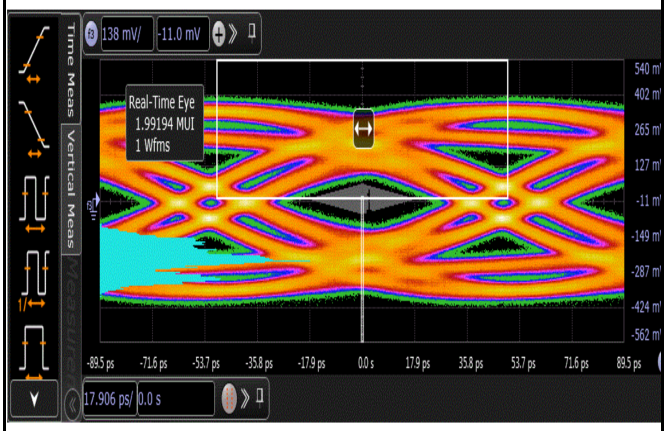
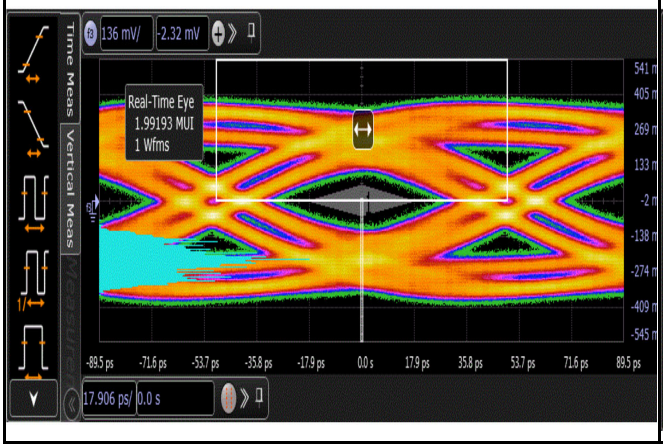
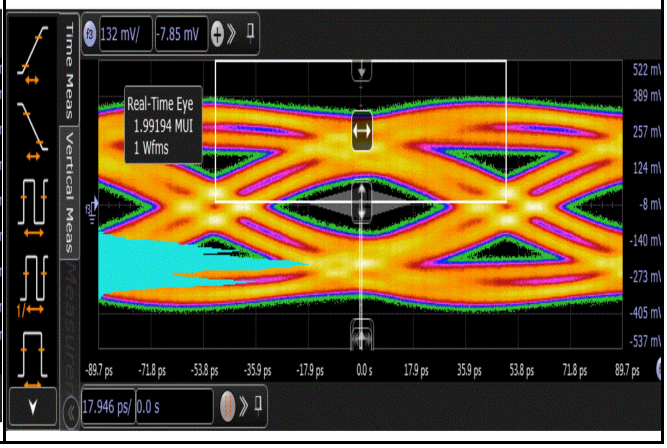
D0 Lane	D1 Lane	D2 Lane
		

Table 12. HDMI2.1 FRL 10 Gbps EYE DIAGRAM

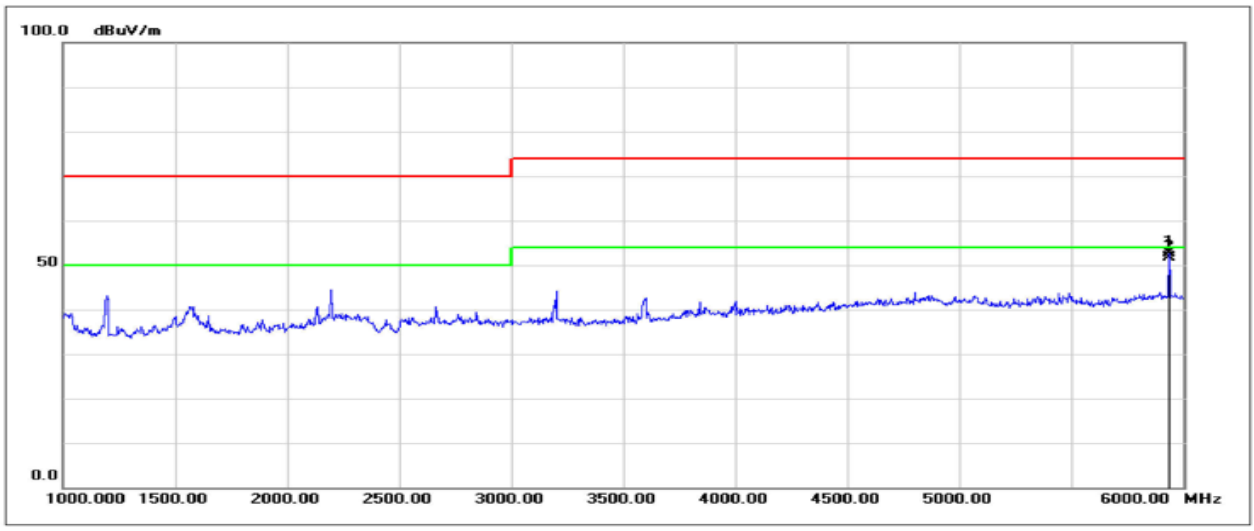
D0 Lane	D1 Lane
	
D2 Lane	**D3 Lane**
	

EMI

For the EMI test, for best results decrease the EQ and slew rate of the redriver channel to get improvement.

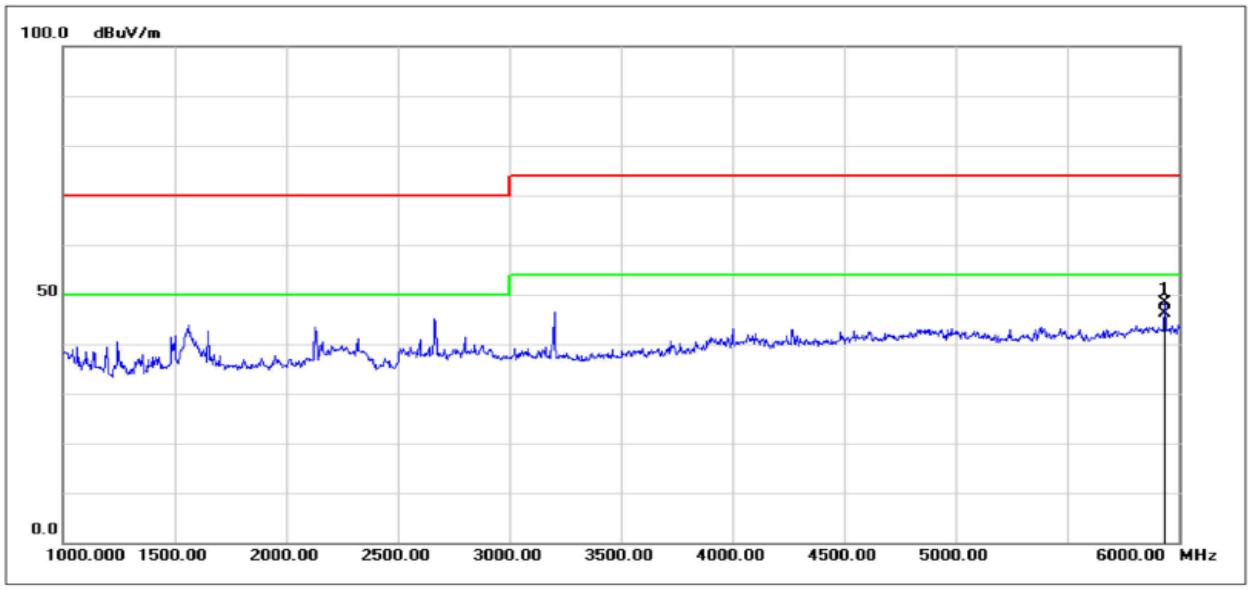
Figures 8 and 9 show one of system HDMI2.1 port with NB7NQ621M Redriver passing the EMI test for the horizontal and vertical scan of test data.

In the figure shown below, the green line is −4 dbμV/m pass EMI of base line in one of system. From the test data is seen that for all of band of frequency – energy is under −10 dbμV/m .



No.	Mk.	Freq.	Reading	Factor	Measurement	Limit	Over	Detector	Comment
		(MHz)	(dBuV)	(dB/m)	(dBuV/m)	(dBuV/m)	(dB)		
1		5935.000	63.07	-10.32	52.75	74.00	-21.25	peak	
2	*	5935.000	62.00	-10.32	51.68	54.00	-2.32	AVG	

Figure 8. Horizontal Scan



No.	Mk.	Freq.	Reading	Factor	Measurement	Limit	Over	Detector	Comment
		(MHz)	(dBuV)	(dB/m)	(dBuV/m)	(dBuV/m)	(dB)		
1		5935.000	58.62	-10.32	48.30	74.00	-25.70	peak	
2	*	5935.000	56.37	-10.32	46.05	54.00	-7.95	AVG	

Figure 9. Vertical Scan

Conclusion

We can conclude that with NB7NQ621M device, it is possible to meet compliance requirement of HDMI display system where applications demand a need for single setting to meet the compliance without involving the system input by using a single I2C setting and meet the EMI requirements.

The above application note provides the details of the required redriver settings.

Reference from Compliance Test Specification	Description

HDMIv1.4b: Table 4-23
Source DC Characteristics at TP1
	Single-Ended low level output voltage, V_L:
	• If attached Sink supports only ≤ 165MHz:
	  ◦ $(AV_{CC} - 600mV) < V_L < (AV_{CC} - 400mV)$
	• If attached Sink supports > 165MHz:
	  ◦ $(AV_{CC} - 700mV) < V_L < (AV_{CC} - 400mV)$

Test Procedure

1. Connect the TPA-P adapter to the Source DUT HDMI output connector.
2. Connect probe to TMDS DATA0-.
3. Configure the EDID to indicate only 27MHz formats (480p and 576p, no Deep Color support) with the 640X480p Established Timings bit set.
4. Control the Source DUT to output a video format with the lowest supported TMDS Clock Frequency (typically 27MHz).
5. Capture at least 16M sample points of waveform and search for 10,000 or more occurrences of an L-H-H-H (or H-L-L-L) bit sequence.
6. Display the voltage (vertical) Histogram on the Oscilloscope, with the Histogram data accumulated only from the last 2-bits of the L-H-H-H sequence.
7. Note the value of $V_{L\text{-}D0\text{-}}$ as the most common low-level voltage shown on the Histogram.
8. If ($V_{L\text{-}D0\text{-}}$ < 2.70V),
   a. Capture 16M sample points of waveform and search for 10,000 or more occurrences of an L-H-H-H (or H-L-L-L) bit sequence.
   b. Display the voltage (vertical) Histogram on the Oscilloscope.
9. Repeat the test for all TMDS DATA0 signals.

Figure 10. Annexure 1

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