

# NCP4318 Tips and Tricks

## AND90154/D

LLC converter is a popular isolated dc-dc power conversion topology for high power applications. The primary-side winding of the transformer in LLC converter sees an ac current of the resonant tank. In lower output voltage scenarios, center-tapped windings are used for the secondary side of the transformer. Two diodes are used to rectify the output current of the secondary windings. To improve conversion efficiency of the LLC converter, people use a synchronous rectification (SR) technique on the output rectifying diodes. Synchronous rectification means using power transistors to replace the diodes. Within the diode conduction time duration, turn on the power transistor to replace the diode's conduction role. It takes the advantage of the on-resistance voltage drop of the power transistor being lower than forward voltage drop of the diodes, thanks to the low on-resistance  $R_{DS(ON)}$  of modern power transistors, such as power MOSFETs.

NCP4318 is a synchronous rectification controller dedicated for LLC converters. Figure 1 shows a typical application circuit of NCP4318. It senses the voltage across drain and source pins of the SR MOSFETs through two sets of VD and VS pins. An  $R_{OFFSET}$  is placed in series of each VD and drain pin connection. NCP4318 has two VG pins to drive the respective SR MOSFET when its body diode can be forward biased. VDD of NCP4318 can be supplied by voltage not higher than 37 V, so the output voltage of the LLC converter can be directly used as NCP4318's power supply. Thus, NCP4318 can control the SR MOSFETs with very low external part counts.

NCP4318 data sheet [1] had introduced basic operation principle of this controller. This application note provides further explanation for its practical operation in different scenarios.

### Drain Voltage of SR MOSFETs

Figure 2 shows an example of the secondary-side currents and voltage waveform of SR MOSFETs. When the current in the  $L_r$  and  $L_m$  of the primary side of the LLC converter diverts from each other, the difference between them becomes the current transferred to the secondary side. Whatever MOSFET or the body diode conducts the secondary-side current, Figure 2 notes the current as  $I_{SD}$ , as the current is flowing from source to drain terminal of the SR MOSFET. When the current flows through M1,  $V_{DS}$  of M1 pulls low. If M2 conducts the secondary-side current,  $V_{DS}$  of M1 shows  $V_{OUT}$  plus reflected voltage from the transformer winding, which makes the voltage amplitude roughly two times of  $V_{OUT}$ .

In a below-resonant operation of the LLC converter, there is a duration that no current is transferred from the primary to the secondary side. The capacitor across the drain and source terminals of the two SR MOSFETs resonates with the equivalent  $L_r$  reflected to the secondary side, making a sub-resonance as in Figure 2.

Zooming in the  $V_{DS}$  and  $I_{SD}$  waveform when the  $I_{SD}$  current conducts, we get a waveform as shown in Figure 3. The body diode of the SR MOSFET conducts first and then NCP4318 generates gate signal, VG, making the SR MOSFET turned on. The amplitude of  $V_{DS}$  change from the forward voltage of the body diode to the voltage drop across the MOSFET's on-resistance. Thus, the conduction loss of the secondary-side current on the rectifying device, which means diodes, can be reduced. The gate signal will be turned off before the  $I_{SD}$  current drop to zero. The time interval between gate turning off and current dropping to zero is the dead time of the SR gate signal.

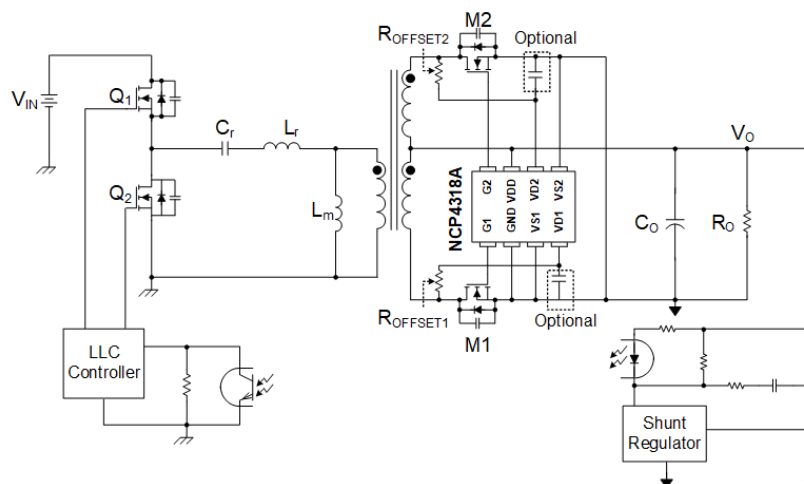
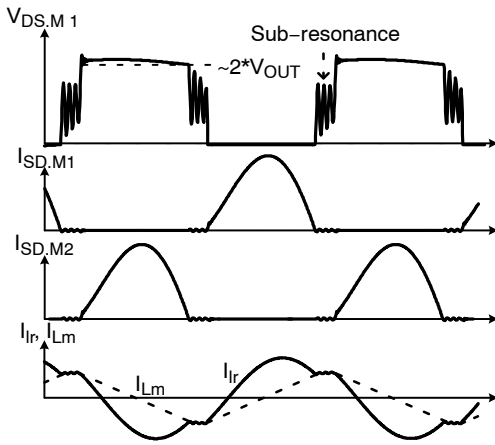
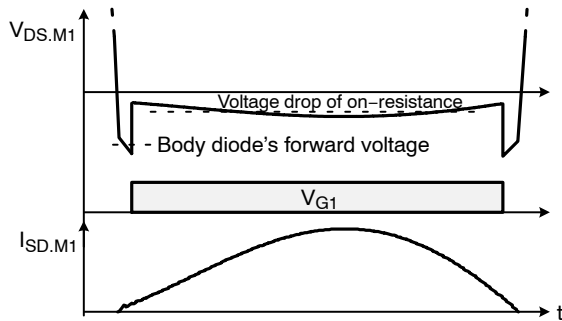


Figure 1. Typical Application Circuit of NCP4318



**Figure 2. Typical SR Current and Voltage Waveforms of a Below-resonant LLC Converter**



**Figure 3. Zoomed-in Waveform of SR Current and Voltage**

**Dead Time Regulation and  $V_{TH-OFF}$  Range**

Figure 4 (a) shows an ideal operating scenario of the SR MOSFET in LLC converters. When the body diode of the SR MOSFET conducts, voltage across its drain and source terminals,  $V_{DS}$ , goes negative. Its amplitude is the forward voltage of the body diode. NCP4318 senses the  $V_{DS}$  to turn on the SR MOSFET when the measured  $V_{DS}$  is lower than a turn-on threshold voltage noted as  $V_{TH-ON}$  in the figure. Since turned on the SR MOSFET,  $V_{DS}$  shows the voltage drop on the  $R_{DS-ON}$ . As the source-to-drain current  $I_{SD}$  drops,  $V_{DS}$  rise to a value close to 0 mV, and NCP4318 turns off the SR MOSFET based on a turn-off threshold voltage  $V_{TH-OFF}$ . Then,  $I_{SD}$  conducts via body diode for the remaining duration of non-zero  $I_{SD}$ .

In practical scenarios, there are parasitic inductance everywhere in the current conducting path. Even if two separate pins are used to sense the differential voltage  $V_{DS}$ ,

stray inductance can still be found in the short PCB trace and the MOSFET package. The stray inductance generates a voltage difference  $V_{LS}$  when amplitude of the flowing-through current changes. The sensed  $V_{DS}$  becomes a summation of  $V_{LS}$  and  $-I_{SD} \cdot R_{DS(ON)}$ . When  $I_{SD}$  drops,  $V_{LS}$  becomes positive, which raises  $V_{DS}$  voltage and makes the SR controller turn off the SR MOSFET prematurely, as shown in Figure 4 (b).

To overcome the premature turn-off phenomenon, NCP4318 has a range of adjustable  $V_{TH-OFF}$  levels and it can adjust the  $V_{TH-OFF}$  by optimizing its turning-off instant and adjusts the  $V_{TH-OFF}$  to regulate the dead time. For avoiding overreaction of the  $V_{TH-OFF}$  adjustment, the optimized dead time is defined as a hysteresis band. NCP4318 adjusts  $V_{TH-OFF}$  higher for the dead time being longer than  $t_{DEAD-HBAND}$  and lower for the dead time being shorter than  $t_{DEAD-LBAND}$ . More, the  $V_{TH-OFF}$  is adjusted with high resolution by the combination of  $V_{TH-OFF}$  and  $I_{OFFSET}$ . These are depicted in Figures 6 and 7.

The  $I_{OFFSET}$  and  $R_{OFFSET}$  changes the  $V_{DS}$  detected in the VD and VS pins, making the turn-off criterion become

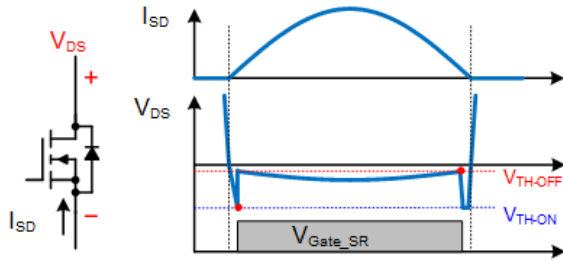
$$V_{DS} + I_{OFFSET} \cdot R_{OFFSET} - V_{TH-OFF} = 0. \quad (eq. 1)$$

So, we can define a virtual  $V_{TH-OFF}$  as a combination of  $V_{TH-OFF}$  and  $I_{OFFSET}$ 's effects as

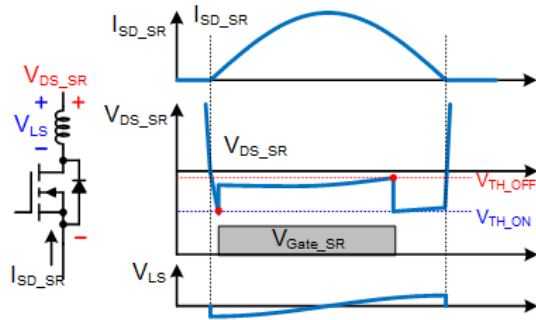
$$Virtual V_{TH-OFF} = V_{TH-OFF} - R_{OFFSET} \cdot I_{OFFSET}. \quad (eq. 2)$$

With both  $V_{TH-OFF}$  and  $I_{OFFSET}$  as variables,  $V_{TH-OFF}$  is defined as larger step and  $I_{OFFSET}$  is defines as smaller step of the adjustment of the virtual  $V_{TH-OFF}$ . Both of them are controlled by 5-bit digital numbers, so there are totally 1024 variations of the combination. Stepping down of the virtual  $V_{TH-OFF}$  can happen in every switching cycle for a fast response. However, stepping up of the virtual  $V_{TH-OFF}$  needs 128 consecutive switching cycles having  $t_{DEAD} > t_{DEAD-HBAND}$ . This is for avoiding too fast dead time reduction that may interfere the feedback loop of LLC control.

$I_{OFFSET}$  varies between 0 and 310  $\mu A$ , and NCP4318 has two different step size for  $V_{TH-OFF}$ . To make the  $I_{OFFSET} \cdot R_{OFFSET}$  fill the step size of  $V_{TH-OFF}$ , the recommended  $R_{OFFSET}$  value is 30  $\Omega$  for  $V_{TH-OFF-STEP} = 8$  mV and 15  $\Omega$  for  $V_{TH-OFF-STEP} = 4$  mV. More, except the  $V_{TH-OFF-STEP}$  options, NCP4318 also has two different options for  $V_{TH-OFF-MIN}$ .  $V_{TH-OFF-MIN}$  and  $V_{TH-OFF-STEP}$  defines the variable range of  $V_{TH-OFF}$ . Larger  $V_{TH-OFF-STEP}$  leads to higher  $V_{TH-OFF-MAX}$ .



a) Without Stray Inductance



a) With Stray Inductance

Figure 4. Effect of Stray Inductance on V<sub>DS</sub>

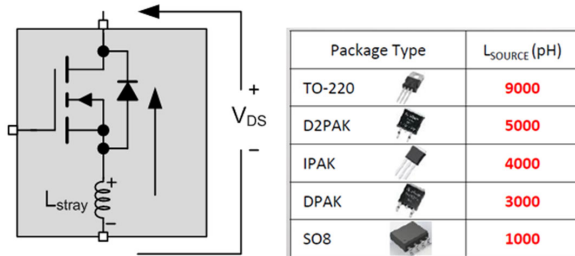


Figure 5. Stray Inductance of the MOSFET Package

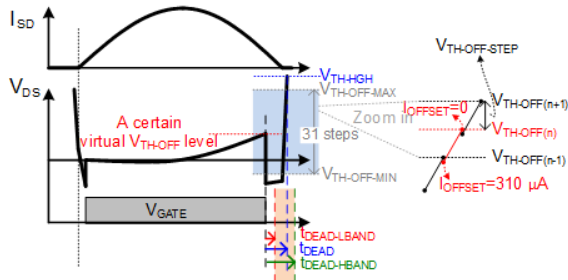


Figure 6. Hysteresis Band of Dead Time Regulation by Adjusting the Virtual V<sub>TH-OFF</sub>

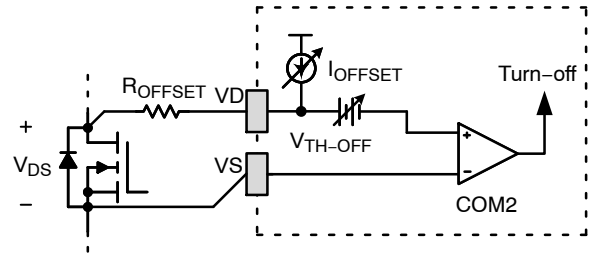


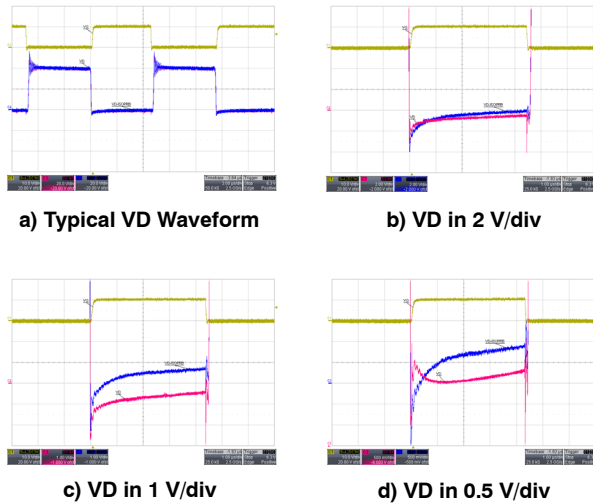
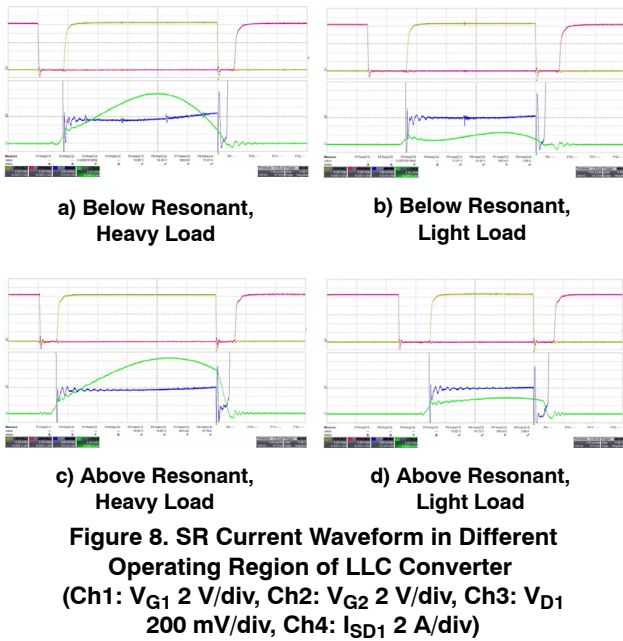
Figure 7. I<sub>OFFSET</sub> and the Virtual V<sub>TH-OFF</sub>

$$V_{TH-OFF-MAX} = V_{TH-OFF-MIN} + 31 \cdot V_{TH-OFF-STEP} \quad (\text{eq. 3})$$

Wider range of V<sub>TH-OFF</sub> may be required when the stray inductance of the SR MOSFET is higher, such as with TO-220 package, or the LLC is operating in below-resonant region mostly. When the LLC converter operates in below-resonant region, as in Figure 8 (a) and (b), variation in current slope tends to be larger. Thus, the effect of stray inductance on V<sub>DS</sub> becomes stronger. If the variable range of V<sub>TH-OFF</sub> is not large enough, the dead time will be larger in heavy load condition. It is due to saturation of the adjustable V<sub>TH-OFF</sub> range; the required V<sub>TH-OFF</sub> for the wanted dead time is higher than V<sub>TH-OFF-MAX</sub>. So, when the dead time is well regulated in light-load conditions and becomes too large in heavy-load conditions, look for V<sub>TH-OFF-STEP</sub> = 8 mV IC option, which provides higher V<sub>TH-OFF-MAX</sub>.

### Inspecting VD Waveform on Oscilloscope

The operation of NCP4318 is based on detecting the voltage across drain and source terminals of SR MOSFETs to decide whether the VG signal should be high or low. For an LLC converter with 19.5 V of output voltage, typical VD waveform is like Figure 9 (a) and has an amplitude of around 40 V, but the portion of interest for VD waveform during the SR operation is in the range of -1~1 V.



**Figure 9. VD Waveforms Captured by an Oscilloscope (Ch1:  $V_{G1}$  10 V/div, Ch2:  $V_{D1}$  by Standard Probe, Ch3:  $V_{D1}$  by Differential Probe)**

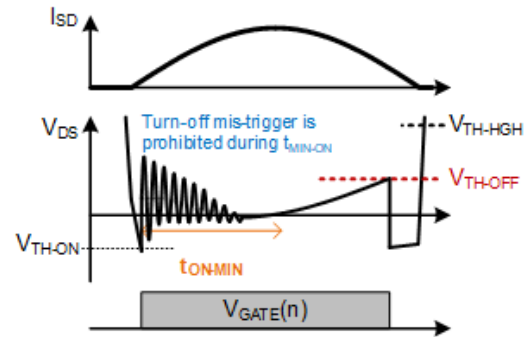
When you try to check VD waveform in the range of interest for NCP4318 by oscilloscope, some non-ideal waveform may be captured due to oscilloscope's characteristics. In the Figure 9, channel #2 and #3 are capturing the same VD signal with different probes. Channel #2 is with standard 10x probe and channel #3 uses a differential probe set at 1/20 of signal ratio. Comparing Figure 9 (b) and (c) for the y-axis zoom-in of the VD signal around 0 V, the shape of VD is slightly different between two kinds of probes. Also, when the voltage scale changes, DC offset of the signal may also change. In Figure 9 (d), the waveform captured by the standard 10x probe is even distorted in its wave shape.

Overall, the waveform captured by differential probes shows a much correct wave shape, but the oscilloscope may introduce some voltage offset at different voltage scale according to the oscilloscope's characteristics. Inspecting the behavior of SR controller by capturing VD signal has no problem but capturing threshold voltage like  $V_{TH-OFF}$  may not be easy in an operating LLC converter.

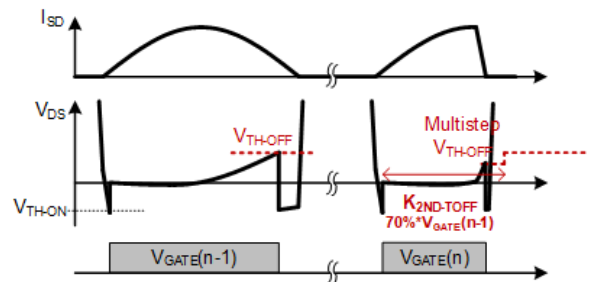
**Minimum On-Time and Multi-Step  $V_{TH-OFF}$**

When SR gate is turning on,  $V_{DS}$  may show ringing due to parasitic components. NCP4318 has a minimum on-time ( $t_{ON-MIN}$ ) to avoid premature gate turning off by the parasitic ringing.

In a load-transient condition under above-resonant operation, the SR conduction time may reduce a lot in consecutive cycles. NCP4318 has a multi-step  $V_{TH-OFF}$  to deal with sudden reduction on the SR conduction time. The multi-step  $V_{TH-OFF}$  means to have lowered  $V_{TH-OFF}$  in a time duration defined as  $K_{2ND-TOFF}$ .



**Figure 10.  $t_{ON-MIN}$  Prevents Premature Turning-Off by Ringing Noise**



**Figure 11. Multistep  $V_{TH-OFF}$  Turns Off SR GATE Earlier when SR Conducting Duration Reduces**

Both  $t_{ON-MIN}$  and  $K_{2ND-TOFF}$  response to operating information of its previous switching cycle, making them adaptive to operating conditions. The  $t_{ON-MIN}$  refers to a SRCOND signal, and  $K_{2ND-TOFF}$  refers to gate on-time. More,  $t_{ON-MIN}$  and  $K_{2ND-TOFF}$  change according to operating-mode flags DLY\_EN and LLD respectively. Definition and variation of SRCOND,  $t_{ON-MIN}$ , and  $K_{2ND-TOFF}$  under different operating modes of NCP4318 are depicted in Figure 12.

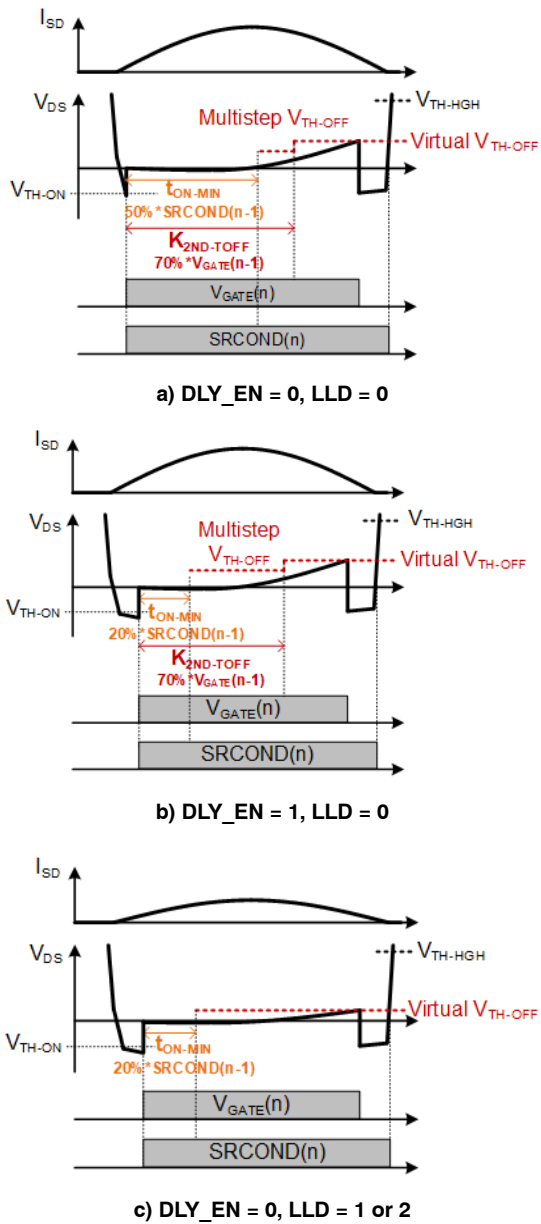


Figure 12.  $t_{ON-MIN}$  and  $K_{2ND-TOFF}$  in Different Modes

**Leading-Edge Inversion Current and  $t_{ON-DLY2}$**

For an LLC converter operating in below-resonant region and light-load condition, current may conduct two times in one switching cycle for a rectifier branch. This phenomenon had been explained in [2] as capacitive current. The main reason is that the amplitude of the  $C_r$  voltage is not enough, so the  $L_r$  current doesn't built up at the beginning of the primary-side on time. However, the  $C_{OSS}$  charging/discharging during the switching transition make the SR MOSFET's body diode conducts for a short period. If SR MOSFET turns on in the short period, it results in leading-edge inversion current in the SR MOSFET conducting duration, which makes additional conduction loss.

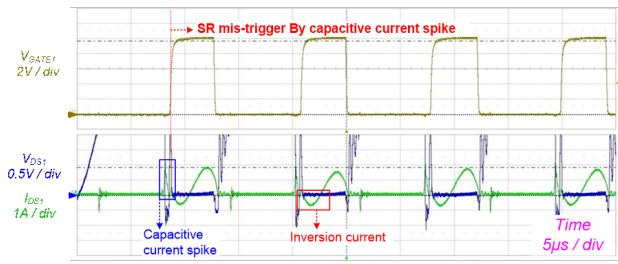


Figure 13. Leading-edge Inversion Current

When the leading-edge inversion current happens, the current inversion detection function SRCINV will be triggered once. Then, turning-on criterion of  $VG1$  and  $VG2$  become requiring  $VD1$  and  $VD2$  to be lower than  $V_{TH-ON}$  continuously for a  $t_{ON-DLY2}$  duration. To avoid conducting inversion current, the  $t_{ON-DLY2}$  needs to be longer than the discharging time of the capacitive current and period of the following sub-resonance.

NCP4318 offers various  $t_{ON-DLY2}$  options from 240 ns to 1580 ns. For an LLC converter operating in above-resonant region,  $t_{ON-DLY2}$  doesn't need to be too long. It may still work in below-resonant region during its input bulk voltage hold-up time during power-off, which is usually a heavy-load condition. However, when an LLC converter can operate in below-resonant region with light load condition, longer  $t_{ON-DLY2}$  may be required for avoiding the leading-edge inversion current.

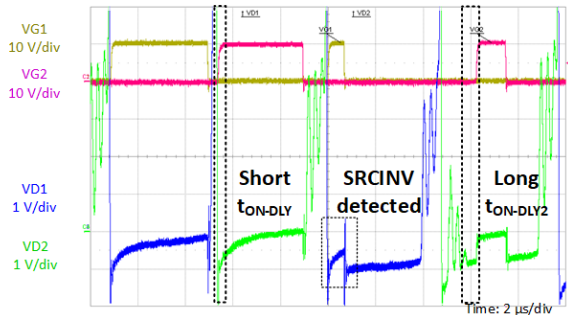


Figure 14.  $t_{ON-DLY}$  Changing Instant

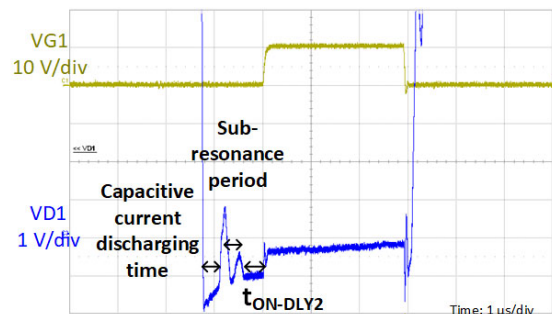


Figure 15.  $t_{ON-DLY2}$  Avoids Inversion Current

SRCINV makes turning-on delay time as the longer  $t_{ON-DLY2}$ , instead of a short  $t_{ON-DLY}$ . To recover back to the short  $t_{ON-DLY}$ , NCP4318 inspects  $V_D$  waveform before SR gate turning on. If  $V_D$  crosses below  $V_{TH-ON}$  for only one time, a  $\eta_{INV-EXT}$  counter adds by one. This counter resets when the  $V_D < V_{TH-ON}$  event happens more than one time in one switching cycle. When the  $\eta_{INV-EXT}$  counter has reached 16000, the criterion of turning on the SR gain recovers back to  $t_{ON-DLY}$ , which is simply a propagation delay. It can also be witnessed in Figure 16 that the recovering from  $t_{ON-DLY2}$  of one channel is independent from the other channel.

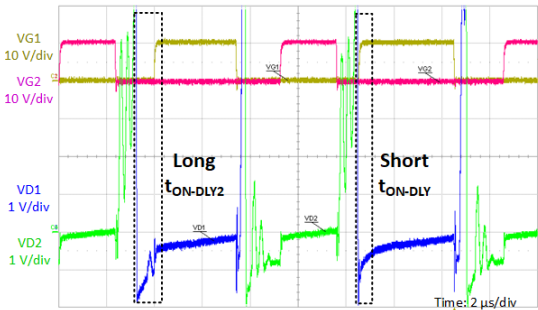


Figure 16. Recovering from the Long  $t_{ON-DLY2}$

**Soft Start and VDD Connection**

Although the steady-state operation of an LLC converter is pulse-frequency modulation (PFM) with designed frequency range, different LLC controllers may have different process of initiating its switching operating after power on. After  $V_{DD}$  exceeds  $V_{DD-GATE-ON}$ , NCP4318 counts switching cycle of the LLC converter and skips the SR gate output for the first 256 cycles to avoid any unpredicted behavior from the LLC controller.  $V_{DD}$  of NCP4318 can be connected to  $V_{OUT}$  or an auxiliary power source. With different connection, the SR gate starts at different moment when the LLC converter start its switching operation.

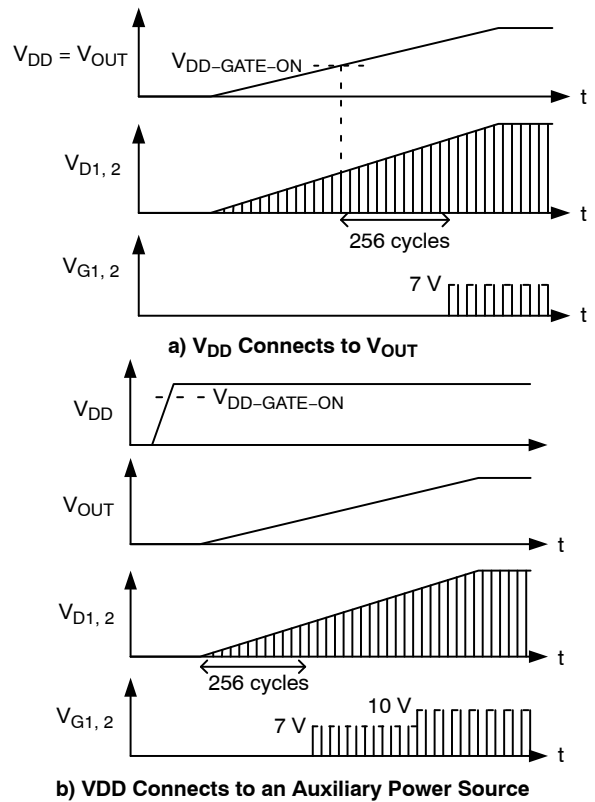


Figure 17. Soft Start

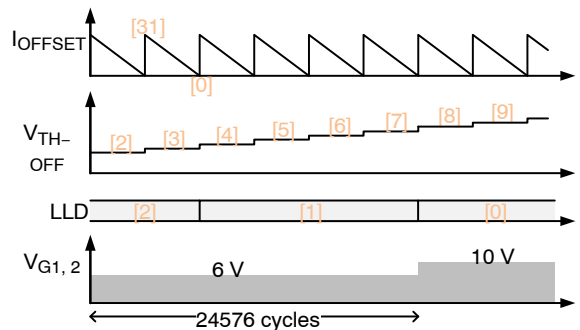


Figure 18.  $I_{OFFSET}$ ,  $V_{TH-OFF}$ , LLD, and  $V_{GATE}$  when the Virtual  $V_{TH-OFF}$  Keeps Increasing

When NCP4318 starts to deliver SR gate signals during soft start, amplitude of  $V_{G1}$  and  $V_{G2}$  starts with 7 V. If the adaptive gate voltage control is not enabled,  $V_{G1}$  and  $V_{G2}$  changes its amplitude to 10 V after another 256 switching cycles. However, when the adaptive gate voltage control is enabled, amplitude of  $V_{G1}$  and  $V_{G2}$  will be decided by the LLD status. Take NCP4318ALC as an example. Its  $V_{TH-OFF-MIN}$ ,  $V_{TH-OFF-STEP}$ , and  $V_{TH-OFF-RST}$  are -6, 4, and 2 mV, which means, at powering on, its  $V_{TH-OFF}$  reset to the 2<sup>nd</sup> step ( $(2\text{ mV} - (-6\text{ mV})) / 4\text{ mV} = 2^{\text{nd}}\text{ step}$ ), in which the 32 steps of  $V_{TH-OFF}$  are noted as 0~31<sup>st</sup> steps.  $V_{GATE}$  amplitude changes to 10 V when the  $V_{TH-OFF}$  is higher than the 7<sup>th</sup> step. Each  $V_{TH-OFF}$  step includes 32 steps of  $I_{OFFSET}$  change, and it takes 128 switching cycles for the virtual  $V_{TH-OFF}$  to increase by one step of  $I_{OFFSET}$  change. Assuming the virtual  $V_{TH-OFF}$  keeps increasing during the process, it will take roughly  $(7 - 2 + 1) \cdot 32 \cdot 128 = 24576$  switching cycles to make  $V_{TH-OFF}$  rise to the level that makes  $V_{GATE}$  change to 10 V. Overall, when the adaptive gate voltage control is enabled, the number of 7 V gate pulses during soft start is much larger than 256.

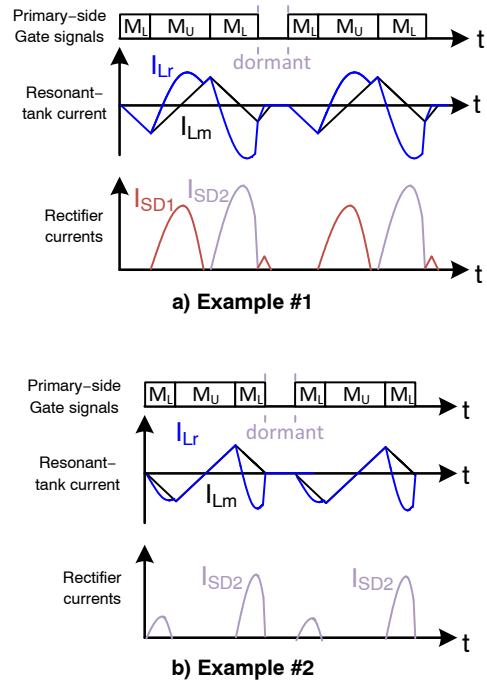
Similar to the soft start, with different VDD connection, SR gate signal stops at different moment when  $V_{OUT}$  drops during power off. In case VDD is supplied from  $V_{OUT}$ ,  $V_{G1}$  and  $V_{G2}$  stops when  $V_{OUT}$  drops below  $V_{DD-GATE-OFF}$  even if the primary side LLC controller still delivers gate pulses to the LLC converter.

**Working with LLC Controllers with a Light-load Mode**

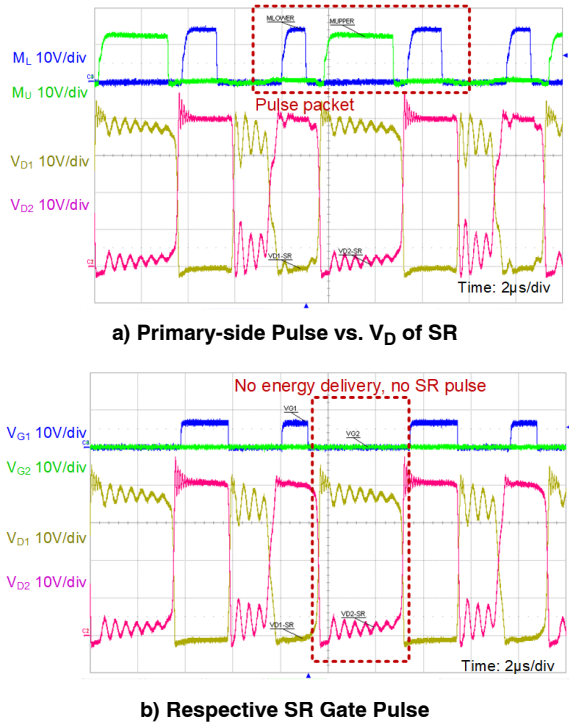
Instead of operating the LLC converter with pulse-frequency modulation (PFM) with 50% of duty cycle, some LLC controller provides special primary-side gate drive pattern to improve light-load efficiency. Let's call it a light-load mode here. The idea is to make the LLC converter delivers similar amplitude of current to the secondary side with similar primary-side pulse on-time, while modulating a dormant duration to adjust average delivered power.

In this mode of operation, the rectifier currents don't grow in every primary-side gate pulse. Whether the rectifier currents grow or not depends on the design of the primary-side pulse packet. For example, in Figure 19, you see  $M_L$ - $M_U$ - $M_L$  primary-side pulse packets. Figure 19 (b) shows shorter on-time in the last  $M_L$  of the packet. It results in no energy delivering during the  $M_U$  pulse duration due to the resulting  $C_T$  voltage in that duration.

Whatever the light-load-mode packet is, while the rectifier currents grow, we want the respective SR gate to turn on, like what we can see in Figure 20. To better cope with the light-load mode operation, you can select NCP4318 with its parameters adjusted as described below.



**Figure 19. Examples of Light-load Mode Current Waveforms**

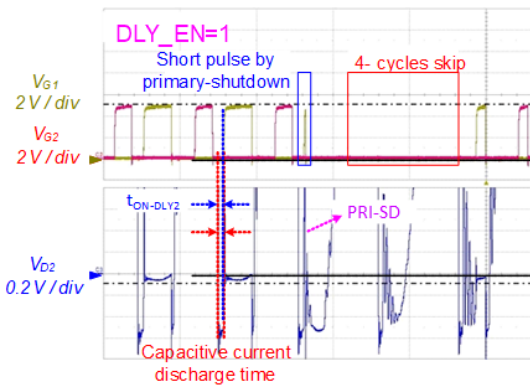


**Figure 20. Waveform of NCP4318 Working with Light-Load Mode**

*Shorter  $t_{ON-DLY2}$*

NCP4318 utilizes  $t_{ON-DLY2}$  to deal with the leading-edge inversion current happening in light-load conditions. When the LLC converter operates in the light-load mode, the leading-edge inversion current may not happen. In addition, the modulated dormant period, which had been indicated in Figure 19, can be longer than  $t_{GRN2-ENT}$ , making  $t_{ON-DLY2}$  be activated. Thus, to work with LLC controllers with such kind of light-load mode, the  $t_{ON-DLY2}$  parameter should be shorter, such as 240 ns in NCP4318AHD.

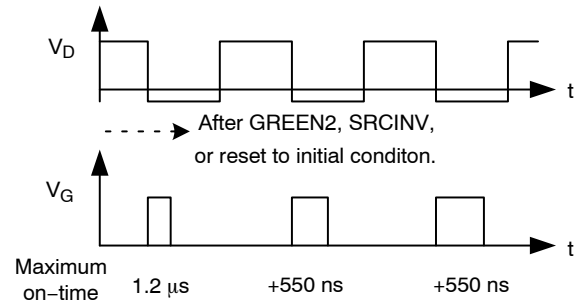
However, sometimes the leading-edge inversion current may still happen in light-load mode. The primary shutdown may be triggered in this condition, as shown in Figure 21. In this situation, slightly longer  $t_{ON-DLY2}$  to cover the capacitive current spike can help the SR operate much stably.



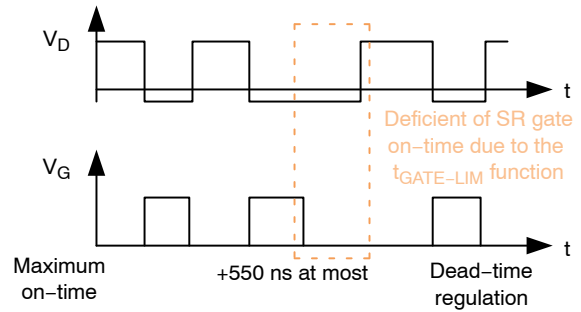
**Figure 21. A Light-load Mode with Leading-edge Inversion Current Makes Primary Shutdown Protection Triggered**

*Disable  $t_{GATE-LIM}$*

The SR conduction duration of the light-load mode may vary a lot in consecutive switching cycles. NCP4318 has an optional  $t_{GATE-LIM}$  function that makes the SR gate on-time increase gradually, as shown in Figure 22 (a). When the SR operation is reset by power-on, SRCINV, or other protections, the on-time of SR gate pulses starts from 1.2  $\mu$ s. The increment rate of the SR gate pulses from their previous cycles is limited to 550 ns. Apparently, that function will make the SR gate on-time always small when the SR conduction duration shows a repetitive short-long-short pattern, as shown in Figure 22 (b). In a light-load mode, the primary-side gate pulses of the LLC converter tend to be not consistent, so as the SR conduction duration. Thus, the  $t_{GATE-LIM}$  function should be disabled to make the SR gate on-time follows the actual conduction duration detected from  $V_{DS}$  signal.



**a)  $t_{GATE-LIM}$  Function**

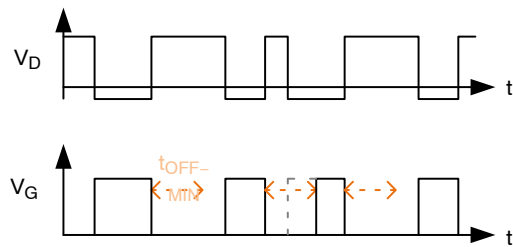


**b)  $t_{GATE-LIM}$  under a Short-long-short Conduction Pattern**

**Figure 22.  $t_{GATE-LIM}$  Function**

*Reduce  $t_{OFF-MIN}$*

NCP4318 has a  $t_{OFF-MIN}$  function which avoids SR gate to be turned on by the noise generated around its turn-off transition. SR gate is prohibited to be turned on again after turning off within a  $t_{OFF-MIN}$  time window. In the light-load mode operation, if the dormant duration, as in Figure 19, is very short, the SR gate may need to be turned on again after it has just been turned off before the short dormant duration. In this condition, we want the  $t_{OFF-MIN}$  parameter of NCP4318 to be shorter.



**Figure 23.  $t_{OFF-MIN}$  Function**

NCP4318 has shorter  $t_{OFF-MIN}$  option for both its H-version and L-version. In addition, since  $t_{ON-DLY2}$  itself can be seen as a minimum off-time, NCP4318 also offers an option to disable  $t_{OFF-MIN}$  when  $t_{ON-DLY2}$  has been activated.

**Estimating Gate-drive Power Consumption**

The operation of SR is to turn on the MOSFET when the body diode is in conduction and turn off the MOSFET to let the body diode takes over at the end of the conducting duration. Load of the gate driver is  $C_{ISS}$  and  $C_{RSS}$  of the MOSFET at  $V_{DS} \approx 0V$ . The VDD pin’s sinking current,  $I_{DD}$ , can be estimated as below.

$$C_{TOTAL} \equiv \sum_{all\_MOSFETs} (C_{ISS}(V_{DS} = 0) + C_{RSS}(V_{DS} = 0)) \quad (eq. 4)$$

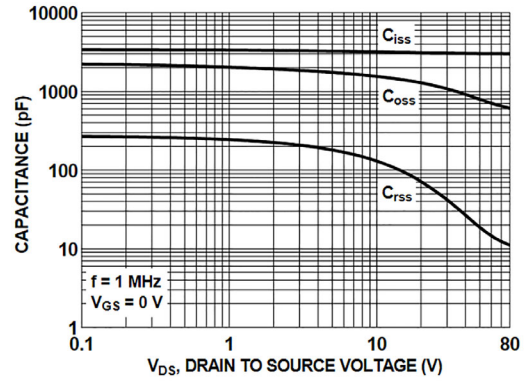
$$I_{DD_{VG\_loaded}} = I_{DD_{VG\_open}} + C_{TOTAL} \cdot V_{GATE} \cdot f_{SW} \quad (eq. 5)$$

For example, the MOSFET FDMS004N08C shows  $C_{ISS} \approx 3200$  pF and  $C_{RSS} \approx 270$  pF. When we put two MOSFET in parallel for each VG channel and make the LLC converter operate at 103 kHz at full load, the total average current consumption of the gate drivers is  $(3200 \text{ pF} + 270 \text{ pF}) \times 2 \times 2 \times 10.5 \text{ V} \times 103 \text{ kHz} = 15 \text{ mA}$ . When  $V_G$  pins are open, the measured  $I_{DD}$  is as 3 mA. So, the total  $I_{DD}$  is 18 mA.

$$E_{DRV-SOURCE} = (V_{DD} \cdot C_{TOTAL} \cdot V_{GATE-MAX} - 0.5 \cdot C_{TOTAL} \cdot V_{GATE-MAX}^2) \cdot \frac{R_{DRV-SOURCE}}{R_{DRV-SOURCE} + R_G} \quad (eq. 6)$$

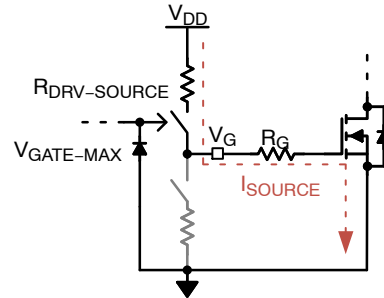
which implied that part of power dissipation will be directed from  $R_{DRV-SOURCE}$  to the external  $R_G$ . Also, the total energy that needs to be dissipated during gate turning off is  $0.5 \times C_{TOTAL} \times V_{GATE-MAX}^2$ . The turn-off energy can be directed to an external PNP bipolar transistor when it is used in the turn-off circuit. However, with the simplest connection in Figure 1, which connects VG pins to MOSFET’s gate terminal without any additional elements, the gate drive power dissipation will be all on the NCP4318 chip.

$$P_{DRV} = V_{DD} \cdot C_{TOTAL} \cdot V_{GATE-MAX} \cdot f_{SW} \quad (eq. 7)$$

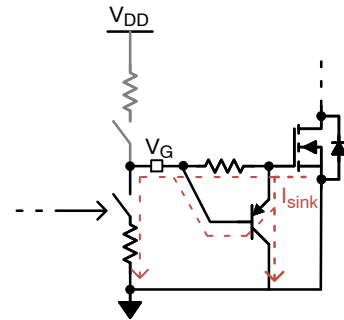


**Figure 24. Capacitance vs.  $V_{DS}$  Drawing for FDMS004N08C**

The total power consumption of NCP4318 is  $V_{DD} \cdot I_{DD}$ , but not all power needs to be eventually dissipated as heat on NCP4318. The gate-drive portion of the power consumption have some variation based on external circuitry. For example, when there is a series resistor  $R_G$  in the turning-on current path, it slows down the turn-on slew rate and makes the power dissipated on  $R_{DRV-SOURCE}$  becomes



**a) Gate Current Sourcing**



**b) Gate Current Sinking**

**Figure 25. Gate Current Sourcing and Sinking Situation with Additional Elements**

**Keeping MOSFET Turn-on Delay Time within  $t_{DB-HGH}$**

We have mentioned a  $V_{TH-HGH}$  parameter in previous paragraphs.  $V_{TH-HGH}$  defines the end of SRCOND signal as in Figure 12 and so involves in definition of dead time as in Figure 6. The value of  $V_{TH-HGH}$  is much higher than  $V_{TH-OFF}$ .  $V_D > V_{TH-HGH}$  indicates finish of current conduction in MOSFET or its body diode. Note that  $V_{TH-OFF}$  is compared with  $V_D - V_S$ , while  $V_{TH-HGH}$  is compared with  $V_D - V_{GND}$ .

The comparison of  $V_D$  and  $V_{TH-HGH}$  has a leading-edge blanking time  $t_{DB-HGH}$ , counting from assertion of the SRCOND signal, which is also the same instant that the gate-drive output starts rising. The value of  $t_{DB-HGH}$  is 450 ns for L-version and 350 ns for H-version NCP4318. Within the leading-edge blanking time,  $V_D > V_{TH-HGH}$  won't reset the SRCOND signal.

The values of these parameters imply a requirement for turning-on of MOSFET:  $V_{TH-HGH}$  being much higher than  $V_{TH-OFF}$  means  $V_D$  won't exceed  $V_{TH-HGH}$  when the MOSFET has been turned on; and, the existence of a leading-edge blanking time means the turning-on process of the MOSFET is expected to be finished within  $t_{DB-HGH}$ . By keeping the turn-on delay within  $t_{DB-HGH}$ , the blanking time helps prevent misjudging the termination moment of the MOSFET or body diode conduction. This ensures that the NCP4318 operates smoothly and stably without unexpected behavior. Otherwise, the SRCOND signal might reset incorrectly, which, in rare cases, could lead to missed triggering of the  $V_{TH-OFF}$  comparator.

So, what's the turn-on delay? GATE and SRCOND signals assert together, and the turning-on of MOSFET is achieved by sourcing a current from the GATE pin to charge the  $C_{ISS}$  of MOSFET, as depicted in Figure 26. The MOSFET is fully turned on when the voltage between its gate and source terminals reaches

$$V_{GS(on)} = V_{GS(th)} \quad (\text{eq. 8})$$

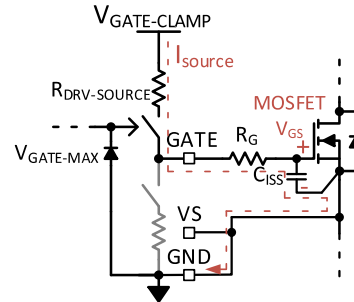
where  $V_{GS(th)}$  is MOSFET turn-on threshold voltage specified on the MOSFET's data sheet. The instant that  $V_{GS}$  reaches  $V_{GS(on)}$  marks the end of turn-on delay. Due to the resistive characteristic of the  $I_{SOURCE}$  path, MOSFET  $V_{GS}$  shows an exponential rising waveform, as shown in Figure 27. If the  $C_{ISS}$  is larger, the turning-on process will take longer time, meaning the turn-on delay will be longer.

To make sure the turning-on process finishes within  $t_{DB-HGH}$ , we suggest checking the MOSFET  $V_{GS}$  waveform in all load conditions in the design. To have some margin, aim at letting MOSFET  $V_{GS}$  exceed  $V_{GS(on)}$  within  $450 * 0.7 = 315$  ns for L-version and  $350 * 0.7 = 245$  ns for H-version NCP4318. If you find the MOSFET  $V_{GS}$  rises too slowly, there are some actions you can take:

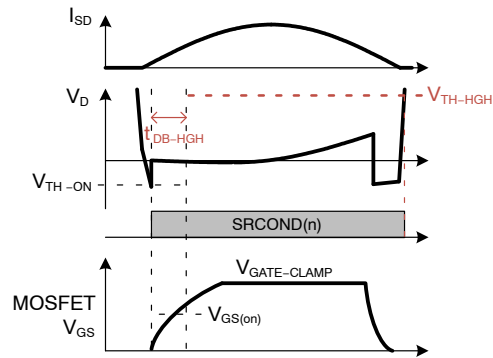
1. Reduce resistance of the  $I_{SOURCE}$  path. You may reduce the  $R_G$  resistance and/or shortening/widening copper trace of the path.
2. Check whether  $V_{GATE-CLAMP}$  is reduced. NCP4318 may have variable  $V_{GATE-CLAMP}$  to reduce gate-driving loss, and the lowered

$V_{GAMP-CLAMP}$  lengthens turn-on delay time of MOSFET. Referring to Adaptive  $V_{GATE}$  Control section in NCP4318 data sheet,  $V_{GATE-CLAMP}$  is adjusted according to  $V_{TH-OFF}$  level (output load condition), switching frequency, and chip junction temperature. Different orderable part numbers of NCP4318 have different triggering thresholds of reducing  $V_{GATE-CLAMP}$  in these regards. When driving large  $C_{ISS}$ , you may want to have multi-level  $V_{GATE}$  and HFS function disabled.

3. Add an external gate driver. When  $C_{ISS}$  is very large, NCP4318's driving capability may not be enough to turn on MOSFET within  $t_{DB-HGH}$ . External gate drivers may have higher driving capability, which means its equivalent  $R_{DRV-SOURCE}$  is lower. The external gate driver can be a gate-driver IC or discrete totem-pole gate-driving circuit.



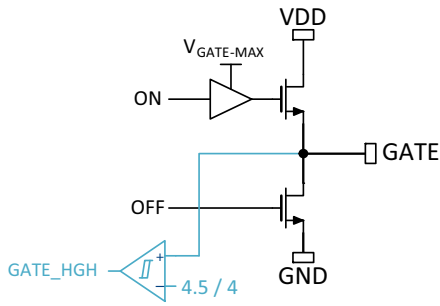
**Figure 26. Gate Turning-on Current-sourcing Path**



**Figure 27.  $t_{DB-HGH}$  and Exponential Rising of MOSFET  $V_{GS}$**

**Damping  $V_{GATE}$  Ringing during GATE Turning-on**

Data sheet of NCP4318 mentioned that the current inversion detection is triggered when “SR gate is turned on and the inversion current occurs”. Also, the test conditions of many protection-related parameters in the electrical characteristics section contains “ $V_{GATE1/2} > 4.5$  V”. These descriptions reflect that NCP4318 has comparators monitoring its GATE-pin voltage. The comparator output is used to judge if protection is allowed to be triggered.

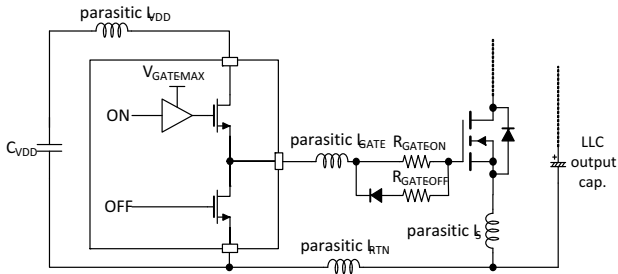


**Figure 28. Comparator for Monitoring GATE Status**

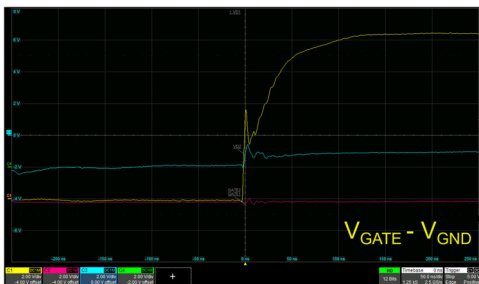
In most cases, protections are triggered nearing the rising edge of a GATE pulse. NCP4318 relies on protections to turn off GATE signals during minimum on-time. To have a clear and firm signal for allowing protections from triggering, GATE signal seen by NCP4318 had better be monotonic rising at its rising edge. Chances are the stray inductance of the gate-driving loop is high enough to make the GATE rising edge show an underdamped response. If you find voltage signal between GATE pin and GND pin is like the Figure 30, increasing  $R_{GATE-ON}$  according to eq.9 can help damping the GATE signal to be monotonic rising.

$$R_{GATE-ON} \geq 2 \cdot \sqrt{\frac{(L_{GATE} + L_S + L_{RTN}) \cdot (C_{ISS} + C_{OUT-DRV})}{C_{ISS} \cdot C_{OUT-DRV}}} \quad (\text{eq. 9})$$

$C_{OUT-DRV}$  is junction capacitance of the gate-driver output. Its value can be estimated as 250 pF based on bench-test result.  $C_{ISS}$  is input capacitance of the SR MOSFET at  $V_{DS} = 0$  V.



**Figure 29. Stray Inductances in Gate-driving Loop**



**Figure 30. GATE-to-GND Voltage Waveform That Shows Non-monotonic Rising**

**PCB Layout Recommendation**

To explain the recommended PCB layout, let us look at the example of an SR daughter card with NCP4318A as its SR controller in Figure 31.

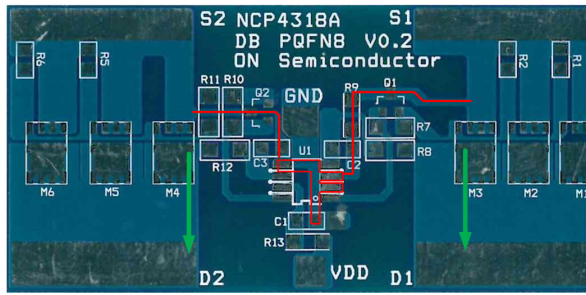
VD1 and VD2 pins for drain sensing are connected to drain pads at terminals that the flowing current, indicated as arrows, begins. It is not at any middle way of any possible current path. This connection avoids the noise generated by the changing current and the stray inductance on the PCB trace.

VS1 and VS2 pins are connected to SR MOSFET’s source terminals and GND pin separately, forming a Y connection. GND pin also connect to a VDD capacitor.

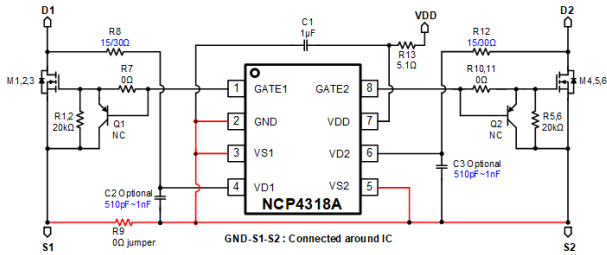
Gate drive current goes from VG1 and VG2 to the respective source terminal of the MOSFET and returns to GND through the VS1 and VS2 connections. Keeping the loop area of VG and VS connections small avoids the gate drive current loop to interfere other parts of the circuit.

For a higher wattage application, gate charge for MOSFETs in each switching cycle can be higher. Using external PNP transistors Q1 and Q2 to help the turning-off process can be considered. The PNP transistors reduce turning-off current-loop area and alleviate the power consumption on the SR controller during the turning-off process.

Since NCP4318 includes SR control logic and two gate drivers, the consideration of VDD-pin capacitor is like general gate driver and digital IC. That is, put high-frequency-decoupling capacitor, which has low equivalent series resistance such as ceramic capacitor, close to IC and connects to GND and VDD pins with short wide traces. The capacitance should be high enough to smooth out ripples on VDD voltage caused by gate driver operation. If the controller is placed far from the energy storage capacitor of its supply voltage source, consider adding additional energy storage capacitor in  $\mu\text{F}$  range close to IC. The bottom line is to avoid VDD voltage drop below  $V_{DD-OFF}$  during operation, even for just a blink of time.



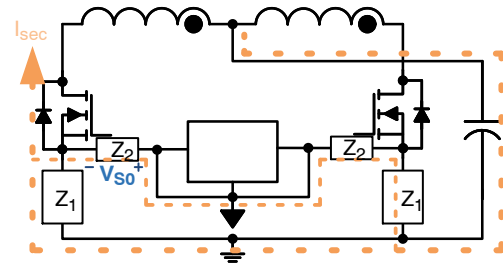
a) Printed Circuit Board



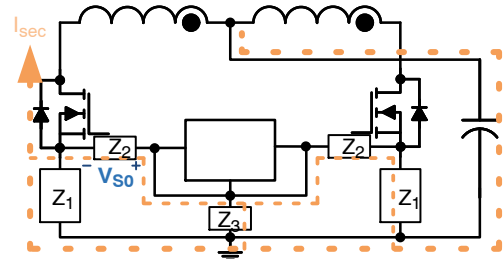
b) Schematic

Figure 31. NCP4318A SR Daughter Card

The GND pin of NCP4318 is connected to LLC converter's output ground terminal through the VS connections. It doesn't need to connect to output ground with other additional connection. Figure 32 shows the connection methods of VS pins, GND pin, and the output ground of the LLC converter. It is assumed that the layout is perfectly symmetrical.  $Z_1$  is the impedance between source pin of MOSFET and the output ground.  $Z_2$  is the impedance between VS pin and source pin of MOSFET. If there is additional connection between the GND pin and the output ground, the impedance is denoted as  $Z_3$ . Assume  $Z_1 \ll Z_2$  and  $Z_1 \ll Z_3$ , for  $Z_1$  being in the main current trace. The voltage difference  $V_{S0}$  between IC's VS pin and MOSFET's source pin can be derived as  $I_{sec} \cdot Z_1/2$  for Figure 32 (a) and  $I_{sec} \cdot Z_1 \cdot (Z_2 + Z_3)/(Z_2 + 2Z_3)$  for Figure 32 (b). The voltage difference  $V_{S0}$  in Figure 32 (a) is smaller between the two.



a) IC ground doesn't connect to output ground



b) IC ground connects to output ground

Figure 32. Ground Connection and Current Flow

### Enhancing Heat-Dissipation Capability of SOIC-8 EP Package

When NCP4318 needs to drive more paralleled SR MOSFETs in higher-output-current designs, power consumption on the gate driver of NCP4318 gets higher. Higher power consumption leads to higher junction temperature on the chip. NCP4318 has an SOIC-8 EP package variant in its lineup. This type of package provides exposed pad for direct thermal attachment, which makes lower the thermal impedance to the chip. To make good use of the package's characteristic, here we provide additional reminder on the PCB layout design.

The exposed pad can be connected to NCP4318's GND pin. When a PCB design still has some room to extend the copper area for GND, one way to enhance the thermal dissipation is to connect the GND copper area to the exposed

pad of the package. This way, the copper area is utilized as heat-sinking copper. Make sure that the exposed pad connects exactly to the copper area. More, note that the GND copper area is signal ground for NCP4318, not power ground for the output of the LLC converter.

If the PCB design is of multi-layer, you may consider drawing the ground copper area in the other layer of the same position as the IC and connecting the exposed pad to the ground copper area through thermal vias. The thermal vias can be spaced by 1 mm and have diameter of 0.3 mm. Figure 33 provides a design example.

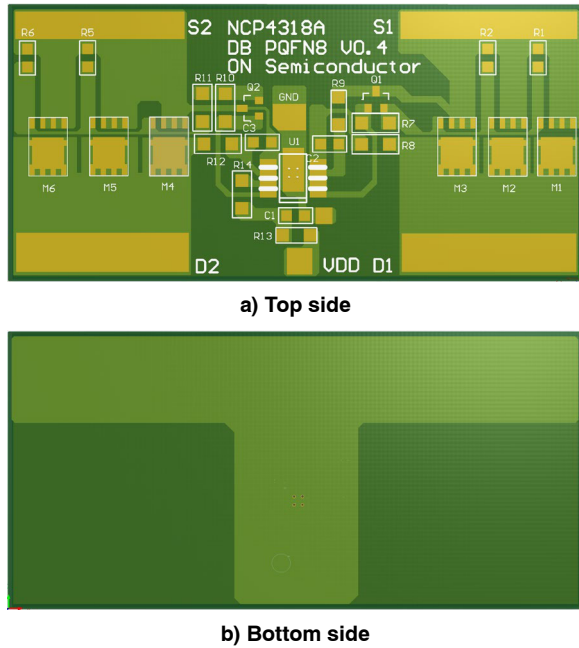


Figure 33. A PCB Layout with Thermal Vias for Package with Exposed Pad

**Situations That May Require Filtering Capacitors on the VD Pins**

The application schematic of Figure 1 mentioned that a capacitor may be added between VD and GND pins. The added capacitor on VD pin forms a low-pass filter with  $R_{OFFSET}$  on the VD signal. Since the low-pass filter will lead to delay on the VD signal, time constant of the low-pass filter had better not to be larger than a number around 30 ns for a proper SR operation. So, use capacitor not greater than 2.2 nF for 15  $\Omega$  of  $R_{OFFSET}$ , and not greater than 1 nF for 30  $\Omega$  of  $R_{OFFSET}$ . Too large of a time constant delays VD signal too much, making the judged dead time being effectively subtracted by the time constant, which in turn may make the gate be turned off too late. The capacitor is not required in general cases for NCP4318 to operate normally. However, there are some cases that adding capacitors on VD pins may help.

**Gate Turn-off Noise**

When the gate capacitance of the MOSFET is huge, amplitude of the MOSFET turn-off current tends to be

higher. The turn-off current of the gate driver can induce a voltage spike on the parasitic inductor in the current path, as described in Figure 34. If the spike is not higher than  $V_{TH-HIGH}$ , it doesn't cause problem. However, if the spike makes  $V_D$  exceeds  $V_{TH-HIGH}$  (0.85 V in typical), it may mis-trigger abnormal-VD protection, or at least interfere the dead-time judgement. In such a situation, adding VD pin capacitors may help to filter the spike. Or there are also orderable part numbers of NCP4318 that has a higher  $V_{TH-HIGH}$  of 1.5 V, which can be an alternative solution to this situation.

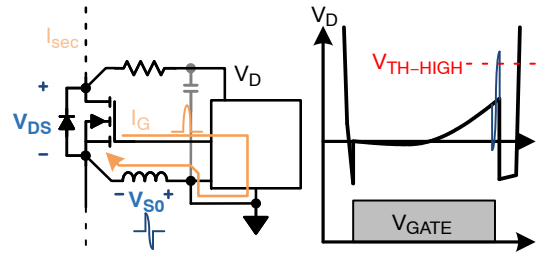


Figure 34. Effect of Gate Turn-off Current on  $V_{DS}$

**Misfiring on the SR Gate while the LLC Controller Shuts Down**

Another example that adding a capacitor between VD and GND may help happens at shutting down of the LLC controller. When the primary side LLC controller shuts down its operation, the resonant tank stops delivering energy to the secondary side. The remaining energy in  $L_m$  and  $C_{OSS}$  of the primary-side power switches makes a resonance. The voltage across  $L_m$  reflects to the secondary side, making a slower ringing on  $V_{DS}$  of the SR MOSFETs. At the same time, the remaining energy in  $C_{OSS}$  of SR MOSFETs and leakage inductance on the secondary side makes an additional resonance at a much higher frequency. Waveform of the two resonances is shown in Figure 35.

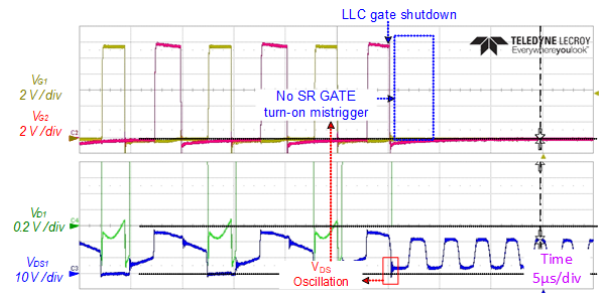


Figure 35. Added-up Resonances on  $V_{DS}$  at LLC Controller Shutting Down

When the two resonances are added up,  $V_{DS}$  on the SR MOSFET may satisfy  $V_{TH-ON}$  and NCP4318 generates gate turn-on signal, which results in an inversion current conducted in the SR MOSFET. The SR inversion current detection function or the primary shutdown protection can

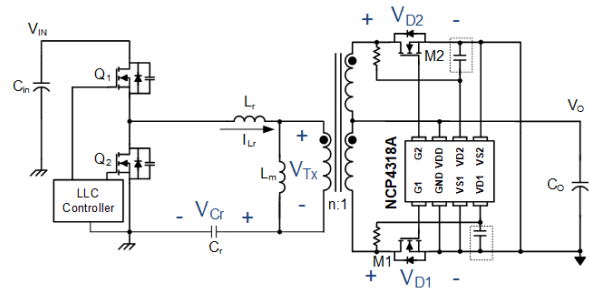
turn off the SR gate immediately; however, it is even better if the  $V_G$  signal isn't turned on by the  $V_{DS}$  ringing. In such a case, adding a R-C snubber to the SR MOSFET or adding a capacitor for the VD signal can absorb or filter out the  $V_{DS}$  ringing, avoiding the mis-triggered SR gate pulse. Note that the  $R_{OFFSET}$  and VD pin capacitor equivalently form an R-C snubber to the SR MOSFET.

*Mis-triggering of SR Gate During LLC Hold-up Time*

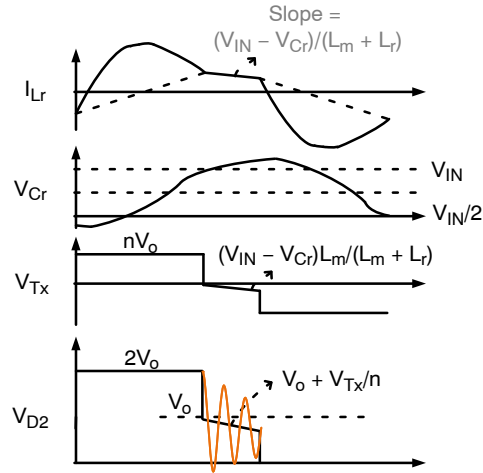
Yet another example that adding VD pin capacitors may help happens during hold-up time. The LLC converter tends to operate in below-resonant region during the hold-up time, so sub-resonance can be seen in each switching cycle. In addition, since the load during hold-up time is usually heavy, turning-on delay of NCP4318 tends to be the shorter  $t_{ON-DLY}$ , which means the SR gate turns on immediately when  $V_D < V_{TH-ON}$ . Furthermore, the  $V_{Cr}$  amplitude tends to be high during the hold-up time.

In some design examples, the amplitude of  $V_{Cr}$  may be increased larger than  $V_{IN}$ . Thus, when the current in M1 cuts off and VD shows sub-resonance, the amplitude of the sub-resonance becomes larger than  $2 \times V_O$ , as depicted in Figure 36. It makes  $V_{D2}$  dips to a negative value, which may satisfy the  $V_{TH-ON}$  criterion and mis-triggers turning-on of M2. Same phenomenon happens on M1 on the other half cycle.

In this case, a snubber on SR MOSFETs damps the sub-resonance and makes the amplitude of the sub-resonance reduce faster. Thus, adding snubber, or using VD pin capacitor to form an equivalent snubber with  $R_{OFFSET}$ , helps avoiding the mis-triggering of SR gate signals.



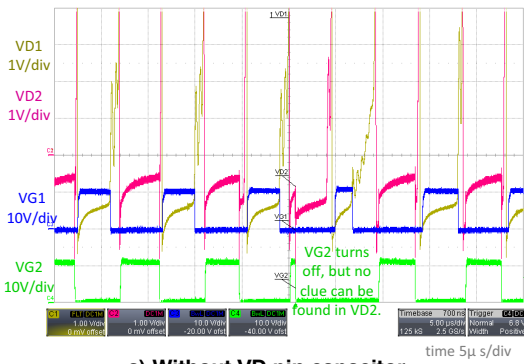
a) An LLC Converter



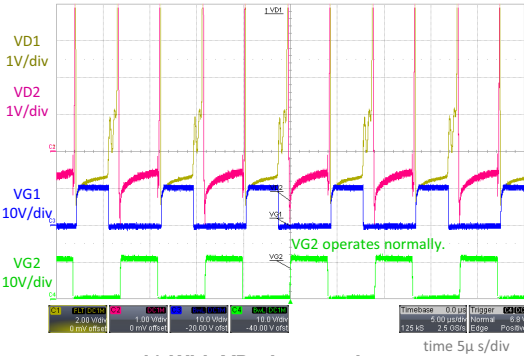
b) Sub-resonance that Causes Mis-trigger of SR Gate  
**Figure 36. Increased Sub-resonance Amplitude During Hold-up Time**

*SR Gate turns off by not-capturable noise*

It had been observed that SR gate may sometimes be turned off while no clue can be found on its respective VD signal. Possible reasons may include radiated noise on the board or noise that is beyond resolution of oscilloscope. In Figure 37 (a), when the VG2 turned off, VD2 didn't show a waveform that satisfied  $V_{TH-OFF}$  or SRCINV. Although the oscilloscope didn't capture the problem, it was found that the problem can be solved by adding a capacitor on the VD2 pin. If that happens in your design too, adding capacitor on VD pins can be worth trying.



a) Without VD pin capacitor



b) With VD pin capacitor

Figure 37. SR Gate is Turned off by Not-capturable Noise

*Common-mode Noise Affects Dead Time Regulation in Above-resonant Operation*

In some LLC converter designs, due to parasitic components, such as inter-winding capacitor in the transformer or stray inductance on the secondary side, a high-frequency noise is induced while the primary-side switches do switching transition. When the LLC converter operates in above-resonant region, the switching transition happens before SR current commutating. If the magnitude of the noise is considerable, such as in Figure 38, the induced noise will hinder the dead-time regulation of NCP4318 to operate properly. The dead time will not be able to stay in the range of  $t_{DEAD-LBAND} \sim t_{DEAD-HBAND}$  for the noise triggering turning-off of the SR gate signal.

If the noise frequency is as high as tens of MHz, adding filtering capacitor on VD pins to form a low-pass filter for the noise can be helpful to get rid of the noise. Even if the noise doesn't get filtered out completely, lowering

magnitude on the noise may make the dead-time regulation get back to proper operation.

When the dead time is found to be always longer than  $t_{DEAD-HBAND}$  in all load conditions, please give this  $V_{DS}$  noise a check.

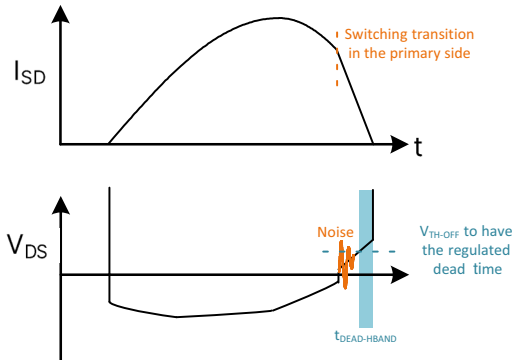


Figure 38. Induced Common-mode Noise on  $V_{DS}$  at Switching Transition of the Primary-side Switches

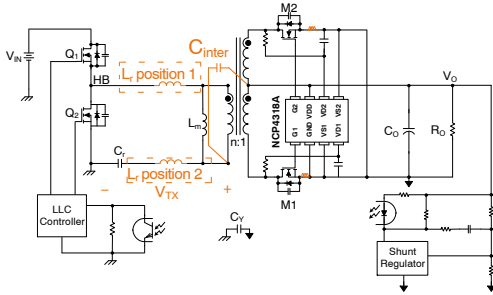
When  $L_T$  is not integrated into the transformer, the position of  $L_T$  matters in the generation of the common-mode noise. Consider two positions for  $L_T$  placement as in Figure 39 (a). For proper operation of the LLC converter, those two positions give no difference. However, when the inter-winding capacitor is considered, which is lumped as a  $C_{inter}$  in the figure, the two positions give different results for the common-mode noise.

The voltage on one side of the  $C_{inter}$  is notated as  $V_{TX}$ . As drawn in Figure 39 (b), the  $L_T$  position 1 makes  $V_{TX}$  equal to  $V_{Cr}$ , which changes gradually during the switching operation. Comparatively, when  $L_T$  is in position 2, the  $V_{TX}$  waveform shows sudden changes in switching transition of the primary side and current commutating of the secondary side.

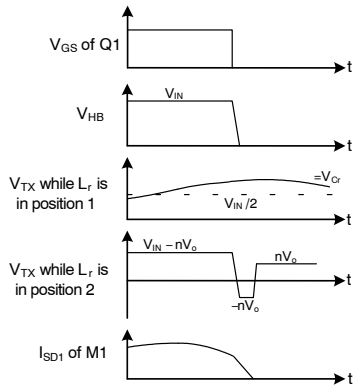
When  $V_{TX}$  shows fast transitions, a displacement current will be induced on the  $C_{inter}$ . The induced current flows through the secondary-side circuit and returns on the EMI-suppressing capacitor  $C_Y$ . The current flowing through the secondary-side circuit excites parasitic components to resonate, resulting in the noise shown in Figure 38.

So, when a design has a non-integrated  $L_T$ , the  $L_T$  had better be placed in the position 1, which induces less noise on the secondary-side circuit.

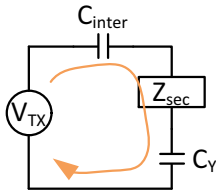
If the noise is found to be not manageable in some rare cases, the NCP4318 functional option of disabling dead-time regulation may be considered. However, solving the noise through circuit modification is encouraged.



(a) An LLC Converter



(b)  $V_{TX}$  at Switching Transition



$$I(s) \approx V_{TX}(s) \cdot (s \cdot C_{inter})$$

(c)  $V_{TX}$  Induces Displacement Current on the Inter-winding Capacitor

Figure 39. Inter-winding Capacitance and Placement of  $L_r$

### Conclusion

NCP4318 is an SR controller for LLC converters with center-tapped secondary-side configuration. With highly integrated functionalities, NCP4318 controls the SR power switches with very few additional circuit elements. NCP4318 delivers the driving pulses for SR power switches that maximize the efficiency of LLC converters. With sophisticated protections, NCP4318 responds to sudden changes in the operation of LLC converters with appropriate actions in the gate drive signals.

NCP4318 has several orderable part numbers (OPNs) that provides different function sets and parameter values. For different LLC converter designs, the required function sets and parameter values may vary. This application note is

meant to share the insights for selecting the appropriate OPN by explaining the functionalities in much detail. Some circuit design tips are provided to ease the difficulties that one might sometimes confront when designing LLC converters with NPC4318 for the SR control.

### References

- [1] NCP4318 Data Sheet  
<https://www.onsemi.com/pdf/datasheet/ncp4318-d.pdf>
- [2] LLC Resonant Converter Synchronous Rectification Design using FAN6248  
<https://www.onsemi.com/pub/collateral/and9618-d.pdf>



# AND90154/D

## REVISION HISTORY

Revision	Description of Changes	Date
6	Adding a section "Damping $V_{GATE}$ Ringing during GATE Turning-on" and one more paragraph to the existing section "PCB Layout Recommendation" section.	2/26/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

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