

MOSFET Selection for Reverse Polarity Protection

AND90146/D

OVERVIEW

When the vehicle’s battery is damaged and needs replacement the probability of connecting the new battery in reverse is high. Since many electronic control units (ECU) in the vehicle are connected to the vehicle’s battery, such an event could lead to numerous ECU failures. Additionally, automotive standards like ISO (International Organization for Standardization) defines the testing methods, voltage levels, limits for electromagnetic emission for electrical and electronic devices to ensure the safe and rugged operation of the system. One such standard related to reverse polarity protection (RPP) is ISO 7637–2:2011 which replicates the various voltage scenarios like in the real application and the system needs to withstand such voltages to showcase the robustness against failures. This made reverse polarity protection a crucial building block that is required by all automotive vehicle manufacturers for any battery connected ECU/system.

This application note will first address the ISO pulses that are commonly used to replicate the voltage transients that could appear in real applications. It will then give details about several protection techniques that could be used, before helping to guide the reader to select an external N–Channel MOSFET, that will provide RPP and help reduce the power losses of the system. Finally, a list of recommended N–Channel MOSFETs to be used along with an ideal diode controller, based on the battery current will be provided.

ISO PULSES

ISO 7637–2:2011 is an international standard which specifies test methods and procedures to ensure the compatibility to conducted electrical transients of equipment installed on passenger cars and commercial vehicles fitted with 12 V or 24 V electrical systems. Refer to ISO 7637–2:2011 for detailed information.

Under this standard there are several types of test pulses that are defined to test the device. Below are few of the test pulses.

- Pulse 1: Transients due to supply disconnection of inductive loads.
- Pulse 2a: Transients due to sudden interruption of currents in a device connected in parallel with the DUT (Device Under Test), due to the inductance of the wiring harness.
- Pulse 3a & 3b: Transients which occur as a result of switching processes. The characteristics of these transients are influenced by distributed capacitance and inductance of the wiring harness.

These test pulses come with different negative and positive voltage levels to stress the DUT to see if it can withstand. For example, Pulse 3b is shown in Figure 1 to give an idea about the type of pulses that are defined in the standard, each pulse will have its own parameters as in Table 1. Pulse 3b simulates the switching noise in the real application, such as relay and switch contact bouncing which can produce a short burst of high frequency pulses. [AND8228/D](#) talks in more details about voltage transients and testing methods.

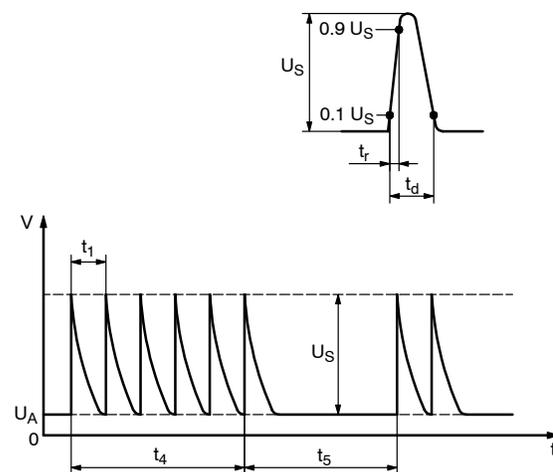


Figure 1. Test Pulse 3b

Table 1. PARAMETERS OF TEST PULSE 3b

Parameters	Nominal 12 V System	Nominal 24 V System
U_S	+75 V to +150 V	+150 V to +300 V
R_i	50 Ω	
t_d	150 ns \pm 45 ns	
t_r	5 ns \pm 1.5 ns	
t_1	100 μ s	
t_4	10 ms	
t_5	90 ms	

REVERSE POLARITY PROTECTION TECHNIQUES

In the following section the three most common techniques used for reverse polarity protection are discussed.

Diode

The simplest way to protect a system from a reverse battery is by using a diode. As shown in Figure 2, a diode will

only conduct current when the correct polarity is applied to its terminals (i.e., forward biased). The forward voltage drop, V_F for a standard diode is around 0.7 V, while for a Schottky diode it can be as low as 0.3 V. As a result, most applications use a Schottky diode, to reduce system losses.

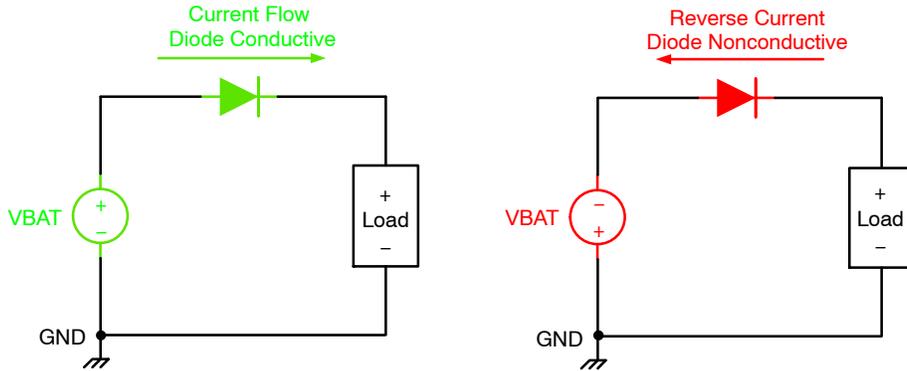


Figure 2. Reverse Polarity Protection using a Diode

Figure 3 shows the typical voltage drop of the [NRVBSS24NT3G Schottky diode](#). If the diode current (I_{DIODE}) increases from 0.5 A to 1.0 A (100% increase), V_F

increases from 0.35 V to 0.40 V (15% increase) at a junction temperature T_J of 25°C.

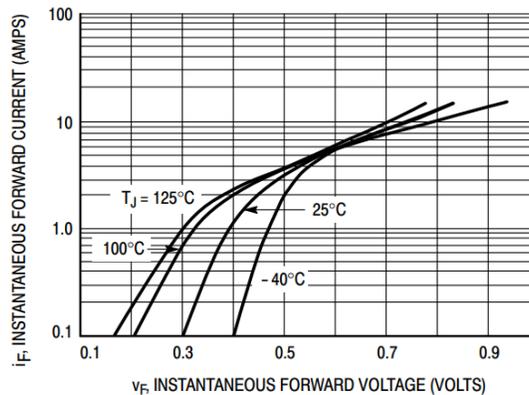


Figure 3. Typical Forward Voltage of NRVBSS24NT3G Schottky Diode

MOSFET

An alternative to a diode is a MOSFET. When a MOSFET is conductive, the voltage drop between the drain–source V_{DS} is dependent on the drain–source resistance $R_{DS,ON}$ and the drain–source current I_D : $V_{DS} = R_{DS,ON} * I_D$. Compared to a Schottky diode the voltage drop is generally much lower.

P–Channel MOSFET

As all MOSFETs, a P–Channel MOSFET has an intrinsic body diode between the source and the drain. When the

battery is properly connected, the intrinsic body diode is conductive till the MOSFET’s channel is turned ON. To turn ON a P–Channel MOSFET, the gate voltage needs to be lower than the source voltage by at least the threshold voltage V_T . When the battery is reversely connected, the body diode is reversed biased, gate and source have the same voltage thus turning OFF the P–Channel MOSFET. An additional Zener diode is used to clamp the gate of the P–Channel MOSFET and protect it in the case of a too high voltage.

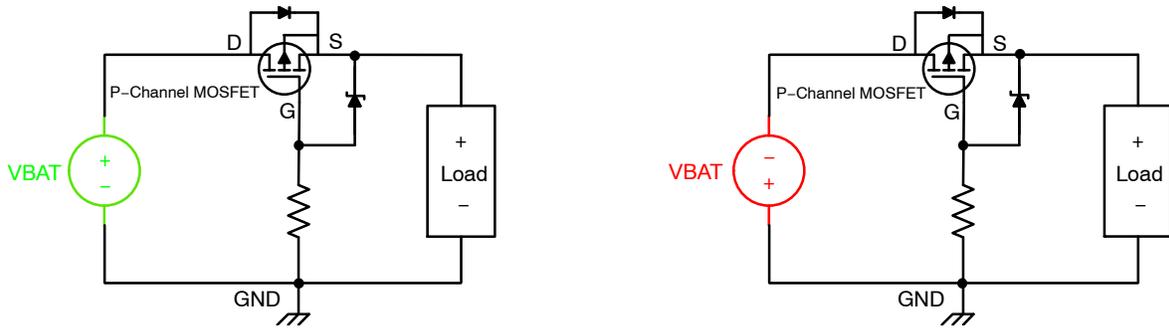


Figure 4. Reverse Polarity Protection using a P-Channel MOSFET

N-Channel MOSFET

It is also possible to use an N-Channel MOSFET for reverse polarity protection. When the battery is properly connected (source is connected to V_{BAT}), to turn ON the MOSFET, the gate-source voltage has to be higher than the threshold voltage ($V_{GS} > V_{TH}$). Given that the source is connected to V_{BAT} , the gate voltage needs to be higher than

V_{BAT} by at least V_T . Hence a dedicated driver is used to drive the gate voltage of the N-Channel MOSFET higher than the source voltage, thus turning ON the N-Channel MOSFET. When the battery is reverse connected, the body diode is reversed biased (anode voltage is lower than cathode voltage) and the driver is disabled (source and gate are shorted), turning the N-Channel MOSFET OFF.

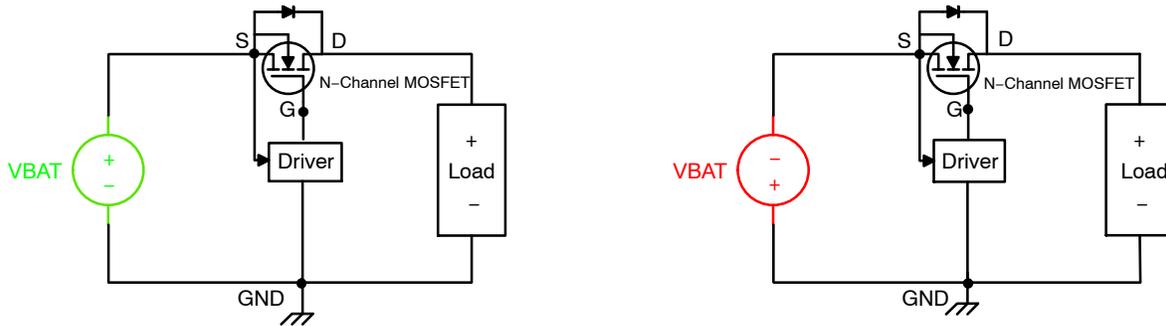


Figure 5. Reverse Polarity Protection using a N-Channel MOSFET

Comparison of Reverse Polarity Protection Techniques

Table 2 summarizes the advantages and disadvantages of the different reverse polarity protection techniques. It is worth mentioning that P-Channel MOSFET operation depends upon the mobility of holes, while an N-Channel MOSFET depends upon the mobility of electrons. Knowing that the mobility of holes is almost 2.5 times lower than the mobility of electrons, for the same drain current, a P-Channel MOSFET will have a bigger die size and, by implication, a higher cost compared to that of an N-Channel MOSFET to achieve the same on-resistance. This makes N-Channel MOSFETs preferable compared to P-Channel MOSFETs in such applications.

Table 2. COMPARISON BETWEEN DIFFERENT PROTECTION TECHNIQUES

	Advantages	Disadvantages
Schottky Diode	<ul style="list-style-type: none"> - Low cost - Simple 	<ul style="list-style-type: none"> - Higher power dissipation - Higher voltage drop
MOSFET	<ul style="list-style-type: none"> - Flexibility (various MOSFETs with various $R_{DS,ON}$) - Higher power dissipation - Lower operating voltage drop 	<ul style="list-style-type: none"> - High cost for low $R_{DS,ON}$ - Higher total solution cost (need of additional charge pump / controller) - Higher complexity (i.e., gate drive and protection)

MOSFET SELECTION

There are various parameters to consider when selecting an N-Channel MOSFET for reverse polarity protection.

- Maximum Breakdown Voltage of the MOSFET $V_{DS, MAX}$
 - ◆ For 12 V board net (vehicle) $V_{DS, MAX} = 40$ V is preferred
 - ◆ For 24 V board net (truck) $V_{DS, MAX} = 60$ V is preferred
- Maximum Operating Junction Temperature $T_{J, MAX}$
 - ◆ For vehicle and truck applications, 175°C is recommended given the harsh environment
- Gate Level
 - ◆ Logic Level is preferred over standard level since they have a lower $R_{DS, ON}$ for the same gate-source voltage V_{GS}
- Package
 - ◆ 3.30 × 3.30 mm (i.e. LPAK33/WDFN8/μ8FL) and 5.00 × 6.00 mm (i.e., SO8-FL/LPAK56) packages with exposed pad for optimized power dissipation are commonly used
- Total Gate Charge $Q_{G, TOT}$
 - ◆ Turning ON a MOSFET happens in 3 phases
 - When the gate voltage V_{GS} rises to the plateau voltage V_{GB} , charges are mainly used to charge the input capacitance C_{ISS} .
 - When V_{GS} is at the plateau voltage V_{GB} , charges are mainly used to charge the reverse transfer capacitance (gate-to-drain capacitance) C_{RSS} .
 - When V_{GS} rises from V_{GP} to driver supply voltage V_{GDR} , the charges are used to further enhance the channel.
 - ◆ Lower the $Q_{G, TOT}$, lesser the gate voltage and current needed to turn ON the MOSFET (i.e., faster turn ON) and vice versa
 - ◆ More information about MOSFET Gate-Charge could be found in the following **onsemi** application note.
 - <https://www.onsemi.com/pub/Collateral/AND9083-D.PDF>
- Drain-Source Resistance $R_{DS, ON}$
 - ◆ $R_{DS, ON}$ plays a role to limit the power dissipation in the device. The higher the $R_{DS, ON}$ for a given load current, the higher is the power dissipation. Higher losses lead to the increase in T_J of the MOSFET. Hence it is important to choose the right device with required $R_{DS, ON}$ to have optimal performance.
 - ◆ In the following sections, MOSFETs for thermal evaluation are chosen in such a way that their $R_{DS, ON}$ will keep power dissipation around 500 mW of losses.

NCV68061 IDEAL DIODE CONTROLLER

The combination of NCV68061 and an external N-Channel MOSFET replicates an ideal diode which acts like a perfect conductor when forward biased voltage (anode voltage is higher than cathode) is applied and like a perfect insulator when the reverse biased voltage (anode voltage is lower than cathode) is applied. The NCV68061 is a reverse polarity protection and ideal diode N-Channel MOSFET controller intended as a lower loss and lower forward voltage replacement for diodes.

The main function of the NCV68061 is to control the ON/OFF state of an external N-Channel MOSFET according to the source to drain differential voltage polarity. Depending on the drain pin connection the device can be configured in two different application modes. With the drain pin is connected to the load the application is in ideal diode mode, whereas with the drain pin connected to ground the NCV68061 is merely in reverse polarity protection mode. In both modes, the controller provides a typical gate voltage of 11.4 V to external N-Channel MOSFET. Hence in all the calculations of following sections, $R_{DS, ON} @ 10$ V V_{GS} has been used.

NCV68061 has undergone ISO 7637-2:2011 tests to demonstrate the robustness of the device to withstand voltage stress. The results are shown in the [NCV68061](#) datasheet.

Ideal Diode Application

Figure 6 shows how the NCV68061 is used in the ideal diode configuration. In this configuration, the input voltage is not allowed to discharge the bulk capacitance C_{bulk} . This configuration has two modes:

- Conduction Mode: Prior to entering the conduction mode, the source voltage is lower than the drain voltage, and both the charge pump and the N-Channel MOSFET are disabled. As the source voltage becomes greater than the drain voltage, the forward current flows through the body diode of the N-Channel MOSFET. Once this forward voltage drop exceeds the source to drain gate charge voltage threshold level (typ. 140 mV), the charge pump is turned ON and the N-Channel MOSFET becomes fully conductive.
- Reverse Current Blocking Mode: When the source voltage becomes less than the drain voltage, reverse current initially flows through the conductive channel of the N-Channel MOSFET. This current creates a voltage drop across the conductive channel of the N-Channel MOSFET which is proportional to its $R_{DS, ON}$. When this voltage drops below the source to drain gate discharge voltage threshold (typ. -10 mV), the charge pump is disabled, and the external N-Channel MOSFET is turned OFF by an internal P-Channel MOSFET of the controller.

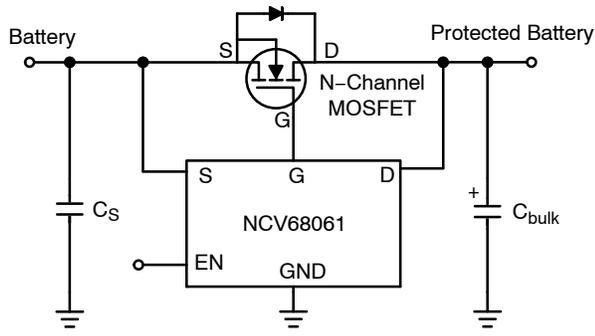


Figure 6. NCV68061 Ideal Diode Application

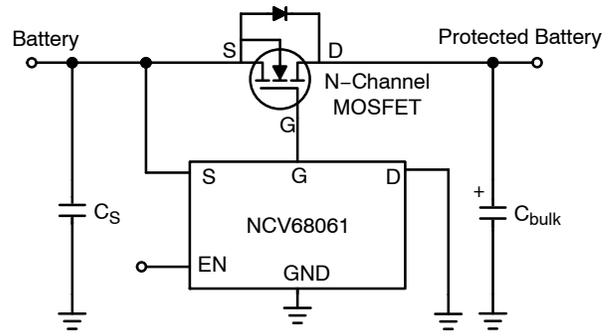


Figure 7. NCV68061 Reverse Polarity Protection Application

Reverse Polarity Protection

By connecting the drain pin to the GND potential, as shown in Figure 7, the NCV68061 does not allow a falling input voltage to discharge the output below GND potential but does allow the output to follow any positive input voltage above the under-voltage lockout (UVLO) threshold. This means that the bulk capacitance C_{bulk} will be discharged by a falling input voltage.

When the source voltage is above the UVLO threshold (typ. 3.3 V), the source/drain and UVLO comparators enable the charge pump to provide gate-source voltage to the external N-Channel MOSFET, which is fully conductive. When the source voltage is below the UVLO threshold (typ. 3.2 V), the charge pump and the N-Channel MOSFET are disabled, and any load current flows through the body diode of the N-Channel MOSFET.

TEST SETUP

A dedicated test board for NCV68061 is used to determine the power dissipation and thermal performance of the various MOSFETs in 3×3 and 5×6 packages with different $R_{DS,ON}$ to help to understand the MOSFET selection for the ideal diode controller considering various load currents.

Schematic

Figure 8 shows the schematic of the test board. It is designed in such a way that MOSFETs in SO-8FL/LFPAK4 and $\mu 8FL/LFPAK33$ can be tested. Each MOSFET circuit has a jumper to enable/disable the NCV68061 to make sure that only one controller is active at a time. A 3.3 V LDO NCV4294 is used to supply the enable pin EN of the controller. The controller will control the N-Channel MOSFET to act like an ideal diode and also to block reverse current.

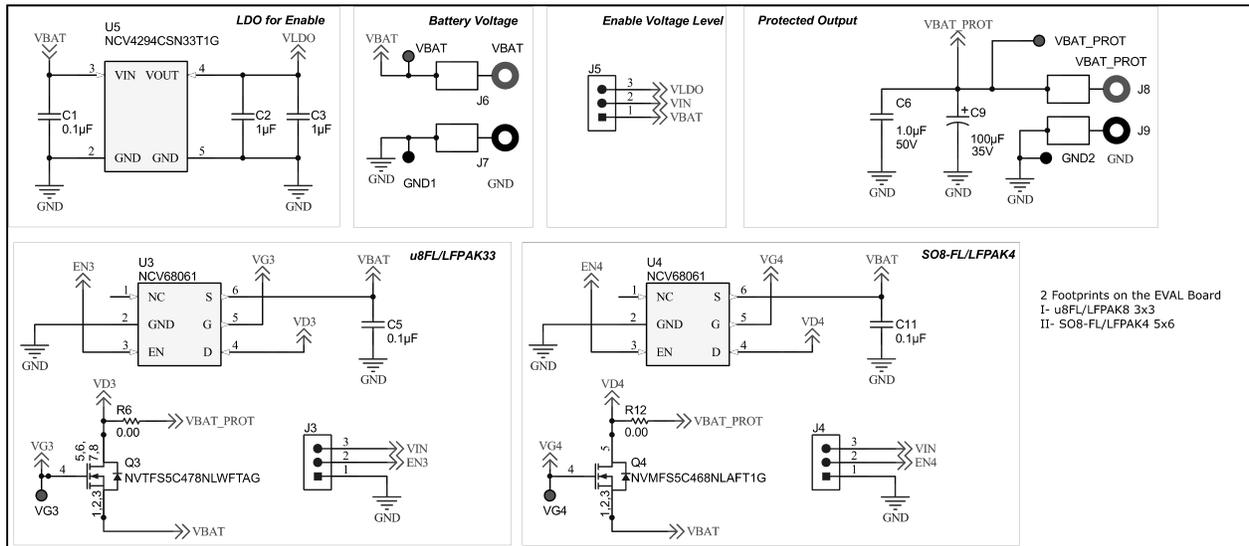


Figure 8. Schematic of NCV68061 Test Board

Layout

The board is a 4-layer printed circuit board (PCB). The input and output currents have been distributed across top, inner1 and inner2 layers. Distributing the current across

several layers helps to reduce the losses and to have better thermal performance of the board. Inner2 layer has traces for gate signals and for enable signal. Bottom layer is fully dedicated for the GND plane.

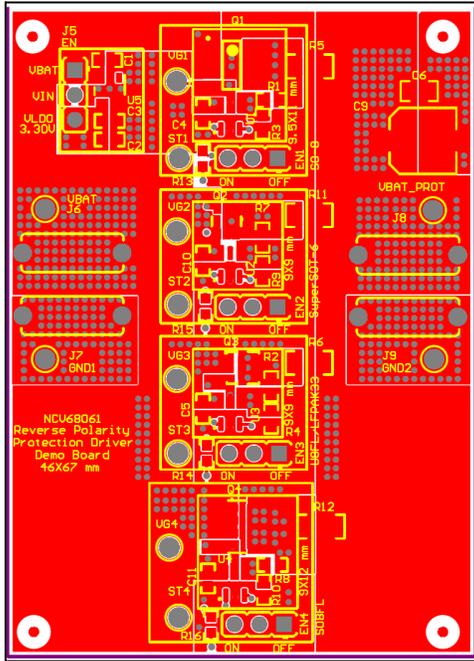


Figure 9. Top Layer

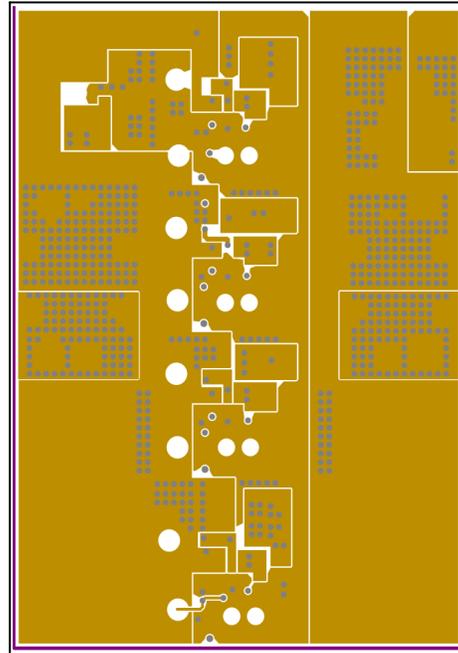


Figure 10. Inner1 Layer

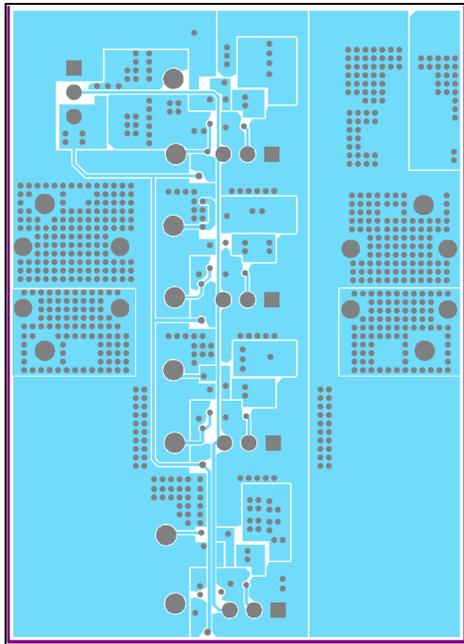


Figure 11. Inner2 Layer

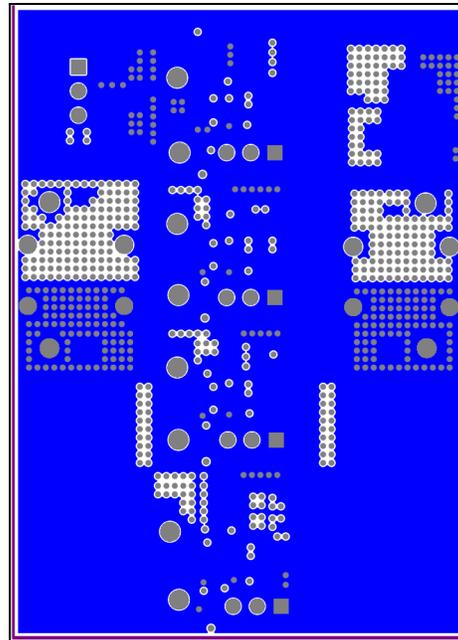


Figure 12. Bottom Layer

THERMAL MEASUREMENTS

Table 3. MOSFETS UNDER EVALUATION

Battery Current	Part Number	Package	Maximum $R_{DS,ON}$ @ 10 V V_{GS} (m Ω)	Maximum Losses P_D (mW)	$R_{\theta JA}$ ($^{\circ}C/W$)	T_{CASE} ($^{\circ}C$)
6 A	NVTFS5C478NLWFTAG	μ 8FL	14.0	504.0	51.0	47.3
	NVMFS5C468NLAFT1G	SO-8FL	10.3	370.8	43.0	40.1
8 A	NVTFS5C466NLWFTAG	μ 8FL	7.3	467.2	48.0	47.4
	NVMFS5C466NLWFT1G	SO-8FL	7.3	467.2	43.0	45.3
10 A	NVTYS005N04CLTWG	LFLPAK8	4.8	480.0	47.7	52.8
	NVMYS4D6N04CLTWG	LFLPAK4	4.5	450.0	40.0	47.5

Table 3 shows the N-Channel MOSFETs used for thermal evaluation. MOSFETs with various $R_{DS,ON}$ are chosen to limit the power dissipation to be around 500 mW. Measurements of the MOSFETs top case temperature are made at 24 $^{\circ}C$ ambient temperature to evaluate the thermal

performance of the MOSFETs with different output currents (6 A, 8 A and 10 A). MOSFETs in SO-8FL/LFLPAK4 (5 \times 6) and μ 8FL/LFLPAK8 (3 \times 3) are used for evaluation. Two measurements are made for each load current, one with 5 \times 6 and another with 3 \times 3 package.

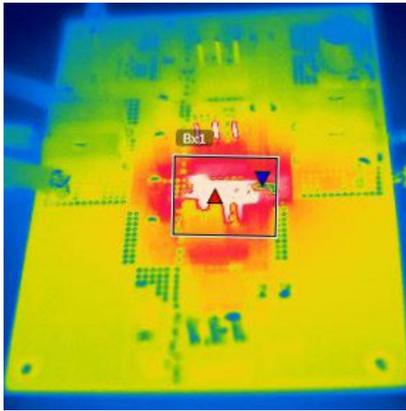


Figure 13. 6 A with μ 8FL

Part Number	NVTFS5C478NLWFTAG
Max. $R_{DS(ON)}$ @ 10 V V_{GS}	14.0 m Ω
Max. Temperature	47.3 $^{\circ}C$

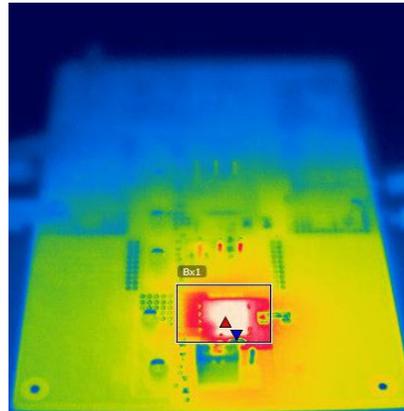


Figure 14. 6 A with SO-8FL

Part Number	NVMFS5C468NLAFT1G
Max. $R_{DS(ON)}$ @ 10 V V_{GS}	10.3 m Ω
Max. Temperature	40.1 $^{\circ}C$

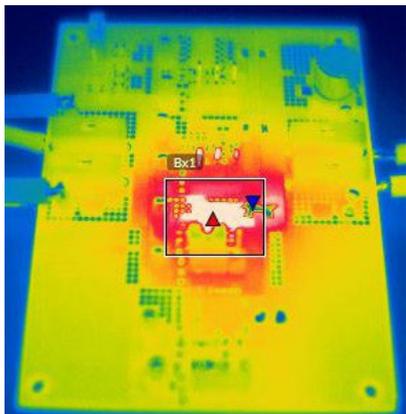


Figure 15. 8 A with μ 8FL

Part Number	NVTFS5C466NLWFTAG
Max. $R_{DS(ON)}$ @ 10 V V_{GS}	7.3 m Ω
Max. Temperature	47.4 $^{\circ}C$

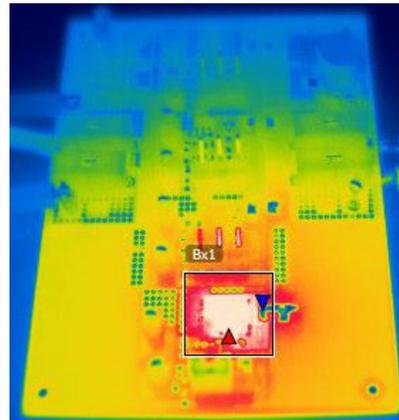


Figure 16. 8 A with SO-8FL

Part Number	NVMFS5C466NLWFT1G
Max. $R_{DS(ON)}$ @ 10 V V_{GS}	7.3 m Ω
Max. Temperature	45.3 $^{\circ}C$

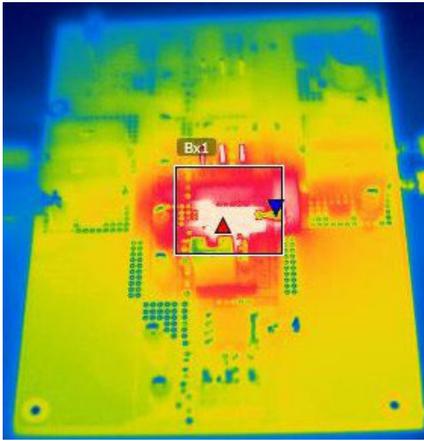


Figure 17. 10 A with LFPAK8

Part Number	NVTYS005N04CLTWG
Max. $R_{DS(ON)}$ @ 10 V V_{GS}	4.8 m Ω
Max. Temperature	52.8°C

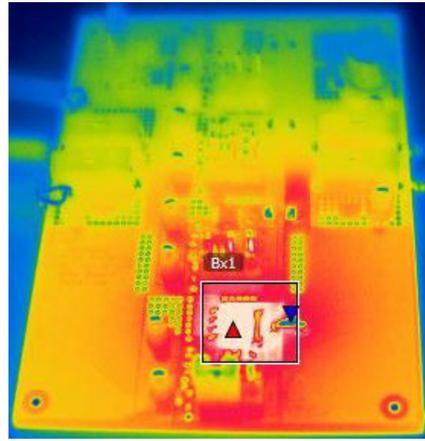


Figure 18. 10 A with LFPAK4

Part Number	NVMYS4D6N04CLTWG
Max. $R_{DS(ON)}$ @ 10 V V_{GS}	4.5 m Ω
Max. Temperature	45.3°C

With the measured top case temperature from thermal measurements and calculated power dissipation, the junction temperature T_J can be calculated using equation 1.

$$T_J = T_{CASE} + P_D \times R_{\theta JT} \quad (\text{eq. 1})$$

- T_J = Junction temperature of the MOSFET
- T_{CASE} = Temperature of the package on top measured by the thermal camera
- P_D = Power dissipation of the MOSFET
- $R_{\theta JT}$ = Thermal resistance between top case and junction of the MOSFET

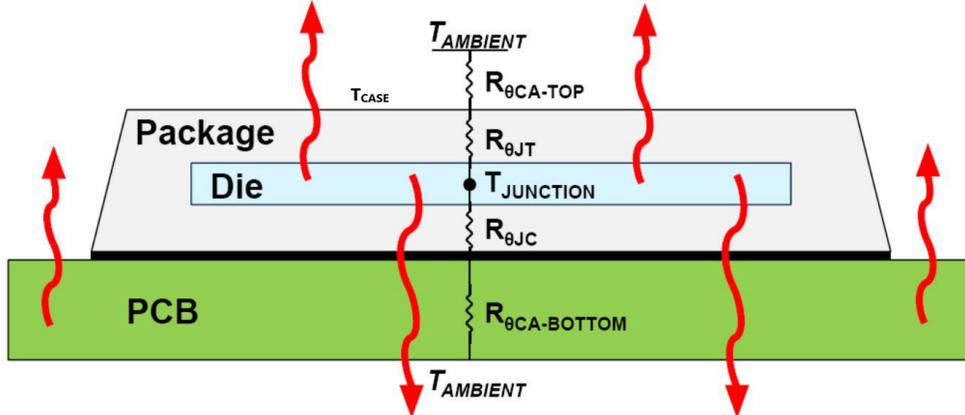


Figure 19. Equivalent Thermal Resistance of the MOSFET

The value of $R_{\theta JT}$ is not fixed, it depends on thermal boundary conditions such as PCB layout, cooling system of the MOSFET (like exposed pad) and other parameters, therefore it is not provided in the datasheet. $R_{\theta JT}$ is a small number with $< 1^\circ\text{C}/\text{W}$, as most of the heat will flow from junction to the PCB via the exposed pad on the bottom side of the package. Therefore, not much heat flows from the

junction to the top of the MOSFET and one can assume that the temperature difference between T_J and T_{CASE} is not significant. For the sake of the application note, the assumption is that $R_{\theta JT}$ is $1^\circ\text{C}/\text{W}$ to determine T_J .

NOTE: $1^\circ\text{C}/\text{W}$ is a very conservative assumption for 3×3 and 5×6 packages. Other packages will have a different thermal resistance.

Estimation of the Junction Temperature T_J

In the following section, the measured T_{CASE} and actual power dissipation in the MOSFET are used to calculate T_J . In the next step a theoretical calculation based on specifications of the datasheets is done and the result is compared to the calculations made using measured data to see if both theoretical and practical calculations of T_J are matching. All calculations consider MOSFET NVTFS5C478NLWFTAG in $\mu 8FL$ (3×3) package.

Estimation for T_J Using Measured T_{CASE}

The below calculations are done to estimate T_J using values obtained from measurements.

- Load current $I_{LOAD} = I_D = 6.0$ A
- Input voltage $V_{in} = 12.0$ V
- Temperature of top case $T_{CASE} = 47.3^\circ C$ (obtained from the thermal measurement)
- Max. on-resistance $R_{DS, ON} @ 10.0$ V $V_{GS} = 14.0$ m Ω
- $R_{\theta JT} = 1.0^\circ C/W$ (assumption for 3×3 and 5×6 packages)

$$P_D = I_D^2 \times R_{DS, ON}$$

$$P_D = (6.0 A)^2 \times 14.0 m\Omega = 504.0 mW \quad (eq. 2)$$

Using Equation 1,

$$T_J = 47.3^\circ C + (504.0 mW \times 1.0^\circ C/W) = 47.8^\circ C$$

Theoretical Calculation for T_J

Theoretical calculations based on specification of the datasheet are used to determine T_J . Assuming losses of 500 mW, the equation 3 is used to determine T_J of the device.

$$P_D = \frac{T_J - T_A}{R_{\theta JA}} \quad (eq. 3)$$

- Junction temperature of the MOSFET T_J
- Ambient temperature at which the MOSFET will be operated $T_A = 24.0^\circ C$
- Power dissipation of the MOSFET $P_D = 500.0$ mW
- Thermal resistance between junction and ambient of the MOSFET $R_{\theta JA} = 51.0^\circ C/W$ (value from the datasheet)

$$T_J = P_D \times R_{\theta JA} + T_A$$

$$= 500.0 mW \times 51.0^\circ C/W + 24.0^\circ C = 49.5^\circ C \quad (eq. 4)$$

This gives 125.5 $^\circ C$ headroom for $T_{J,MAX}$ of 175.0 $^\circ C$ for [NVTFS5C478NLWFTAG](#).

The difference between estimated and theoretically calculated T_J 's is minor at 1.7 $^\circ C$ (49.5 $^\circ C$ vs. 47.8 $^\circ C$). In Table 4, as shown in the above calculations, theoretically calculated T_J and measured T_{CASE} , $R_{\theta JT}$ and P_D are used to estimate T_J for various loads and packages.

Table 4. CALCULATED T_J OF THE PROPOSED MOSFETS VS. LOAD CURRENT

Battery Current	Part Number	Package	Maximum $R_{DS, ON} @ 10$ V V_{GS} (m Ω)	Maximum Losses P_D (mW)	$R_{\theta JA}$ ($^\circ C/W$)	Measured T_{CASE} ($^\circ C$)	T_J ($^\circ C$)			Estimated T_J Headroom from Maximum 175 $^\circ C$ Based on Measurement ($^\circ C$)
							Estimated @ 24 $^\circ C$ Ambient Based on Measurement	Calculated Theoretical Value	ΔT_J Between Theoretical and Scaled Up Value	
6 A	NVTFS5C478NLWFTAG	$\mu 8FL$	14.0	504.0	51.0	47.3	47.8	49.5	-1.7	127.2
	NVMFS5C468NLAFT1G	SO-8FL	10.3	370.8	43.0	40.1	40.4	45.5	-5.1	134.6
8 A	NVTFS5C466NLWFTAG	$\mu 8FL$	7.3	467.2	48.0	47.4	47.8	48.0	+0.2	127.2
	NVMFS5C466NLWFT1G	SO-8FL	7.3	467.2	43.0	45.3	45.7	45.5	+0.2	129.3
10 A	NVTYS005N04CLTWG	LFPK8	4.8	480.0	47.7	52.8	53.2	47.8	+5.4	121.8
	NVMYS4D6N04CLTWG	LFPK4	4.5	450.0	40.0	47.5	47.9	44.0	+3.9	127.1

- At 6 A load current there is approximately 5.8 % higher head room for T_J with 5×6 than 3×3 package.
- At 8 A load, approximately 1.6 % higher head room with 5×6 than 3×3 . Both the devices are having the same die in different packages, therefore there is not much difference between T_J 's is seen.
- At 10 A, approximately 4.3 % higher head room with 5×6 than with 3×3 .
- Likewise, the difference in theoretical and estimated T_J is not significant except around 5.4 $^\circ C$ difference for one of the 10 A MOSFETs. This shows that the $R_{\theta JA}$ in the datasheet is reliable for this specific test setup.
- Measurement of $R_{\theta JA}$ in the datasheet using 2 oz. copper pad with larger area board seems unrealistic from real application point of view but looking at the minor difference in T_J as estimated above shows that $R_{\theta JA}$ matched quite well with 4-layer test board optimized for thermal dissipation.
- The results show that due to the larger package (5×6) the heat is getting dissipated efficiently and being distributed across the whole device hence there is better head room. Larger packaged devices are suitable for higher load current application from thermal point of view as well as for applications with higher ambient temperature.

Estimation of the Maximum Ambient Temperature T_A

The previous calculations show that $R_{\theta JA}$ of the datasheet matches quite well with the NCV68061 test board. Therefore, the maximum ambient temperature above which the MOSFET cannot be operated can be calculated.

Figure 20 shows the variation of $R_{DS, ON}$ in relation to T_J for NVTFS5C478NLWFTAG. At 175°C junction temperature, the maximum $R_{DS, ON}$ is around 1.85 times higher compared to 25°C junction temperature. This results in a maximum $R_{DS, ON}$ of $1.85 \times 14 \text{ m}\Omega = \sim 25.9 \text{ m}\Omega$.

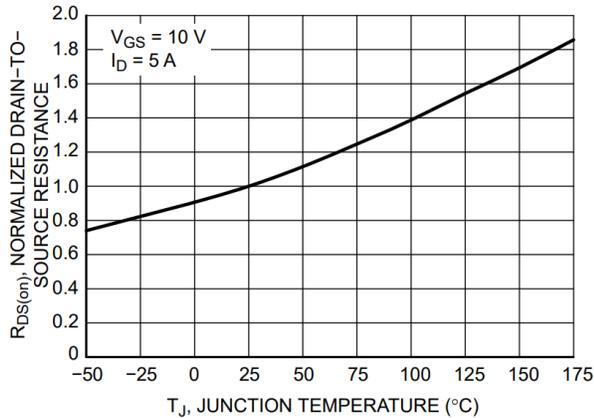


Figure 20. NVTFS5C478NLWFTAG On-Resistance Variation with Temperature

The power dissipation at 175°C junction temperature and 6 A load current is as follows:

$$P_D = (6.0 \text{ A})^2 \times 25.9 \text{ m}\Omega = 932.4 \text{ mW}$$

With $R_{\theta JA} = 51.0^\circ\text{C/W}$, the temperature difference between junction and ambient can be calculated:

$$\text{Temperature difference } \Delta T = 51.0^\circ\text{C/W} \times 932.4 \text{ mW} = 47.5^\circ\text{C}$$

$$\text{Maximum } T_A = T_J - \Delta T$$

$$\text{Maximum } T_A = 175.0^\circ\text{C} - 47.5^\circ\text{C} = 127.5^\circ\text{C}$$

(eq. 5)

From the above example, the MOSFET can be operated at maximum ambient temperature of 127.5°C. If the ambient temperature goes above the calculated value, then it would mean that the T_J has reached over 175°C.

The silicon of the MOSFET itself can be operated at above 175°C, but due to the limitation of package mold compound and to ensure reliability over long-term operation, the MOSFET datasheet states that maximum T_J to be 175°C. Temperature above maximum T_J would lead to unguaranteed behavior of the device, and it also means that device is operating out of specification.

Table 5 shows the estimated maximum ambient temperature for various MOSFETS, considering different load currents and a junction temperature of 175°C.

Table 5. ESTIMATED MAXIMUM T_{AMB}

Battery Current	Part Number	Package	Maximum $R_{DS, ON}$ @ 10 V V_{GS} @ 175°C T_J (m Ω)	Maximum Losses P_D (mW)	$R_{\theta JA}$ (°C/W)	Estimated Maximum T_{AMB} (°C)
6 A	NVTFS5C478NLWFTAG	μ 8FL	25.9	932.4	51.0	127.5
	NVMFS5C468NLAFT1G	SO-8FL	19.6	705.6	43.0	144.6
8 A	NVTFS5C466NLWFTAG	μ 8FL	14.4	921.6	48.0	130.7
	NVMFS5C466NLWFT1G	SO-8FL	13.2	844.8	43.0	138.6
10 A	NVTYS005N04CLTWG	LFLPAK8	8.8	880.0	47.7	133.0
	NVMYS4D6N04CLTWG	LFLPAK4	8.3	830.0	40.0	141.8

CONCLUSION

Reverse polarity protection circuits are one of the core building blocks of any ECU in a vehicle. In this application note several reverse polarity protection techniques are discussed including diodes, P-Channel MOSFET and N-Channel MOSFET. A comparison between all the techniques is presented highlighting advantages and disadvantages of each technique. Moreover, a MOSFET selection guide is given to support the MOSFET selection process, including a list of recommended devices. Thermal measurements with load currents from 6 A to 10 A show that 5 × 6 packages perform well from thermal point of view, due to the larger package and bigger die, $R_{DS, ON}$ will be reduced and power losses are lesser than 3 × 3 package. Additionally,

a larger die helps to dissipate the heat better than with a smaller die. With that said, table 3 shows that the difference in margin for maximum T_J between 5 × 6 and 3 × 3 is not significant. Depending upon the application needs and cooling system used either 5 × 6 or 3 × 3 packaged MOSFETs can be used.

Without significant difference between the theoretically calculated and practically estimated junction temperature T_J , $R_{\theta JA}$ given in the datasheet is a realistic value to perform thermal analysis in the real applications. $R_{\theta JA}$ helps to calculate the maximum ambient temperature at which the MOSFET can be operated using the calculations shown in the document earlier.

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