

FXMA2102 I²C Translator

AN-9718/D

Introduction

The FXMA2102 is a high-performance voltage-level translator, or level shifter, specifically designed for I²C and SMBUS open-drain applications. It features auto-direction and can translate either side (A or B) from 1.65 V to 5.5 V.

The FXMA2102 has open-drain I/Os and requires external pull-up resistors on the four data I/O pins, as shown in Figure 1. If a pair of data I/O pins (A_N/B_N) is not used, both pins should be tied to GND (or both to V_{CC}). In this case, pull-down or pull-up resistors are not required. The recommended values for the pull-up resistors (R_{PU}) are 1 kΩ to 10 kΩ. However, depending on the total bus capacitance, the pull-up resistor value can vary to meet the maximum I²C edge rate per the I²C specification (UM10204 rev. 03, June 19, 2007). For example, the maximum rise time (30% – 70%) during fast mode (400 kbit/s) is 300 ns. So, if bus capacitance is approaching the maximum 400 pF, lower the R_{PU} value to keep the rise time below 300 ns (Fast Mode). Section 7.1 of the I²C specification provides an excellent guideline for pull-up resistor sizing.

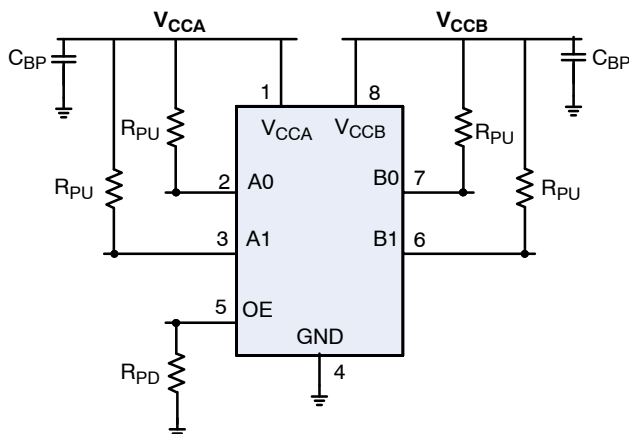


Figure 1. Application Circuit

Theory of Operation

The FXMA2102 is designed for high-performance level shifting and buffer/repeating in an I²C application. As seen in Figure 2, each bi-directional channel contains two series N-passgates and two dynamic drivers. This hybrid architecture is highly beneficial in an I²C application where auto-direction is a necessity.

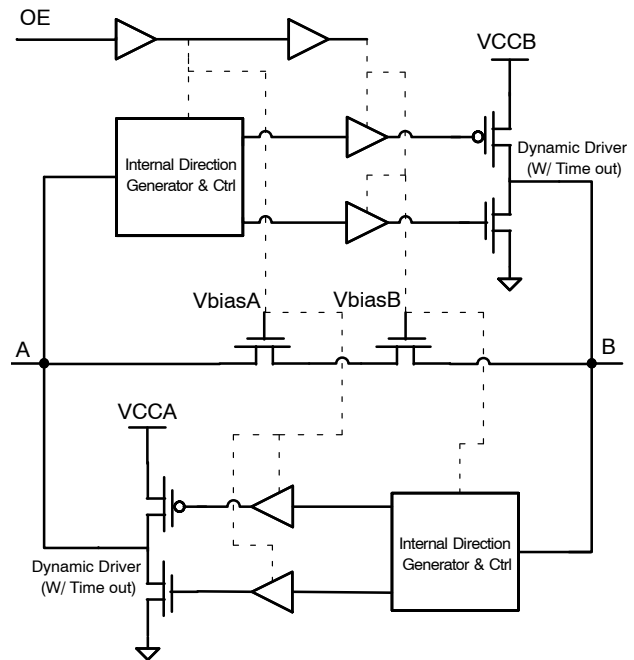


Figure 2. FXMA2102 Architecture

For example, during these three I²C protocol events:

- Clock stretching
- Slave acknowledgement: the slave's ACK bit (9th bit = 0) following a master's write bit (8th bit = 0)
- Clock synchronization and multi-master arbitration

The bus direction needs to change from master-to-slave to slave-to-master without the occurrence of an edge. If there is an I²C translator between the master and slave in these examples, the I²C translator must change direction when both A and B ports are LOW. The N-passgates can accomplish this efficiently because, when both A and B ports are LOW, the N-passgates act as a low-resistive short between the two (A and B) ports.

Due to I²C's open-drain topology, I²C masters and slaves are not push/pull drivers. Logic LOWs are pulled down (Isink), while logic HIGHs are "let go" (tri-state). For example, when the master lets go of SCL (SCL always comes from the master), the rise time of SCL is largely determined by the RC time constant where R = R_{PU} and C = the bus capacitance. If the FXMA2102 is attached

to the master in this example, say on the A port, and there is a slave on the B port, the N-passgates act as a low-resistive short between both ports until either of the port's $V_{CC}/2$ thresholds are reached. After the RC time constant has reached the $V_{CC}/2$ threshold of either port, the port's edge detector triggers both dynamic drivers to drive their respective ports in the LOW-to-HIGH (LH) direction, accelerating the rising edge. The resulting rise time resembles the scope shot of Figure 3. Effectively, there are two distinct slew rates to the rise time. The first slew rate (slower) is the RC time constant of the bus. The second slew rate (much faster) is the dynamic driver accelerating the edge.

If both the A and B ports of the translator are HIGH, a high-impedance path exists between the A and B ports. This is because both the N-passgates are turned off. If a master or slave device pulls SCL or SDA LOW, that device's driver pulls down (I_{sink}) SCL or SDA until the edge reaches the A or B port $V_{CC}/2$ threshold. When either the A or B port threshold is reached, the port's edge detector triggers both dynamic drivers to drive their respective ports in the HIGH-to-LOW (HL) direction, accelerating the falling edge.

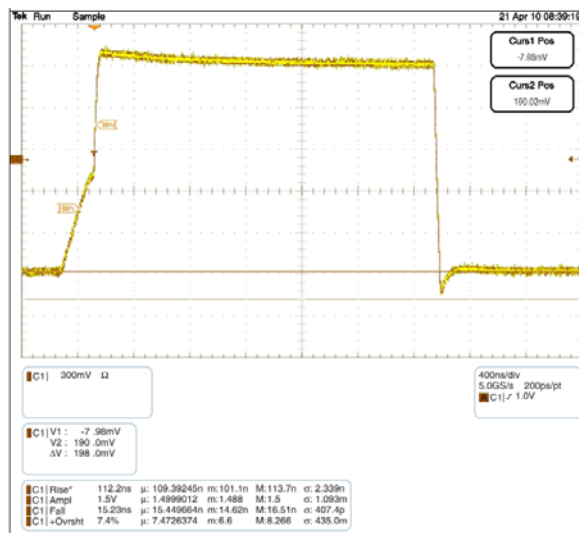


Figure 3. Waveform C: 600 pF, $R_{PU} = 2.2 \text{ k}\Omega$

Clock Stretching

Clock stretching allows a slave to hold SCL LOW, forcing the master to wait until the slave releases SCL. According to the I²C specification, there is not a maximum time limit for how long SCL can be held LOW by a slave; however, most

masters provide a time-out algorithm during clock stretching so the I²C bus does not hang.

Clock stretching occurs in many smart-phone applications. For example, there may be an I²C master host processor that has requested the current GPS coordinates from a GPS slave. Meanwhile, the GPS device may have stored the last GPS coordinates in an internal register from a previous master request. The master does not want the previously stored GPS coordinates. The master wants real-time GPS coordinates. This means that the GPS slave device must produce the new coordinates. This effort may take milliseconds. Therefore, the GPS slave must force the master to wait until it is ready to service the request for new GPS coordinates.

The interesting aspect of clock stretching for an I²C translator application configuration like Figure 4 is that the translator's auto-direction circuitry must change direction when both sides of SCL are LOW. The FXMA2102 tested 100% compliant during I²C clock stretching.

Multi-Master

The I²C specification also describes protocol timing requirements for "clock synchronization and arbitration" when multiple I²C masters attempt to transmit on an idle I²C bus at the same time. The FXMA2102 has been tested and verified in a multi-master application.

Buffer / Repeater Performance

The FXMA2102 dynamic drivers have current sourcing capability and can drive a 400 pF capacitive bus. This is beneficial when an I²C buffer/repeater is required. The I²C specification stipulates a maximum bus capacitance of 400 pF. If an I²C segment exceeds 400 pF, an I²C buffer/repeater is required to split the segment into two segments, each of which is less than 400 pF. Figure 3 is a scope shot of an FXMA2102 driving a lumped load of 600 pF. Notice the (30% - 70%) rise time is only 112 ns ($R_{PU} = 2.2 \text{ k}\Omega$). This is well below the maximum rise time of 300 ns. So, not only does the FXMA2102 drive 400 pF, but it also provides headroom below the I²C specification maximum rise time of 300 ns.

V_{OL} vs. V_{IL} & I_{OL}

The I²C specification mandates a maximum V_{IL} (assuming a minimum I_{OL} of 3 mA) of $V_{CC} \cdot 0.3$ and a maximum V_{OL} of 0.4 V. If, for example (see Figure 4), there is a master on the A port of an I²C translator with a V_{CC} of 1.65 V and a slave on the I²C translator B port with a V_{CC} of 3.3 V, the maximum V_{IL} of the master is $(1.65 \text{ V} \times 0.3)$ 495 mV.

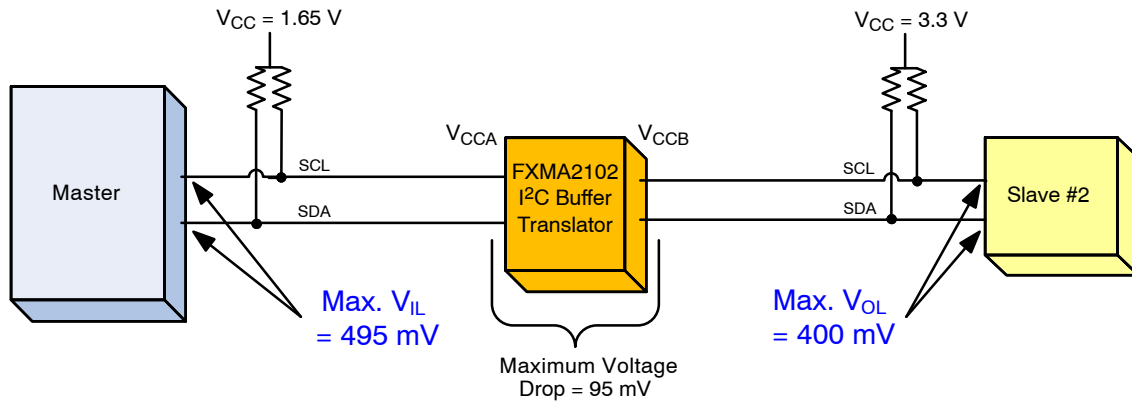


Figure 4. Clock Stretching

The slave in the Figure 4 example could legally transmit a valid logic LOW of 0.4 V to the master. If the I²C translator’s channel resistance is too high, the voltage drop across the translator could present a V_{IL} to master > 495 mV. To complicate matters, the I²C specification states that 6 mA of I_{OL} is recommended for bus capacitances approaching 400 pF. More I_{OL} increases the voltage drop across the I²C translator. The I²C application benefits when I²C translators exhibit low V_{OL} performance. Figure 5 depicts the typical FXMA2102 V_{OL} performance, given a 0.4 V V_{IL}.

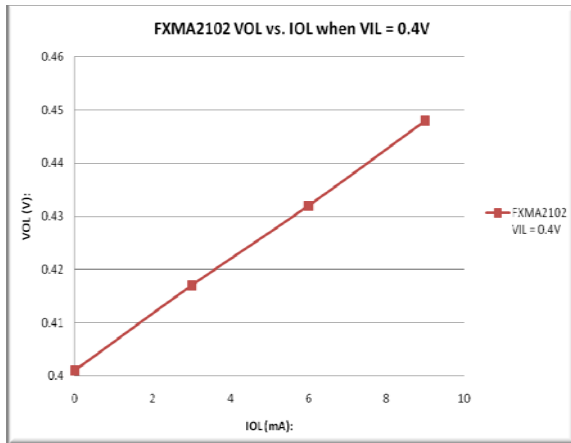


Figure 5. V_{OL} vs. I_{OL}

Bus Clear

The I²C specification defines the minimum SCL frequency of 0 Hz. Therefore, the SCL signal can legally be held LOW forever. However, this condition shuts down the I²C bus. The I²C specification refers to this condition as “Bus Clear.” In Figure 6, if slave #2 holds down SCL forever, the master and slave #1 are not able to communicate because the FXMA2102 passes the SCL stuck-LOW condition from slave 2 to slave 1 as well as the master. However, if the OE pin of the FXMA2102 is pulled LOW (disabled), both ports (A and B) of are in tri-state. This results in the FXMA2102 isolating slave #2 from the master and slave #1, allowing full communication between master and slave #1.

Either V_{CC} to GND

If, in an application such as Figure 6, slave #2 is a camera that is suddenly removed from the I²C bus, resulting in V_{CCB} transitioning from a valid V_{CC} (1.65 V – 5.5 V) to 0 V, the FXMA2102 automatically forces SCL and SDA on both its A and B ports into tri-state. Once V_{CCB} reaches 0 V, there is full I²C communication between the master and slave #1.

I²C Bus Isolation

FXMA2102 supports I²C bus isolation for these conditions:

- Bus isolation in the event of bus clear.
- Bus isolation in the event of either V_{CC} going to ground.

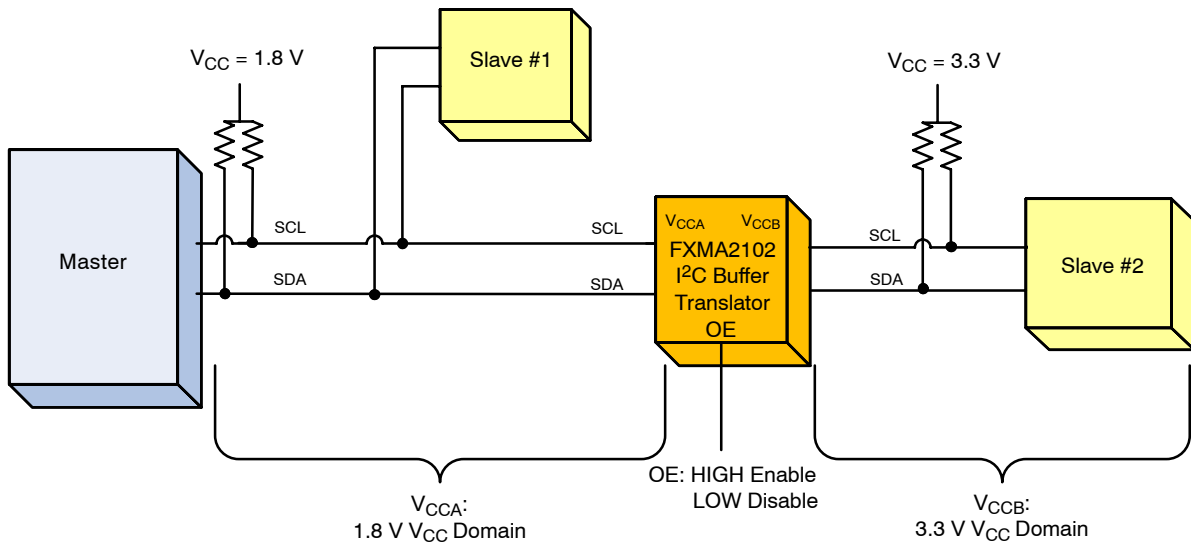


Figure 6. Bus Clear

Power-Good Voltage

Typically, if V_{CCA} or V_{CCB} are below 600 mV, the I²C signals (SDA and SCL) are tri-state on both the FXMA2102 A port and B port. OE is tied to V_{CCA}.

Typically, if V_{CCA} and V_{CCB} are above 600 mV, the I²C signals (SDA and SCL) are active on both the FXMA2102 A port and B port. OE is tied to V_{CCA}.

Parallel I²C Voltage Segments

Smart-phone applications are driving demand for a variety of mobile IC devices like accelerometers,

gyroscopes, compasses, GPS, proximity sensors, and temperature sensors. Many of these devices communicate with the mobile host processor via I²C, while most of these devices do not share a common V_{CC}. Therefore, to maintain proper I²C communication, the smart-phone architect must segment these individual I²C sensors into parallel voltage segments/domains where their respective V_{CCs} agree. Figure 7 illustrates this concept.

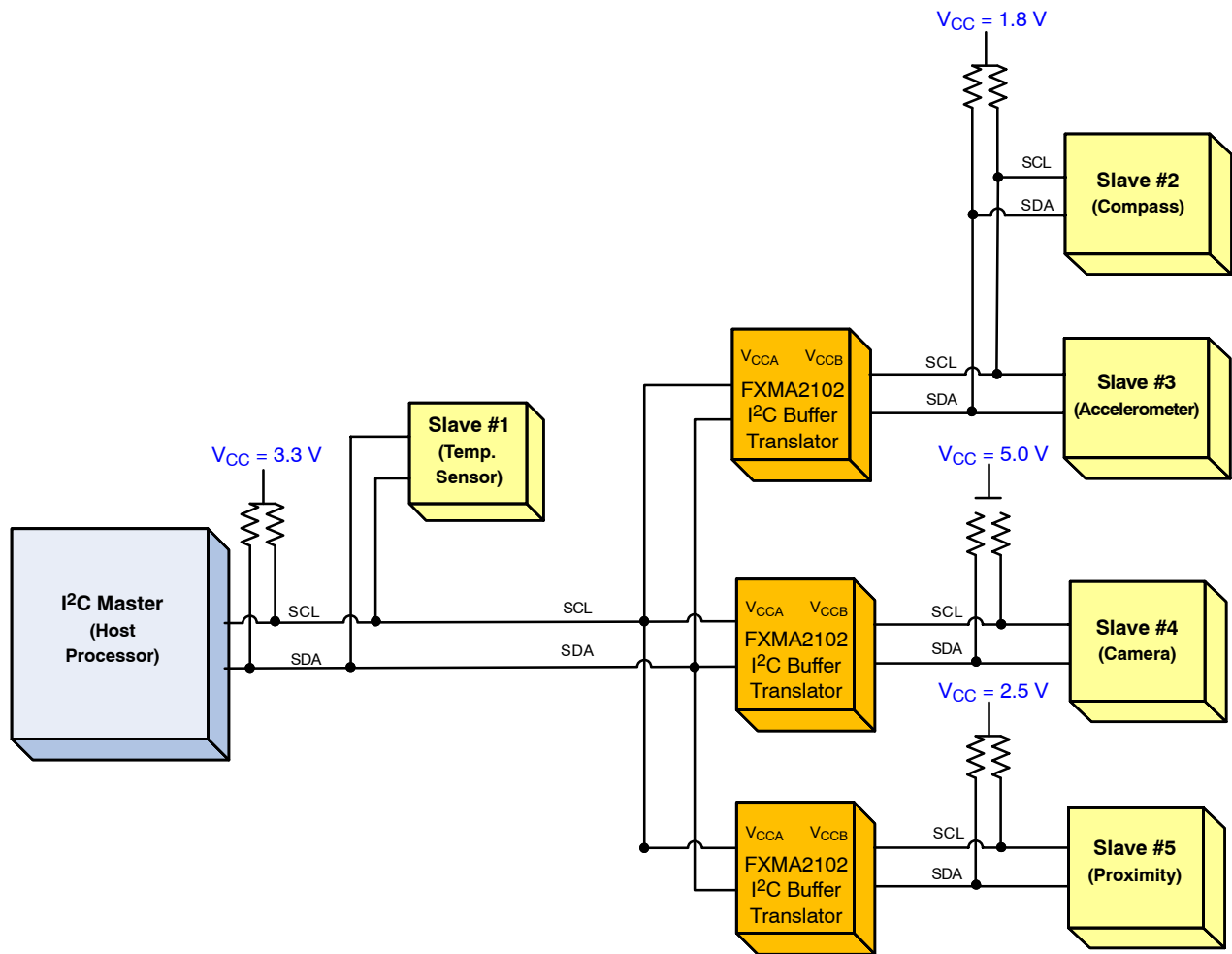


Figure 7. Three V_{CC} Domain Segments in Parallel

Figure 7 depicts a hypothetical example of I²C V_{CC} domain segmentation typical of today’s mobile smart-phone architectures. At the physical layer, multiple I²C voltage translators are placed in parallel to resolve V_{CC} disagreement. Figure 7 illustrates three V_{CC} domain segments in parallel, each of which is electrically connected to the V_{CCB} sides of each I²C translator.

- I²C V_{CC} Domain Segment #1: Slave #2 and Slave #3 at 1.8 V
- I²C V_{CC} Domain Segment #2: Slave #4 at 5.0 V

- I²C V_{CC} Domain Segment #3: Slave #2 at 2.5 V
Meanwhile, the I²C master and slave #1 represent a fourth V_{CC} domain segment at 3.3 V on the V_{CCA} sides of the three I²C translators.

RELATED DEVICES AND DATASHEETS

onsemi offers other voltage level translators suitable for I²C-Bus and SMBus applications. Table 1 below shows the configurations that are available.

Table 1.

Device / Datasheet	Number of Channels	Integrated I/O Pull-Ups
FXMA2102	2	n/a
FXMAR2102	2	10 kΩ
FXMA2104	4	n/a
FXMAR2104	4	10 kΩ
NL5X4002 (Notes 1 and 2)	2	10 kΩ
NL5X4E02 (Note 1)	2	n/a

1. Please contact onsemi for more information.
2. AEC-Q100 Qualified devices available.

onsemi is licensed by Philips Corporation to carry the I²C Bus Protocol.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales