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AN-9077

Motion SPM® 7 Series User's Guide

Table of Contents

1 Introduction

This application note is about Motion SPM® 7 Series. It should be used in conjunction with the datasheet, the reference design, and other related application notes listed in the Related Resources section.

1.1. Design Concept

The key design objective of Motion SPM 7 series is to provide a solution for compact and reliable inverter design when assembly space is constrained. It also can provide an energy-efficient solution for small power-motor drive applications, such as fans and pumps.

SPM 7 series MOSFETs reduce the amount of body-diode reverse-recovery charge to minimize the switching loss and enable fast switching operations. Softness of the reverse-recovery characteristics is managed through advanced MOSFET design processes and optimized gate resistor selection to contain Electromagnetic Interference (EMI) noise within a reasonable range.

The SPM 7 series has six fast-recovery MOSFETs (FRFET®) and one three-phase HVIC. These MOSFETs and HVIC are not available as discrete parts. The FRFET-based power module has improved ruggedness and a larger Safe Operation Area (SOA) than IGBT-based module or Silicon-On-Insulator modules.

The FRFET-based power module has an advantage over an IGBT-based power module in light-load efficiency because the voltage drop across the transistor decreases linearly as current decreases; whereas IGBT V_{CE} saturation voltage stays at the threshold level. Some applications require continuous operation at light load except short transients, and improving the efficiency in the light-load condition is the key to saving energy. Refrigerators, water circulation pumps, and some fans are good examples.

The temperature-sensing function is implemented in the HVIC to enhance the system reliability. An analog voltage proportional to the temperature of the HVIC is provided for monitoring the module temperature and protection against over-temperature situations.

1.2. Features

The detailed features and integrated functions are:

- 250 V/ 500 V 3-phase FRFET Inverter Including HVIC
- Max. $R_{DS(ON)}$ - FSB70325; 1.4 Ω, FSB70625; 0.8 Ω , FSB70250; 3.4 Ω, FSB70450; 2.2 Ω , FSB70550; 1.85 Ω
- Separate Open-Source Pins from Low-Side MOSFETs for Three-Phase Current-Sensing
- Active-HIGH Interface, Works with 3.3 / 5 V Logic
- Schmitt-Trigger Input
- Optimized for Low Electromagnetic Interference
- HVIC Temperature-Sensing Built-In for Temperature
- Monitoring
- HVIC for Gate Driving with Under-Voltage Protection
- Interlock Function
- Isolation Rating: 1500 VRMS / Minimum
- Moisture Sensitive Level (MSL) 3
- RoHS Compliant

2 Product Selections

2.1. Ordering Information

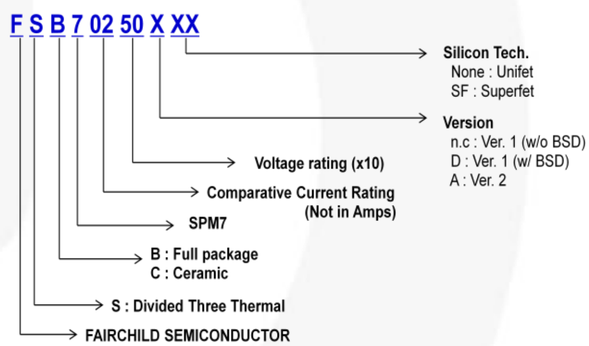


Figure 1. Ordering Information

2.2. Product Line-Up

Table 1 shows the basic line up without package variations.

Table 1. Product Line-Up

Part Number	BV_{DSS}	Current Rating				$R_{\theta JCB}$ (Typ.)
		I_{D25}	I_{DP}	$R_{DS(ON)}$ (Typ.)	$R_{DS(ON)}$ (Max.)	
FSB70325	250	4.1	8.2	1.1	1.4	2.0
FSB70625	250	6.9	13.9	0.7	0.8	1.2
FSB70250	500	3.3	6.7	2.5	3.4	1.2
FSB70450	500	4.8	9.7	1.9	2.2	0.9
FSB70550	550	5.3	10.6	1.6	1.85	0.9

An online loss and temperature simulation tool, Motion Control Design Tool *(http://www.fairchildsemi.com/support/design-tools/motion-control-design-tool/)*, is recommended to choose the right SPM product for the application.

3 Package

3.1. Internal Circuit Diagram

The internal circuit diagram is shown in Figure 2. The V_{TS} pin from the HVIC gives the temperature-sensing signal.

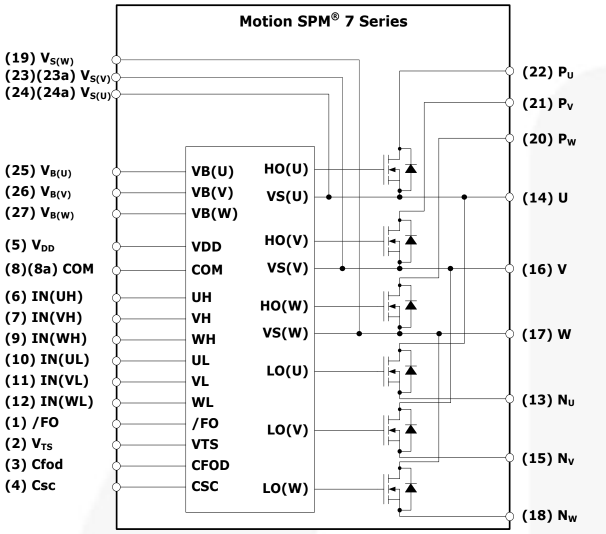


Figure 2. Circuit Diagram of Motion SPM 7 Series

3.2. Pin Description

Figure 3 shows the locations and the names of the pins. Figure 5 in the later section illustrates the internal layout of the module in more details.

The detailed functional descriptions are provided in Table 2.

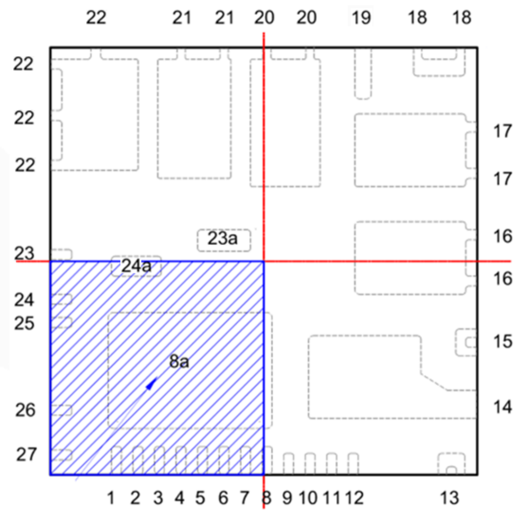


Figure 3. Pin Map (Top View)

Table 2. Pin Description

Pin #	Name	Pin Description
1	/FO	Fault Output
2	V_{TS}	Voltage Output of HVIC Temperature
3	Cfod	Capacitor for Duration of Fault Output
4	CSC	Capacitor (Low-Pass Filter) for Short-Circuit Current Detection Input
5	V_{DD}	Supply Bias Voltage for IC and MOSFETs Driving
6	IN_UH	Signal Input for High-Side U Phase
7	IN_VH	Signal Input for High-Side V Phase
8 (8a)	COM	Common Supply Ground
9	IN_WH	Signal Input for High-Side W Phase
10	IN_UL	Signal Input for Low-Side U Phase
11	IN_VL	Signal Input for Low-Side V Phase
12	IN_WL	Signal Input for Low-Side W Phase
13	Nu	Negative DC-Link Input for U Phase
14	U	Output for U Phase
15	Nv	Negative DC-Link Input for V Phase
16	V	Output for V Phase
17	W	Output for W Phase
18	Nw	Negative DC-Link Input for W Phase
19	$V_{S(W)}$	High-Side Bias Voltage Ground for W Phase MOSFET Driving
20	P_W	Positive DC-Link Input for W Phase
21	P_V	Positive DC-Link Input for V Phase
22	P_U	Positive DC-Link Input for U Phase
23(23a)	$V_{S(V)}$	High-Side Bias Voltage Ground for V Phase MOSFET Driving
24(24a)	$V_{S(U)}$	High-Side Bias Voltage Ground for U Phase MOSFET Driving
25	$V_{B(U)}$	High-Side Bias Voltage for U Phase MOSFET Driving
26	$V_{B(V)}$	High-Side Bias Voltage for V Phase MOSFET Driving
27	$V_{B(W)}$	High-Side Bias Voltage for W Phase MOSFET Driving

High-Side Bias Voltage Pins for Driving the High-Side MOSFET / High-Side Bias Voltage Ground Pins for Driving the High-Side MOSFET

Pins: $V_{B(U)}$ – U,$V_{S(U)}$, $V_{B(V)}$ – V,$V_{S(V)}$, $V_{B(W)}$ – W,$V_{S(W)}$

- These are drive power supply pins for providing gate drive power to the high-side MOSFETs.
- The advantage of boot-strap scheme is that no separate external power supplies are required to drive the high-side MOSFETs.
- Each bootstrap capacitor is charged from the V_{DD} supply during ON state of the corresponding low-side MOSFET.
- To prevent malfunctions caused by noise and ripple in supply voltage, a quality filter capacitor with low Equivalent Series Resistance (ESR) and Equivalent Series Inductance (ESL) should be mounted very close to these pins.

Supply Bias Voltage for IC and MOSFETs Driving

Pin: V_{DD}

- This is a control supply pin for the internal ICs.
- This pin should be connected externally.
- To prevent malfunctions caused by noise and ripple in the supply voltage, a quality of filter capacitor with low ESR and ESL should be mounted very close to this pin.

Low-Side Common Supply Ground Pin

Pin: COM

- The common pin connects to the control ground for the internal ICs.
- **Important!** To prevent switching noises caused by parasitic inductance from influencing operations of the module, the main power current should not flow through this pin.

Signal Input Pins

Pins: $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$, $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$

- These are pins to control operation of the MOSFETs.
- These terminals are activated by voltage input signals and internally connected to a Schmitt trigger circuit.
- The signal logic of these pins is active HIGH: the MOSFET turns ON when sufficient logic voltage is applied to the associated input pin.
- The wiring of each input needs to be short to protect the module against noise influences.
- The RC filter can be used to mitigate signal oscillations or noise picked up by the trace of the input signals.

Analog Temperature Sensing Output Pin

Pin: V_{TS}

- This indicates the temperature of the HVIC with analog voltage. The HVIC itself creates some power loss, but mainly it is heat generated from the MOSFETs that increases the temperature of the HVIC
- V_{TS} vs. temperature characteristics is illustrated in Figure 14.

Positive DC-Link Pins

Pins: P_U, P_V, P_W

- These are the DC-link positive power supply pins of the inverter.
- These are connected to the collectors of the high-side MOSFETs.
- These pins should be connected externally.
- To suppress the surge voltage caused by the DC-link wiring or PCB pattern inductance, connect a smoothing filter capacitor close to this pin. Metal film capacitors are typically recommended.

Negative DC-Link Pins

Pins: N_U, N_V, N_W

- These are the DC-link negative power supply pins (power ground) of the inverter.
- These pins are connected to the low-side MOSFET sources of the each phase.

Inverter Power Output Pin

Pins: U, V, W

- Inverter output pins to be connected to the inverter load, such as an electrical motor.

Short-Current Detection Pin

Pin: CSC

- A current-sensing shunt resistor should be connected between this pin and the low-side ground COM to detect short-circuit current *(reference Figure 12).*
- The shunt resistor should be selected to meet the detection levels matched for the specific application. An RC filter should be connected to CSC pin to eliminate noise.
- The connection length between the shunt resistor and CSC pin should be minimized.

Fault Output Pin

Pin: /FO

- This is the fault output alarm pin. An active-LOW output is given on this pin for a fault state condition in the SPM.
- The alarmed conditions are Short-Circuit (SC) or low-side bias Under-Voltage (UV) operation.
- It is an open-collector output and should be pulled up to the 5 V logic power supply with approximately 4.7 kΩ resistance.

Fault-Out Duration Time Selection Pin

Pin: C_{FOD}

- This is the pin for selecting the fault-out pulse length.
- An external capacitor should be connected between this pin and COM to set the fault-out pulse length.
- The fault-out pulse width, t_{FOD}, depends on the capacitance of C_{FOD}, as the following approximates:

$$C_{FOD} = 24 \times 10\text{-}6 \times t_{FOD} \text{ [F]} \quad (1)$$

3.3. Package Structure

Figure 4 shows the internal package structure, including the lead frame and bonding wires. This design has been revised to further improve the manufacturability and the reliability.

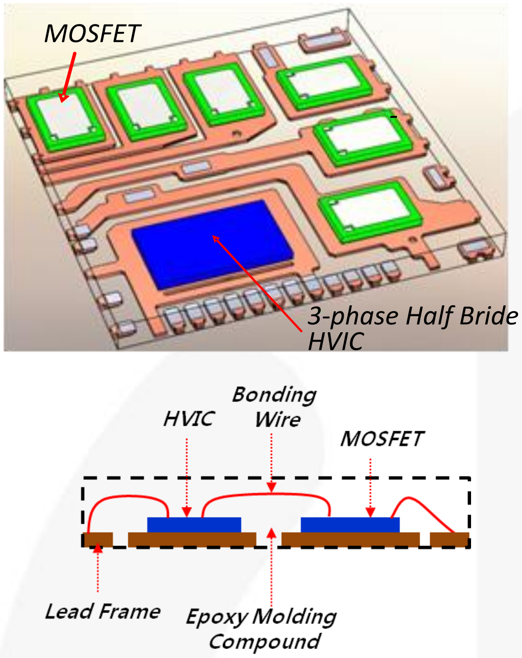


Figure 4. Package Structure

3.4. Package Outline

For more detailed data regarding the package dimension and land pattern recommendation, refer to the datasheet.

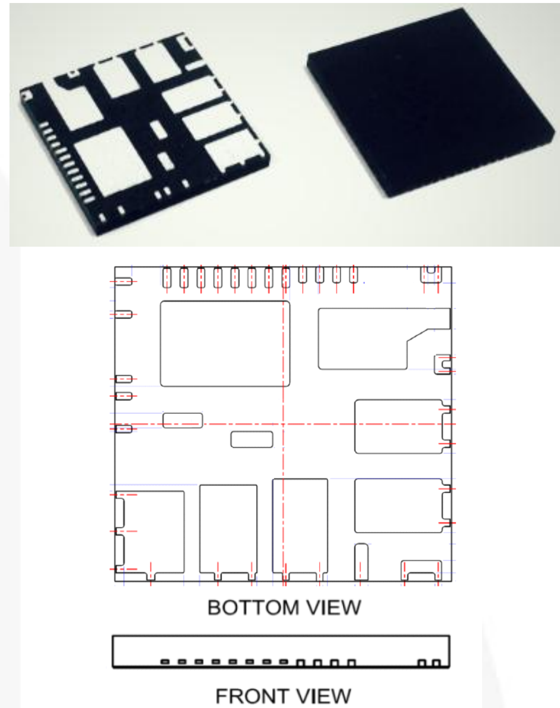


Figure 5. Package Outline

3.5. Marking Specification

The marking of the package is shown in Figure 6.

1ST LINE MARKING

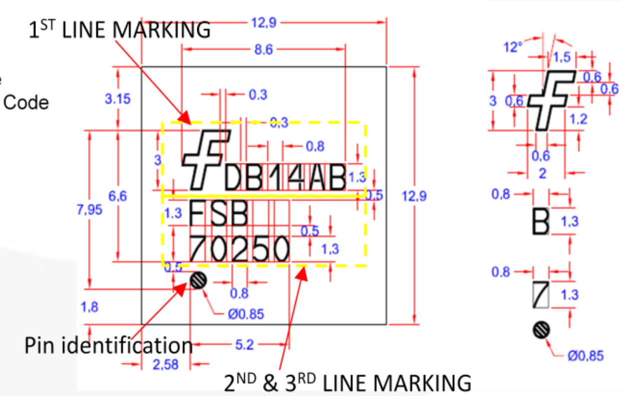
SYMBOLS	-	MEANING
D	-	Plant Code
D	-	Calendar year code
14	-	Workweek date code
AB	-	Die Run Code or Lot Code
CIRCLE	-	Pin 1 Identification

2ND & 3RD LINE MARKING

FSB	-	Device Mark
7025	-	Device Mark

Calendar Year	Code
2010	A
2011	B
2012	C
2013	D
2014	E
2015	F
2016	G
2017	H
2018	J
2019	K

SPM7 MARKING LAYOUT



Note
- All dimensions are in mm
- All front including pin mark would be 0.08mm width
- Marking Font is Arial or Helv

Figure 6. Marking of Package

4 Integrated Functions and Protection Circuit

4.1. Internal Structure of HVIC

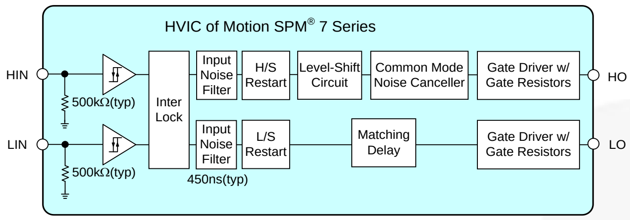


Figure 7. Internal Block Diagram of HVIC

Figure 7 shows the block diagram of structure of the HVIC inside the Motion SPM 7 series. Gate signal input pins have internal 500 kΩ pull-down resistors. The weak pull-down reduces standby power consumption. If there is concern about malfunction due to noise associated with layout, additional pull-down resistors of 4.7 kΩ, for example, can be placed close to the module input pins. RC filters can be used instead of pull-downs to eliminate noise and narrow pulses as well. Consider, however, that this filter introduces some distortion of PWM volt-second because the ON/OFF thresholds are not symmetrical within the supplied voltage.

4.2. Circuit of Input Signal ($V_{IN(H)}$, $V_{IN(L)}$)

Figure 8 shows an example of PWM input interface circuit from the MCU to Motion SPM 7 series. The input logic is active HIGH and, because there are built-in pull-down resistors of 500 kΩ; external pull-down resistors are not typically needed.

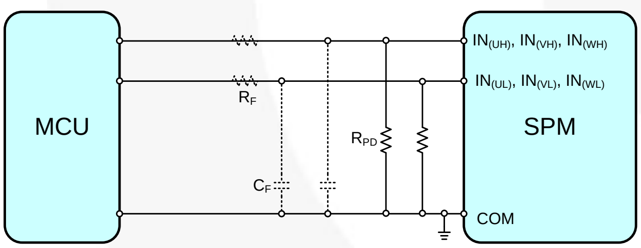


Figure 8. Recommended MCU I/O Interface Circuit

The maximum rating voltages of input pins are shown in Table 3. The RC coupling at each input is shown as dotted in Figure 8 and may change depending on the PWM control scheme used in the application and the wiring impedance of the application PCB layout.

Table 3. Maximum Ratings of Input Pins

Symbol	Item	Condition	Rating	Unit
V_{DD}	Control Supply Voltage	Applied between V_{DD} – COM	20	V
V_{IN}	Input Signal Voltage	Applied between IN(xH) – COM, IN(xL) – COM	-0.3 ~ V_{DD} + 0.3	V

The Motion SPM 7 series employ active-HIGH input logic. This removes the sequence restriction between the control supply and the input signal during startup or shutdown of power supply operation. In addition, pull-down resistors are internal to each input circuit. External pull-down resistors are not typically needed, and the number of external components is smaller as a result. The input noise filter inside the HVIC suppresses short-pulse noise and prevents the MOSFET from malfunction and excessive switching loss. Furthermore, by lowering the turn-on and turn-off threshold voltages of the input signal, as shown in Table 4, a direct connection to 3.3 V-class MCU or DSP is possible.

Table 4. Input Threshold Voltage Ratings (at V_{DD}=15 V, T_J=25°C)

Symbol	Item	Condition	Min.	Max.	Unit
V_{IH}	On Threshold Voltage	$IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$ – COM		2.4	V
V_{IL}	Off Threshold Voltage	$IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ - COM	0.8		V

As shown in Figure 7, the input signal integrates a 500 kΩ (typical) pull-down resistor. Therefore, when using an external filtering resistor between the MCU output and the Motion SPM® input, attention should be paid to the signal voltage drop at the SPM® input terminals to satisfy the turn-on threshold voltage requirement. For instance, R=100 Ω and C=1 nF can be used for the parts shown dotted in Figure 8.

4.3. Functions vs. Control Supply Voltage

Control and gate drive power for the Motion SPM 7 series is normally provided by a single 15 V DC supply connected to the module V_{DD} and COM terminals. For proper operation, this voltage should be regulated to 15 V ±10% and its current supply should be >260 µA for the SPM product only. Table 5 describes the behavior of the SPM parts for various control supply voltages. The control supply should be well filtered with a low-impedance electrolytic capacitor and a high-frequency decoupling capacitor connected at the pins.

High-frequency noise on the supply might cause the internal control IC to malfunction and generate erroneous fault signals. To avoid this, the maximum ripple on the supply should <±1 V/µs. In addition, it may be necessary to connect a 24 V/1 W Zener diode across the control supply to prevent surge destruction under severe conditions.

It is crucial that all control circuits and power supplies be referred to COM terminal of the module; not to the N power terminal. In general, it is best practice to make the common reference (COM) a ground plane in the PCB layout.

The main control power supply is also connected to the bootstrap circuits used to establish the floating supplies for the high-side gate drives.

When control supply voltage (V_{DD} and V_{BS}) falls below Under-Voltage Lockout (UVLO) level, HVIC turns off the MOSFETs while disregarding gate control input signals.

Table 5. Control Voltage Range vs. Operations

Control Voltage Range	Function Operations
0 ~ 5 V	Control IC does not operate. UVLO and fault output do not operate. dv/dt noise on main P-N supply can trigger MOSFETs.
5 ~ 10 V	Control IC starts to operate. As the UVLO is set, gates of MOSFETs pull down regardless of control input signals.
10 ~ 13.5 V	UVLO is cleared. MOSFETs operate in accordance with control gate input. Driving voltage is below recommended range; $R_{DS(ON)}$ and the switching loss are higher than under normal condition.
13.5 ~ 16.5 V_{DD}	**Normal operation. This is the recommended operating condition.**
16.5~20 V for V_{DD} 16.5~20 V for V_{BS}	MOSFETs still operate. Because driving voltage is above the recommended range, MOSFETs switch faster. May increase system noise. Peak short-circuit current may increase.
Over 20 V	Module control circuit in can be damaged.

4.4. Under-Voltage Lockout Protection (ULVO)

The three-phase HVIC has an under-voltage lockout function to protect MOSFETs from operation with insufficient gate driving voltage. A timing chart for this protection is shown in Figure 9 and Figure 10.

a1: Control supply voltage rises: after the voltage reaches UV_{BSR}, the circuit starts to operate immediately.

a2: Normal operation: MOSFET turns on and carries current.

a3: Under-Voltage detection (UV_{BSD}).

a4: MOSFET turns off regardless of control input condition, but there is no fault output signal.

a5: Under-voltage lockout is cleared (UV_{BSR}).

a6: Normal operation: MOSFET turns on and carries current.

b1: Control supply voltage rises: after the voltage rises UV_{DDR}, the circuit starts when next input comes in.

b2: Normal operation: MOSFET turns on and carries current.

b3: Under-voltage detection (U_{VDDD}).

b4: MOSFET turns off regardless of control input condition and fault output signal goes LOW.

b5: Under-voltage lockout is cleared (UV_{DDR}).

b6: Normal operation: MOSFET turns on and carries current.

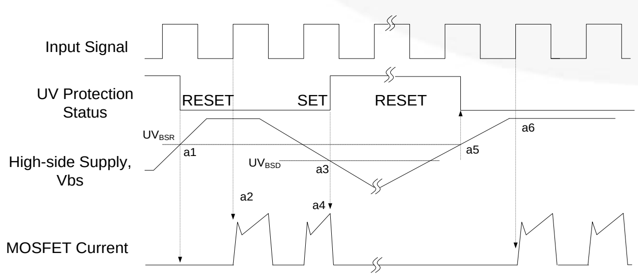


Figure 9. Timing Chart of UVLO [High Side]

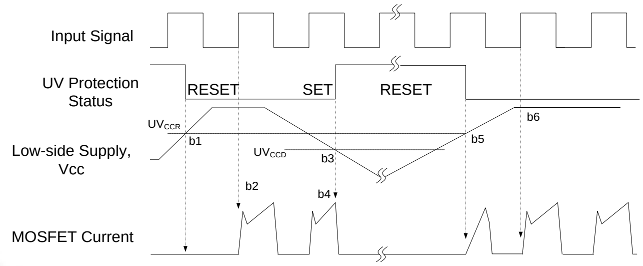


Figure 10. Timing Chart of UVLO [Low Side]

4.5. Short-Circuit Protection

4.5.1 Timing of Short-Circuit Protection

The HVIC has a built-in short-circuit function. The IC monitors the voltage to the CSC pin and, if this voltage exceeds the $V_{SC(ref)}$, which is specified in the device datasheet, a fault signal is asserted and the six MOSFETs are turned off. The maximum short-circuit current magnitude is Typically gate-voltage dependant. A higher gate voltage results in a larger short-circuit current. To avoid this potential problem, the maximum short-circuit trip level is generally set to below 1.7 times the nominal rated collector current. The LVIC short-circuit protection-timing chart is shown in Figure 11 (with the external shunt resistance and RC connection).

c1: Normal operation: MOSFET ON and carrying current.

c2: Short-circuit current detection (SC trigger).

c3: Hard MOSFET gate interrupt.

c4: MOSFET turns OFF.

c5: Fault output timer operation starts: the pulse width of the fault output signal is set by external capacitor C_{FO}.

c6: Input LOW: MOSFET OFF state.

c7: Input HIGH: MOSFET ON state, but during the active period of fault output the MOSFET doesn't turn ON.

c8: MOSFET OFF state.

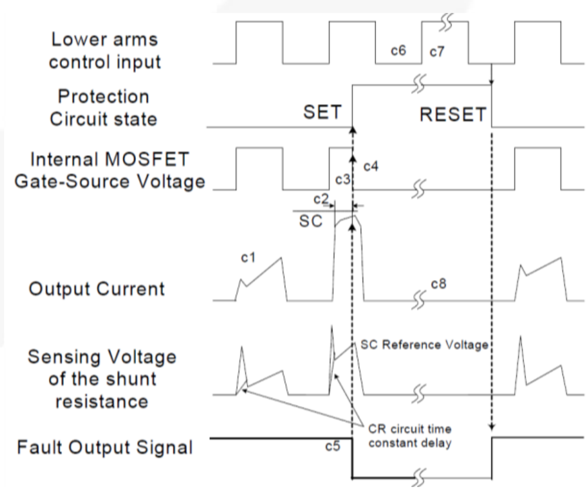


Figure 11. Timing Chart of Short-Circuit Protection

4.5.2 Selecting Current Sensing Shunt Resistor

Figure 12 shows an example circuit of the SC protection using a 1-shunt resistor. The line current on the N side DC-link is detected and the protective operation signal is passed through the RC filter. If the current exceeds the SC reference level, all the gates of the six MOSFETs are switched to OFF state and the FO fault signal is transmitted to the CPU. Since SC protection is non-repetitive, MOSFET operation should be immediately halted when the FO fault signal is given.

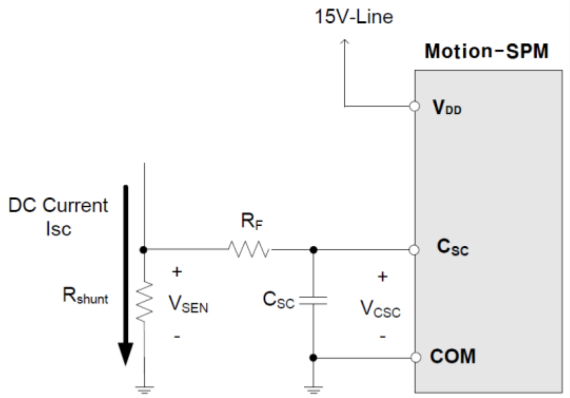


Figure 12. Example of Short Circuit Protection Circuit with 1-Shunt Resistors

The internal protection circuit is triggered under short-circuit condition by comparing the external shunt voltage to the reference SC trip voltage in the LVIC. The drive IC then interrupts low-side MOSFET gates to stop MOSFET operation. The value of current-sensing resistor is calculated by the following expression:

$$R_{SHUNT} = \frac{V_{SC(REF)}}{I_{SC}} \quad (2)$$

where $V_{SC(REF)}$ is the SC reference voltage of the HVIC.

An RC filter (reference RF CSC above) is necessary to prevent noise related SC circuit malfunction. The RC time constant is determined by the applied noise time and the MOSFET withstand capability. It is recommended to be set in the range of 1.5 ~ 2 µs.

When the external shunt resistor voltage drop exceeds the SC protection level, this voltage is applied to the C_{SC} pin via the RC filter. The filter delay time (t1) is required for the C_{SC} pin voltage to rise to the referenced SC protection level. Table 6 shows the specification of the SC protection level. The IC has an internal delay (t2) of 550 ns, including internal filtering time (Typical 400 ns).

Therefore, the total time from the detection of the SC trip current to the gate off of the MOSFET becomes:

$$T_{TOTAL} = t_1 + t_2 \quad (3)$$

Table 6. SC Protection Reference Level $V_{SC(REF)}$

Item	Min.	Typ.	Max.	Unit
SC Trip Level $V_{SC(REF)}$	0.45	0.50	0.55	V

The three-shunt resistor circuit is more complicated and has more considerations than the one-shunt resistor circuit. The three-shunt circuit is popular because it permits sensing of individual phase currents. The circuit is very cost-effective and provides good current-sensing performance.

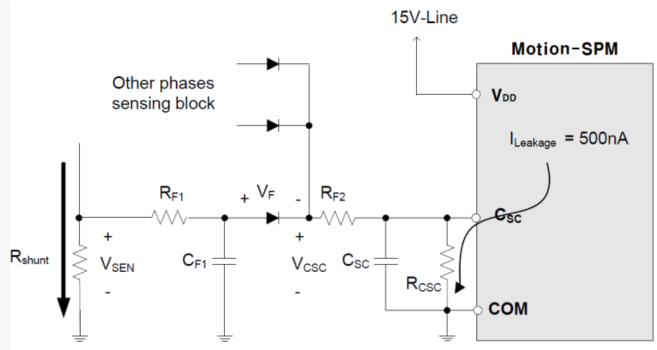


Figure 13. Example of Short Circuit Protection Circuit with 3-Shunt Resistors

Figure 13 shows a typical circuit for short-circuit detection using diodes. There are additional considerations when using this circuit. Note that this circuit is not adequate for the precise over-current detection due to dispersion and temperature dependency of V_F.

The short circuit sensing signal delay increases. A R_{F1} x C_{F1} time constant delay (t3) is added, so total delay becomes:

$$T_{TOTAL} = t_1 + t_2 + t_3 \quad (4)$$

The added diode blocks the IC leakage current (approximately 500 nA) from the CSC pin. If this current is applied to the capacitor, C_{SC}, V_{CSC} increases to a somewhat higher value and causes SPM to stop gating even under normal conditions. To compensate for this corruption of SC current-sensing voltage, R_{CSC} must be placed in parallel with C_{SC}. The recommended value of R_{CSC} is approximately 47 kΩ.

For the short circuit state, the diode drop voltage must be considered to set the short-circuit protection reference level. The equation is:

$$V_{SEN} = V_{CSC} + V_F \quad (5)$$

5 Key Parameter Design Guidance

5.1. Thermal Sensing Unit (TSU)

The junction temperature of power devices should not exceed the maximum junction temperature. Even though there is some margin between the T_{JMAX} specified on the datasheet and the actual T_{JMAX} at which power devices are destroyed, ensure the junction temperature stays well below the T_{JMAX}.

The Thermal Sensing Unit (TSU) uses the technology based on the temperature dependency of transistor V_{be}; V_{be} decrease 2 mV as temperature increases by 1ºC.

The TSU analog voltage output reflects the temperature of the HVIC in Motion SPM 7 series. The relationship between V_{TS} voltage output and HVIC temperature is shown in Figure 14. It does not have any self-protection function and, therefore, should be used properly based on application requirement. There is a time lag from MOSFET temperature to HVIC temperature, making it difficult to respond quickly when temperature rises sharply in a transient condition, such as a shoot-through event. Even though the TSU has some limitations, it enhances system reliability.

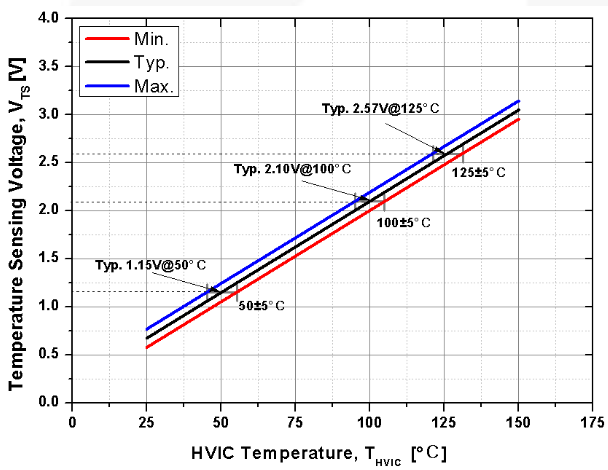


Figure 14. Temperature vs. V_{TS}

Figure 14 shows that the relationship between V_{TS} voltage and V-phase HVIC temperature. It can be expressed as:

$$V_{TS} = 0.019 \times T_{HVIC} + 0.2 \text{ [V]} \quad (6)$$

The maximum variation of V_{TS}, due to process variation, is ±0.095 V, which is equivalent to ±5ºC. This is regardless of temperature because the slopes of the three lines are identical. If the ambient temperature information is available, for example, through NTC in the system; V_{TS} can be measured to adjust the offset before the motor starts.

As temperature decrease further below 0°C, V_{TS} decreases linearly until it reaches zero volts. If the temperature of HVIC increases above 150ºC, which is above the maximum operating temperature, V_{TS} would increase theoretically up to 5.2 V until it gets clamped by the internal Zener diode.

Figure 15 shows the equivalent circuit diagram of the TSU inside the IC and a typical application diagram. The output voltage is clamped to 5.2 V by an internal Zener diode, but if the maximum input range of the analog-to-digital converter of the MCU is below 5.2 V, an external Zener diode should be inserted between an A/D input pin and the analog ground pin of the MCU. An amplifier can be used to change the range of voltage input to the analog-to-digital converter for better resolution of the temperature. It is recommended to add a ceramic capacitor of 1000 pF between V_{TS} and COM (ground) to improve V_{TS} stability.

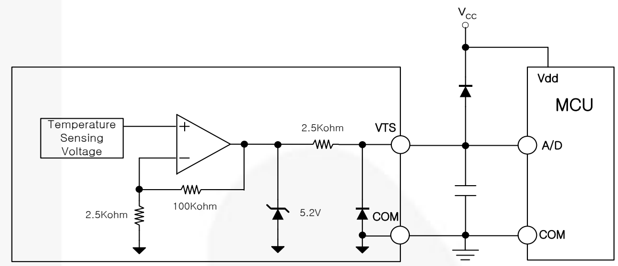


Figure 15. Internal Diagram, Interface Circuit of TSU

Figure 16 and Figure 17 show the sourcing capability of the V_{TS} pin at 25ºC and the test method. V_{TS} voltage decreases as the sourcing current increases. Therefore, the load connected to V_{TS} pin should be minimized to maintain the accurate voltage output level without degradation.

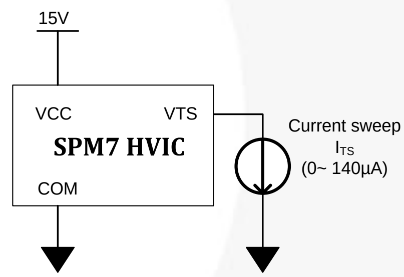


Figure 16. Test Method

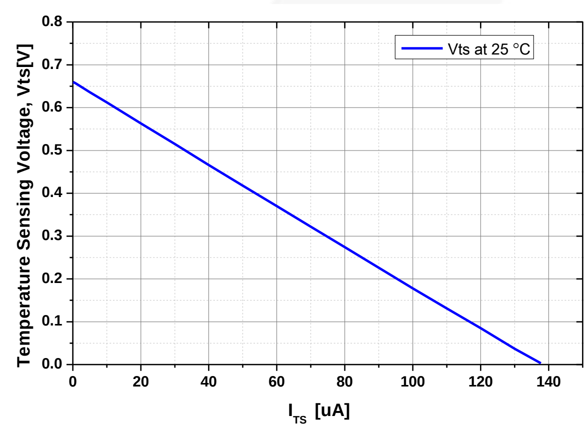


Figure 17. Load Variation of V_{TS}

Figure 18 shows the test result representing the relationship between HVIC temperature and other measured temperature in a real application condition. The real junction temperature was measured with a special package and it is similar to case temperature and P pin (Pu, Pv, Pw) temperature.

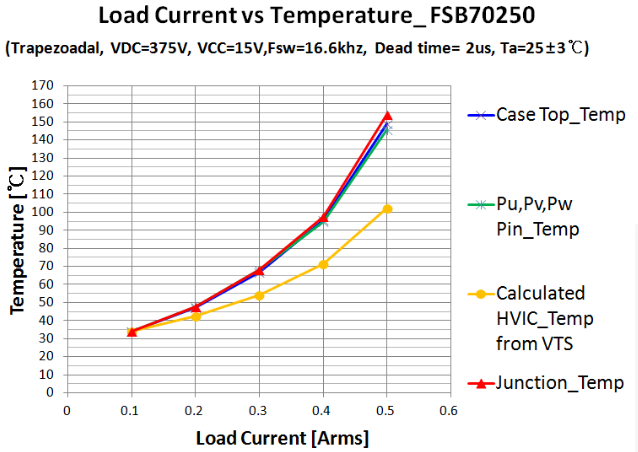


Figure 18. Load Current vs. Temperature (without Heat Sink)

The gap between MOSFET junction temperature and HVIC tempature gradually increases coresponding to load current. Judging from the experiment, MOSFET junction temperature can be estimated by calculated HVIC temperature, as shown in Figure 19. However, system conditions, such as heat dissipation, can change the curve.

Therefore, it is necessary to make a profile according to set application conditions. As shown in Figure 18, real junction temperature has a similar values with measured case temperature or P pin (Pu, Pv, Pw) temperature if an external heatsink is not attached.

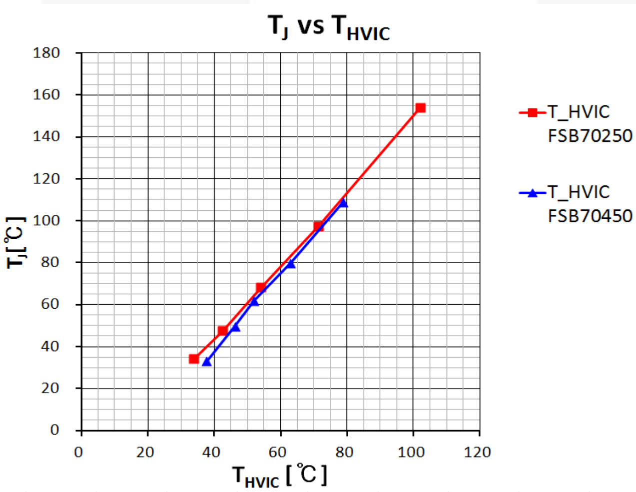


Figure 19. T_J vs. T_{HVIC} (without Heat Sink)

Figure 20 is an example of the over-temperature protection circuit. A comparator with hysteresis is used to create a low-active signal that can be read by a microprocessor. Based on this signal, the microprocessor can disable or enable PWM output. As an example, calculate the resistor values to set the upper threshold level at 100°C and the lower threshold level at 80°C so that the comparator output voltage V_O matches the waveform in Figure 21.

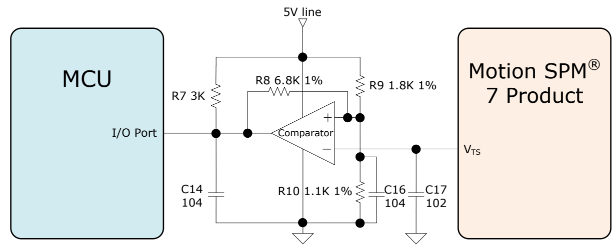


Figure 20. Example of Over-Temperature Protection using TSU (Trip Level)

When the temperature is below 80°C; V_O, the open-collector output of the comparator, should stay HIGH. To make V_O transition to LOW at 100°C, V_{REF} needs to drop below 2.10 V, V_{TS} voltage at 100°C.

$$\frac{1}{\frac{1}{R_9}+\frac{1}{R_7+R_8}} = R_1' \quad \frac{R_{10}}{R_1'+R_{10}} \times 5 = V_{ref} = 2.099V \tag{7}$$

When the temperature is above 100°C, V_O should stay LOW. To make V_O transition to HIGH at 80°C, V_{REF} must be higher than 1.724 V, V_{TS} voltage at 80°C.

$$\frac{1}{\frac{1}{R_{10}}+\frac{1}{R_8}} = R_2' \quad \frac{R_2'}{R_9+R_2'} \times 5 = V_{ref} >= 1.724V \tag{8}$$

There are four variables with two equations, so two variables need to be set. R7, the pull-up resistor for V_O, can be chosen to be 3 kΩ. R2 can be 1.1 kΩ, considering V_{REF} is below one half of the supply voltage (5 V in this example) and R9 needs to be bigger than R10.

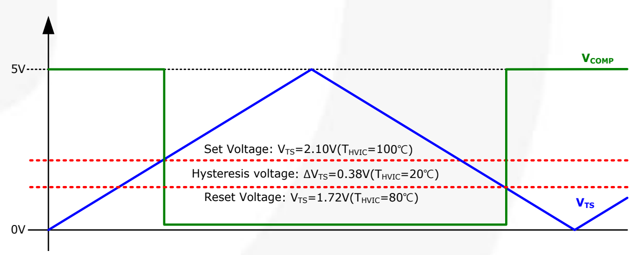


Figure 21. Comparator Output, Hysteresis using TSU

5.2. Bootstrap Circuit Design

5.2.1 Operation of Bootstrap Circuit

The V_{BS} voltage, which is the voltage difference between $V_{B(U,V,W)}$ and $V_{S(U,V,W)}$, provides the supply to the HVIC within the Motion SPM 7 series. This supply must be in the range of 13.5 V~16.5 V to ensure that the HVIC can fully drive the high-side MOSFET. The under-voltage lockout protection for the V_{BS} ensures that the HVIC does not drive the high-side MOSFET if V_{BS} drops below the specific voltage. This function prevents the MOSFET from operating in a high-dissipation mode.

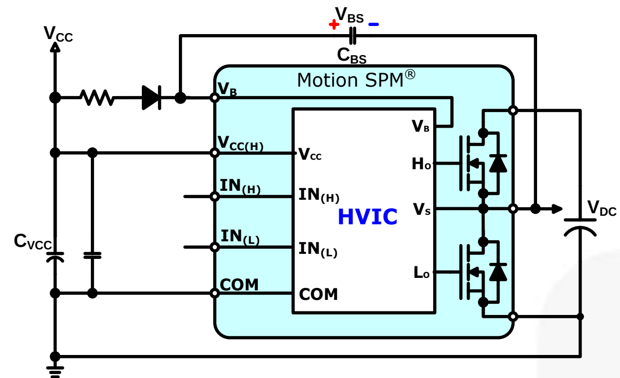


Figure 22. Bootstrap Circuit for the Supply Voltage (V_{BS}) of HVIC

The V_{BS} floating supply can be generated in a number of ways, including the bootstrap method shown in Figure 22. This method has the advantage of being simple and inexpensive; however, the duty cycle and on-time are limited by the need to refresh the charge in the bootstrap capacitor. The bootstrap supply is formed by a combination of bootstrap diode, resistor, and capacitor, as shown in Figure 22.

The current flow path of the bootstrap circuit is shown in Figure 23. When V_S is pulled down to ground (either through the low-side power device or the load), the bootstrap capacitor (C_{BS}) is charged through the bootstrap diode (D_{BS}) and the resistor (R_{BS}) from the V_{DD} supply.

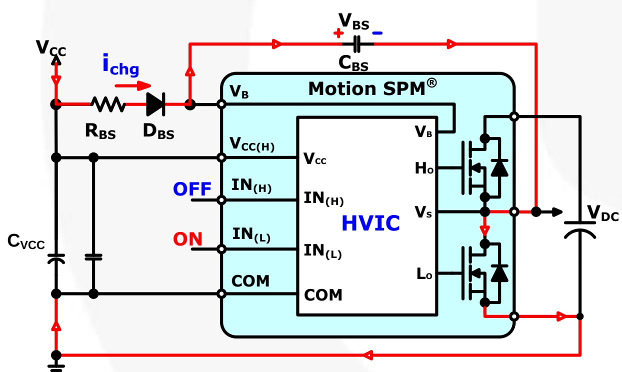


Figure 23. Bootstrap Circuit Charging Path

5.2.2 Initial Charging of Bootstrap Capacitor

Adequate on-time duration of the low-side MOSFET to fully charge the bootstrap capacitor is initially required before normal operation of the PWM starts. Figure 24 shows an example of the initial bootstrap charging sequence. Once V_{DD} establishes, V_{BS} needs to be charged by turning on the low-side MOSFETs. PWM signals are typically generated by an interrupt triggered by a timer with a fixed interval based on the switching carrier frequency. Therefore, it is desirable to maintain this structure without creating complimentary high-side PWM signals.

The capacitance of V_{DD} should be sufficient to supply necessary charge amount to V_{BS} capacitance of all three phases. If normal PWM operations start before V_{BS} reaches the under-voltage lockout reset level, the high-side MOSFETs do not switch without creating any fault signal. This can lead to failure of motor start in some applications.

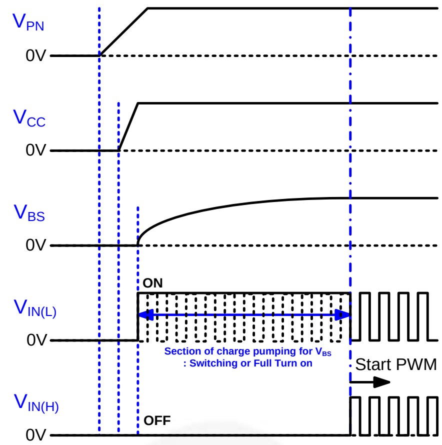


Figure 24. Timing Chart of Initial Bootstrap Charging

If the three phases are charged synchronously, initial charging current through a single shunt resistor may exceed the over-current protection level. Therefore, the initial charging time for the bootstrap capacitors should be separated, as shown in Figure 25.

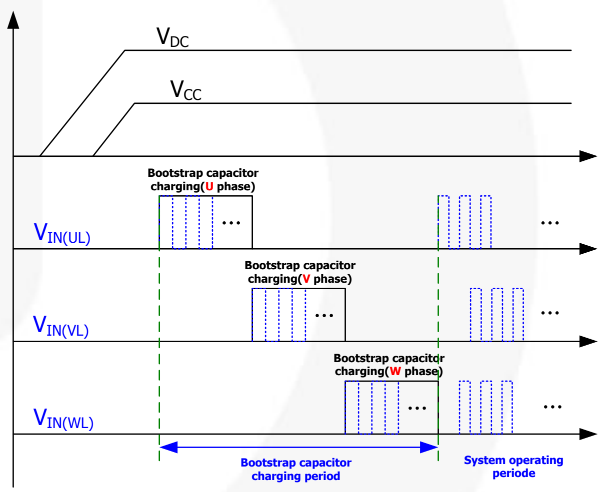


Figure 25. Recommended Initial Bootstrap Capacitor Charging Sequence

Adequate on-time duration of the low-side MOSFET to fully charge the bootstrap capacitor is required for initial bootstrap charging.

In case of Motion SPM® 7 Series, the initial charging time (t_{charge}) can be calculated from the following equation:

$$t_{charge} = C_{BS} \times R_{BS} = \frac{1}{\delta} \times In \frac{V_{CC}}{V_{CCg} - V_{BS(\min)} - V_F - V_{LS}} \quad (9)$$

where:

V_F: forward voltage drop across the bootstrap diode;

$V_{BS(min)}$: minimum value of the bootstrap capacitor;

V_{LS}: voltage drop across the low-side MOSFET or load; and

δ: duty ratio of PWM. (0 – 1).

5.2.3 Selection of Bootstrap Capacitor

The bootstrap capacitor of Motion SPM® 7 series can be calculated by:

$$C_{BS} = \frac{Q_{BS}}{\Delta V_{BS}} \quad (10)$$

where:

Q_{BS} = Total charge from C_{BS};

ΔV_{BS} = the allowable drop voltage of the C_{BS} (voltage ripple).

Total gate charge, Q_{BS}, required by the bootstrap capacitor can be calculated by:

$$Q_{BS} = Q_g + (I_{LK,D} + I_{LK,C} + I_{QBS}) \times t_{ON} + Q_{LS} \quad (11)$$

where:

Q_g = Gate charge to turn on the high-side MOSFET;

$I_{LK,D}$ = Bootstrap diode leakage current;

$I_{LK,C}$ = Bootstrap capacitor leakage current, which can be ignored if it is not an electrolytic capacitor;

I_{QBS} = Quiescent current of gate driver IC;

t_{ON} = Maximum on pulse width of high-side MOSFET; and

Q_{LS} = Level-shift charge required per cycle.

In case of FSB70325, minimum C_{BS} is calculated as:

$$C_{BS\_min} = \frac{Q_{BS}}{\Delta V_{BS}} = \frac{Q_g + Q_{LS} + (I_{LK,D} + I_{LK,C} + I_{QBS}) \times t_{ON}}{\Delta V_{BS}} = \frac{50nC + (100\mu A + 0 + 70\mu A) \times 200\mu s}{0.1V} = 0.84\mu F \quad (12)$$

→ More than two times (2X) → 2.2 µF

where:

V_{DD} = 15 V;

Bootstrap Diode = US1J;

$Q_g + Q_{LS}$ = Approximately 50 nC (designed value);

$I_{LG,D}$ = 100 µA (maximum value from datasheet);

$I_{LK,C}$ = 0 (ceramic capacitor);

I_{QBS} = 70 µA (maximum value from datasheet);

t_{ON} = 200 µs (depends on system); and

ΔV_{BS} = 0.1 V (depends on system).

Recommended CBS is normally two times C_{BS_min}.

This capacitance value can be changed according to the switching frequency, the type of capacitor used, and the recommended V_{BS} voltage of 13.5~16.5 V (from datasheet). The above result is a calculation example and can be changed according to the actual control method and lifetime of the selected components.

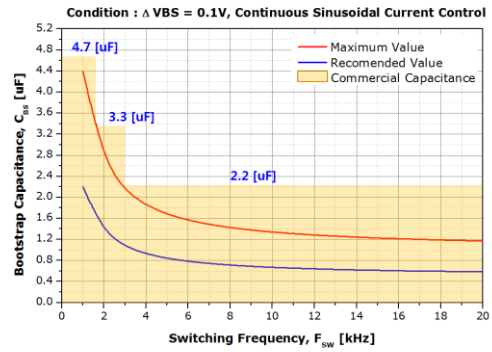


Figure 26. Capacitance of Bootstrap Capacitor on Variation of Switching Frequency

The bootstrap capacitor should always be placed as close to the pins of the SPM as possible. At least one low-ESR capacitor should be used to provide local de-coupling. For example, a separate ceramic capacitor close to the SPM is essential if an electrolytic capacitor is used for the bootstrap capacitor. If the bootstrap capacitor is either a ceramic or tantalum, it should be adequate for local decoupling.

5.2.4 Selection of Bootstrap Diode

When a high-side MOSFET or body-diode conducts, the bootstrap diode (D_{BS}) supports the entire bus voltage. A withstand voltage of more than 600 V is recommended. It is important that this diode be fast recovery (recovery time < 100 ns) to minimize the amount of charge fed back from the bootstrap capacitor into the V_{DD} supply. Similarly, the high-voltage reverse leakage current is important if the capacitor must store a charge for long periods of time.

5.2.5 Selection of Bootstrap Resistance

A resistor, R_{BS}, must be added in series with the bootstrap diode to slow down the dV_{BS}/dt and this resistor determines the time to charge the bootstrap capacitor. If the minimum ON pulse width of the low-side MOSFET or the minimum OFF pulse width of high-side MOSFET is t_O, the bootstrap capacitor must be charged ΔV during this period. Therefore, the value of bootstrap resistance can be calculated by:

$$R_{BS} = \frac{(V_{CC} - V_{BS}) \times t_O}{C_{BS} \times \Delta V_{BS}} \quad (13)$$

The current flow path of the bootstrap circuit is shown in Figure 27. When V_S is pulled down to ground (either through the low-side power device or the load), the bootstrap capacitor, C_{BS}, is charged through the bootstrap diode, D_{BS}, and the resistor, R_{BS}, from the V_{DD} supply.

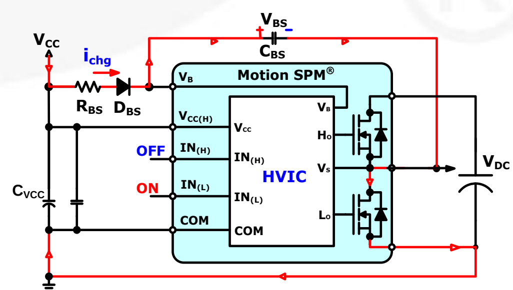


Figure 27. Charging Bootstrap Capacitor at Startup

5.3. Minimum Pulse Width

As shown in Figure 28, input noise filters with a 450 ns time constant screen out pulses narrower than the filter time constant. Additional propagation delay in the level-shifter and other circuits, plus gate charging time, prevent Motion SPM 7 series from responding to a narrow input pulse.

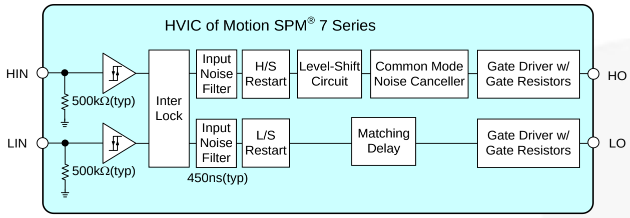
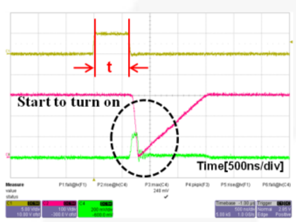


Figure 28. Internal Structure of Signal Input Pins

VDD=VBS	13V	15V	20V
High Side	771	645	500
Low Side	738	629	476

VIN[5V/div] ID[50mA/div] VDS[100V/div]



VDD=VBS	13V	15V	20V
High Side	344	404	543
Low Side	327	409	587

VIN[5V/div] ID[50mA/div] VDS[100V/div]

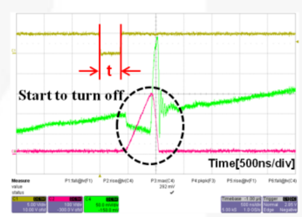


Figure 29. Test Result for Short Pulse Input

5.4. Interlock Function

The Motion SPM® 7 series interlock function prevents shoot-through phenomena when high- and low-side input, HIN and LIN, are placed in HIGH status at the same time.

The first input signal has priority to prevent shoot-through. Table 7 and Figure 31 show the behavior of the interlock function based on one-leg diagram of SPM, Figure 30.

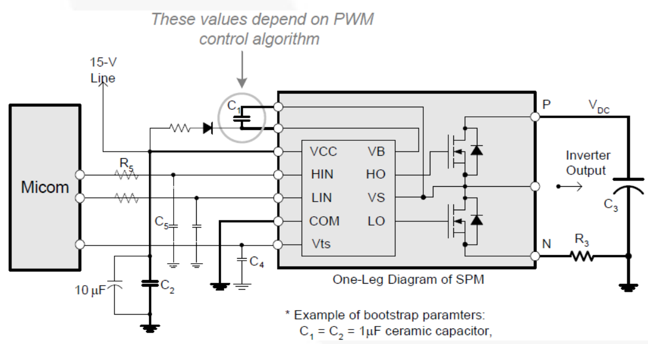


Figure 30. One-Leg Diagram of Motion SPM® 7 Series

Table 7. Logic Table for Inverter Output

HIN	LIN	Output	Status
0	0	Z	Both MOSFETs OFF
0	1	0	Low-Side MOSFET ON
1	0	V_{DC}	High-Side MOSFET ON
1	1	Forbidden	Interlock *(refer to Figure 31)*
Open	Open	Z	Same as (0,0)

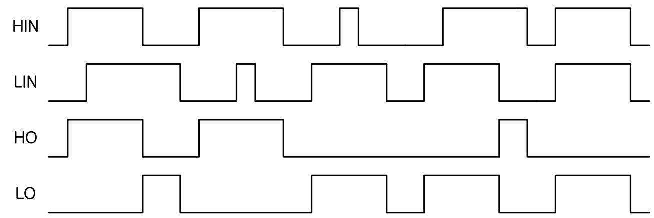


Figure 31. Timing for the Input and Output of HVIC

5.5. Selection of CFOD

The external capacitor connected between the C_{FOD} and COM pins determines the Time of the Fault Output Duration (t_{FOD}). The t_{FOD} can be calculated by the following approximate equation:

$$t_{FOD} = C_{FOD} / (24 \times 10\text{-}6)\ [s] \quad (14)$$

5.6. Short Circuit Test

Motion SPM 7 series has MOSFET and behaves much more ruggedly than IGBT-based modules when short circuit situations occur. Figure 32 is the test circuit used to measure short circuit withstanding time and the definitions of the terms used in the measurement. The low-side MOSFET is shorted with a wire and the high-side device is turned on.

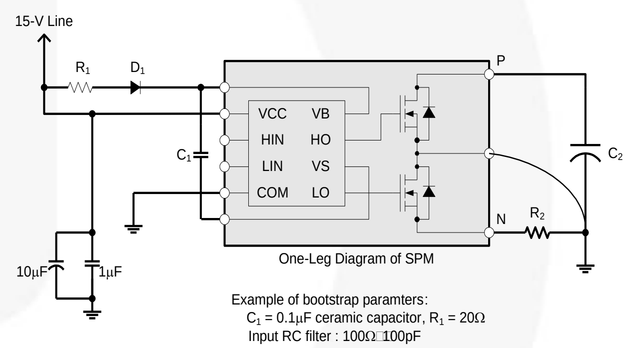
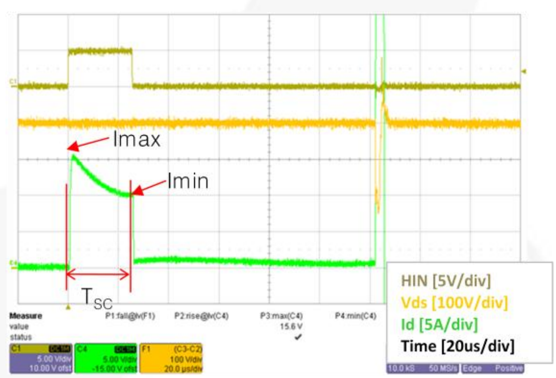


Figure 32. Short Circuit Withstanding Time Test Circuit



T_J [°C]	V_{DC} [V]	V_{DD} [V]	I_{MAX} [A]	I_{MIN} [A]	T_{SC} [µs]
150.0	400.0	20.0	15.6	10.0	25.0

Figure 33. SCWT of FSB70250 at Worst Condition

Figure 33 is a waveform of the FSB70250 at a short-circuit condition of V_{DC}=400 V, V_{DD}=V_{BS}=20 V, T_C=T_J=150°C. Even in this extreme condition, the FSB70250 demonstrates short-circuit withstand time (t_{SC}) longer than IGBT modules.

6 Application Example

6.1. General Application Circuit Examples

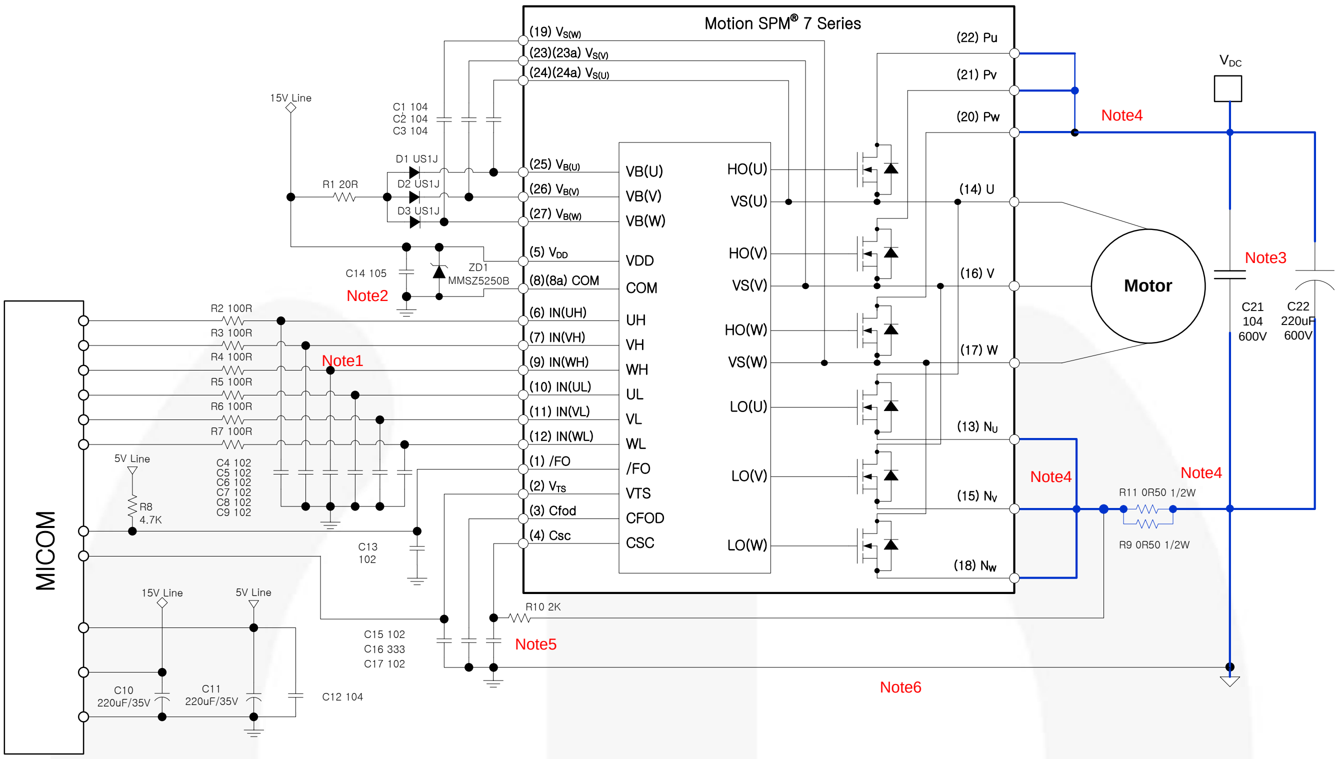


Figure 34. Example of Application Circuit

Notes:

1. Shorter traces are desired between the microprocessor and the power module. If necessary, RC filters can be employed on gate signals to suppress noise coupled from power traces and remove very narrow pulses. RC values should be selected for input signals to be compatible with the turn-on and turn-off threshold voltages. Keep in mind that this RC filter may alter the timing of PWM and the resulted volt-second.
2. Each HVIC needs to have an 1 µF cermaic capacitor close to V_{DD} pin and possibly to Com pin to supply instantaneous power. An electrolytic capacitor of 10 µF is required as well to supply stable V_{DD} voltage to the module. A Zener diode can be used in parallel to make sure V_{DD} does not increase beyond certain voltage at surge events.
3. A high frequency non-inductive capacitor of around 0.1~0.22 µF, C21, should be placed very close to the module and between P and the ground side of the shunt resistor R9 and R11.
4. PCB traces for the main power paths between DC bus capacitor C22 and the module should be as short as possible to minimize the noise associated with the parasitic inductance. These traces are colored in blue.
5. The current feedback trace should be connected directly from the shunt resistor (Kelvin connection) to get a clean and undistorted signal.
6. Power ground and signal ground need to be connected at a single point to prevent noise from the power to interfere with control signals.

6.2. Recommended Wiring of Shunt Resistor

External current-sensing resistors are applied to detect phase current. A longer pattern between the shunt resistor and SPM pins causes large surge voltages that might damage the IC and distort the sensing signals. To decrease the pattern inductance, the wiring between the shunt resistor and SPM pins should be as short as possible. Parasitic impedance between the shunt resistor and the power module pins should be less than 10 nH, which results from a trace in 3 mm width, 20 mm length, and 1 oz thickness.

6.3. Snubber Capacitor

As shown in Figure 35, snubber capacitors should be located to suppress surge voltages effectively. Generally a 0.1∼0.22 µF snubber capacitor is recommended. If the snubber capacitor is installed in location ‘A’ in Figure 35, it cannot suppress the surge voltage effectively because of parasitic impedance of the traces between the capacitor and the module. If the capacitor is installed in the location ‘B’, surge suppression is most effective because the snubber capacitor is connected right at the module power pins. However, in a single shunt resistor is used for phase current reconstruction or over-current protection, the voltage across the shunt resistor cannot correctly reflect the DC bus current information consumed by the module and, therefore, the current feedback signal is distorted. The ‘C’ position is a reasonable compromise with better suppression than in location ‘A’ without impacting the current sensing signal accuracy. For this reason, the location ‘C’ is generally used.

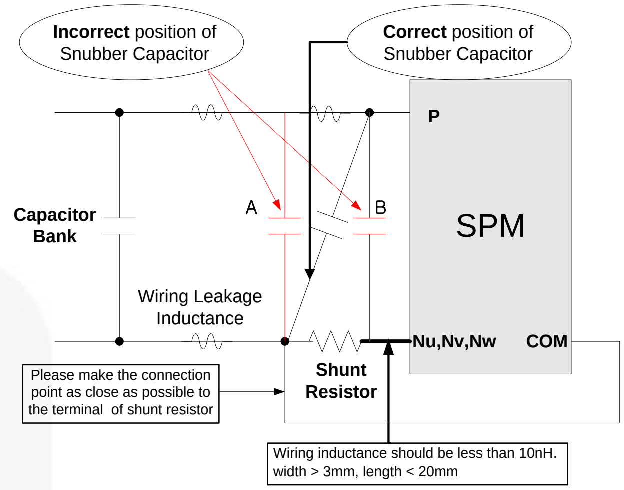


Figure 35. Recommended Wiring of Shunt Resistor and Snubber Capacitor

6.4. PCB Layout Guidance

Figure 36 shows the PCB layout of *the* test board. *Figure 37* shows the actual test board. The compact size of Motion SPM 7 series is the key to overcome the mechanical challenge in this type of design. *More detailed guideline can be found in* [*RD-356*](RD-356).

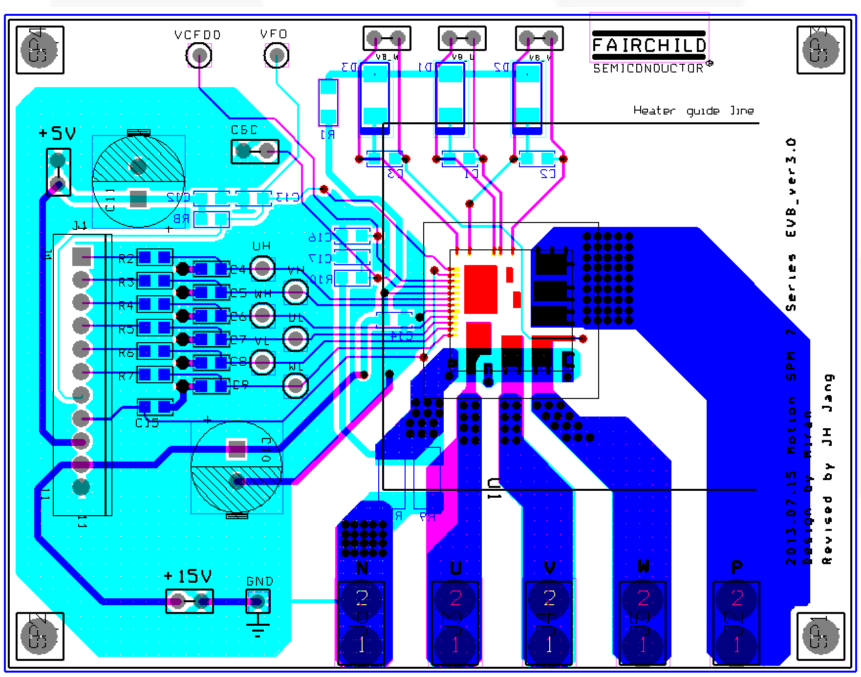


Figure 36. PCB Layout Example

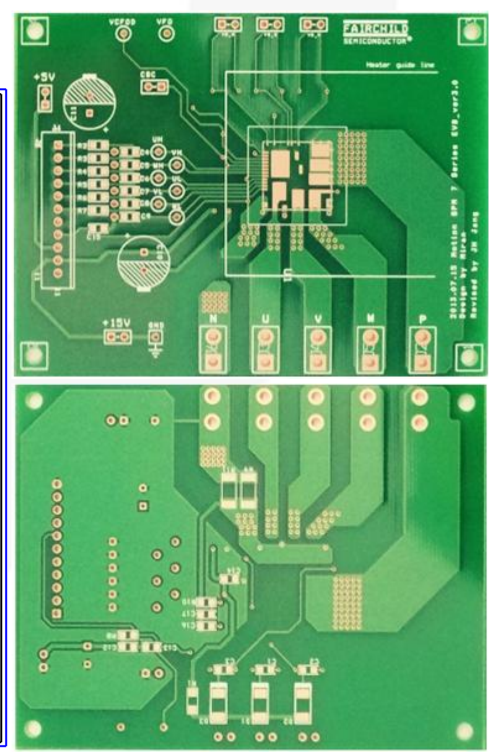


Figure 37. Test Board

6.5. Thermal Characteristics

Figure 38 shows thermal equivalent circuit of an Motion SPM 7 series with heat sink placed on the bottom side of the PCB. Even though heat sink is absent, the PCB plays a role as a heat sink. In this case, T_J can be calculated as:

$$T_J = P_D \times R_{\theta JCB} + T_{CB} \quad (15)$$

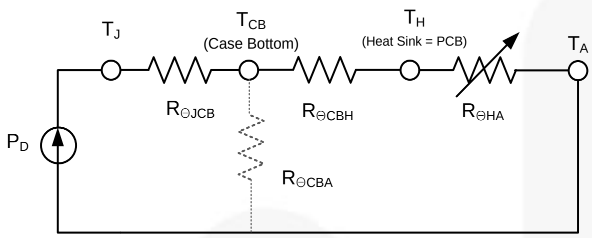


Figure 38. Thermal Equivalent Circuit with Heat Sink on Bottom-Side

6.6. Thermal Simulation

6.6.1 Condition for $R_{\theta JCB}$ and $R_{\theta JA}$

To investigate thermal characteristics of the Motion SPM 7 series, variable conditions should be considered. The following simulation results for $R_{\theta JCB}$ and $R_{\theta JA}$ adopt variable factors with test board, solder void, and PCB pattern.

General description for the thermal test board specification is as shown in Table 8.

Table 8. Specification for Thermal Test Board

Class	Thermal Test Board Specification
Overall Size	114.3 * 76.2 * 1.6 mm^3
Trace Width	0.25 mm ±10% for ≥ 0.5 mm Pin Pitch; lead width for < 0.5 mm Pin Pitch
Trace Thickness	Signal: 2 oz (0.07 mm ±20%), Power/Ground: 1 oz (0.035 mm +0/-20%)
Buried Plane Size	74 x 74 mm^2
Trace Pitch (via spacing)	2.54 mm
Fan Out Trace Length	Min. 25 mm
Remarks	PKG Length <27 mm

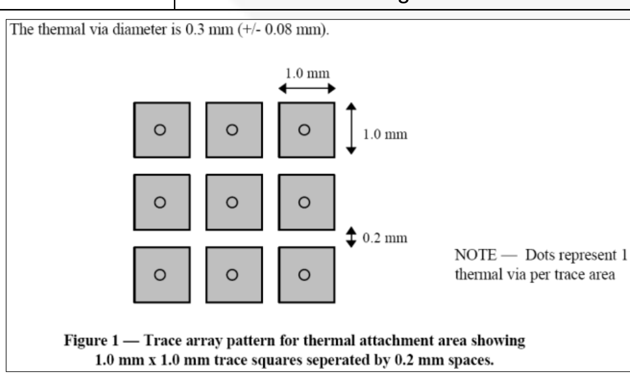


Figure 39. Trace Array Pattern for Thermal Attachment

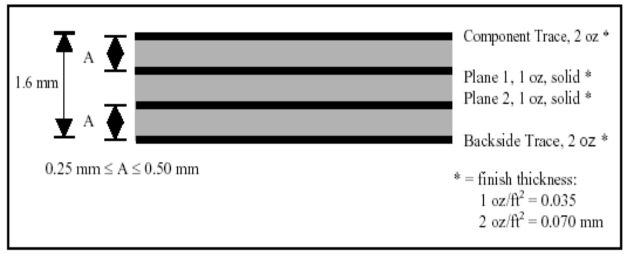


Figure 40. Vertical Structure of Trace

6.6.2 Simulation for $R_{\theta JCB}$

The analysis model and boundary conditions for $R_{\theta JCB}$ are:

- Three-dimensional model, steady-state analysis
- Flow, heat transfer, and radiation solution
- Simplified model
- Based on Mil Std 883C Method 1012.; Thermal Characteristics of Microelectronic Devices

Figure 41 shows the modeling for $R_{\theta JCB}$ with ideal condition with infinite cooling.

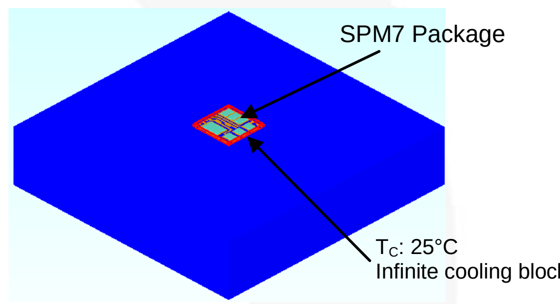


Figure 41. Modeling for $R_{\theta JCB}$

Table 9 and Table 10 show analysis results for the simulation. The portion of the solder void is 0 ~ 20% of the chip size.

Table 9. Solder Void vs. $R_{\theta JCB}$ at 1 Chip Heating

Solder Void	$R_{\theta JCB}$ at 1 Chip Heating [°C/W]		
	Low-Side	High-Side	HVIC
Void Free	1.073	1.073	0.386
2%	1.225	1.224	0.513
4%	1.358	1.354	0.617
6%	1.476	1.475	0.704
8%	1.596	1.592	0.804
10%	1.722	1.732	0.895
12%	1.826	1.824	0.979
14%	1.956	1.964	1.052
16%	2.044	2.036	1.149
18%	2.182	2.180	1.225
20%	2.316	2.312	

Table 10. Solder Void vs. $R_{\theta JCB}$ at Total Chip Heating

Solder Void	$R_{\theta JCB}$ at Total Chip Heating [°C/W]		
	Low-Side	High-Side	HVIC
Void Free	1.073	1.074	0.386
2%	1.225	1.226	0.513
4%	1.359	1.354	0.617
6%	1.476	1.477	0.702
8%	1.596	1.594	0.801
10%	1.722	1.736	0.895
12%	1.828	1.830	0.977
14%	1.958	1.970	1.049
16%	2.046	2.040	1.145
18%	2.184	2.184	1.220
20%	2.318	2.318	1.307

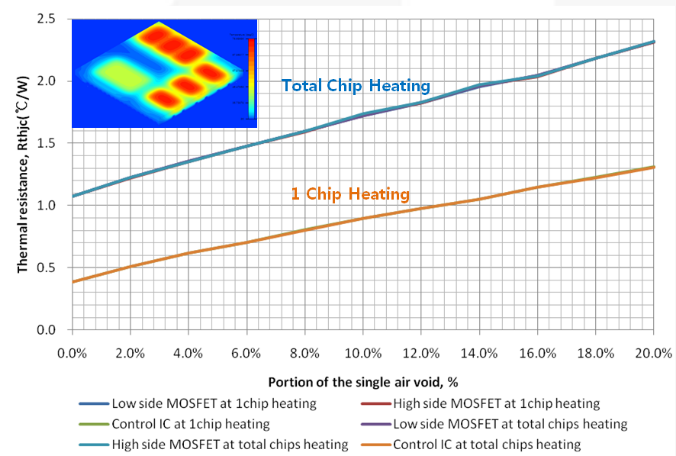


Figure 42. Solder Void vs. $R_{\theta JCB}$

6.6.3 Simulation for $R_{\theta JA}$

The SPM7 is mounted on the PCB specified in JEDEC to simulate $R_{\theta JA}$. The Analysis model and boundary conditions for $R_{\theta JA}$ are:

- Three-dimensional model, steady-state analysis
- Flow, heat transfer, and radiation solution
- Simplified model
- Based on JEDEC 51-2, integrated circuits thermal test method environment conditions - natural convection (still air)
- Various thermal test board options:
  - 1s0p (one signal layer and zero power layer) with copper plane (minimum and 74mm^2 land pattern per MOSFET, JESD51-3)
  - 1s2p (one signal layer and two power layers) with copper plane (minimum and 74mm^2 land pattern per MOSFET, JESD51-7)

Figure 43 and Figure 44 show the dimensions of the thermal test board.

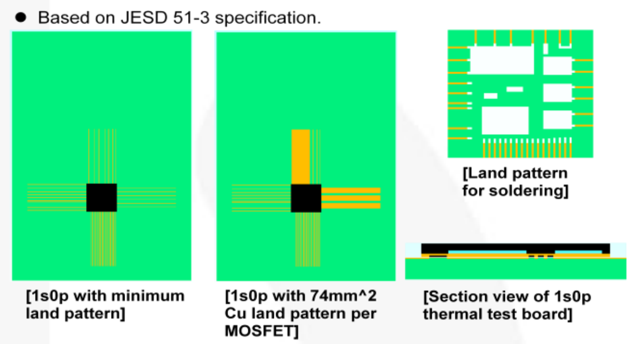


Figure 43. Thermal Test Board (JESD51-3)

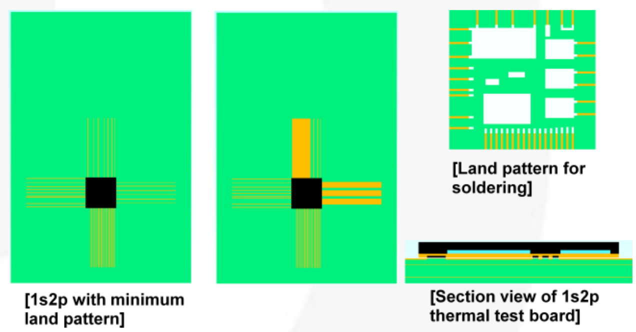


Figure 44. Thermal Test Board (JESD51-7)

Table 11. Solder Void vs. $R_{\theta JA}$ at 1s0p PCB

Solder Void	$R_{\theta JA}$ at 1s0p PCB with Min. Cu Trace Pattern at Total Chip Heating (CASE1) [°C/W]			$R_{\theta JA}$ at 1s0p PCB with 74 mm^2 Cu Trace Pattern for MOSFET at Total Chip Heating (CASE2) [°C/W]		
	Low-Side	High-Side	HVIC	Low-Side	High-Side	HVIC
Void Free	253.1	281.5	1441.7	183.9	199.0	1423.7
4%	253.1	281.7	1441.6	183.9	199.0	1423.7
10%	253.2	282.1	1441.6	183.9	199.3	1423.7
14%	253.4	282.3	1441.6	184.1	199.6	1423.6
20%	253.7	282.5	1441.6	184.4	199.8	1423.6

Table 12. Solder Void vs. $R_{\theta JA}$ at 1s2p PCB

Solder Void	$R_{\theta JA}$ at 1s2p PCB with Min. Cu Trace Pattern at Total Chip Heating (CASE3) [°C/W]			$R_{\theta JA}$ at 1s2p PCB with 74 mm^2 Cu Trace Pattern for MOSFET at Total Chip Heating (CASE4) [°C/W]		
	Low-Side	High-Side	HVIC	Low-Side	High-Side	HVIC
Void Free	112.0	118.6	1390.8	92.8	96.8	1549.6
4%	112.3	118.8	1390.8	92.8	96.8	1549.6
10%	112.6	119.2	1390.8	93.2	97.1	1549.6
14%	112.8	119.4	1390.8	93.4	97.3	1549.6
20%	113.1	119.6	1390.8	93.7	97.5	1549.6

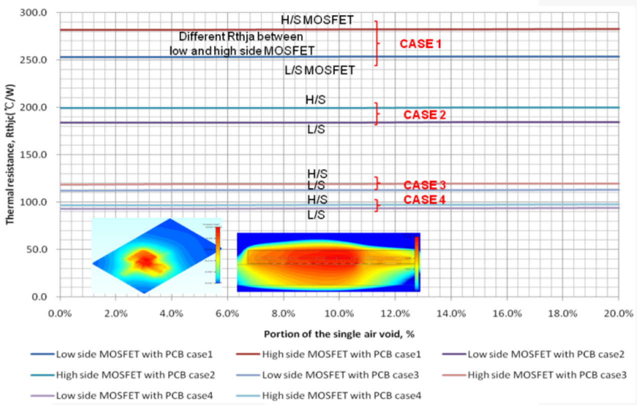


Figure 45. Solder Void vs. $R_{\theta JA}$

As shown in the simulation results, the epoxy void does not seem to be a significant risk factor for thermal performance of SPM 7 series. In simulation, the portion of increasing $R_{\theta JA}$ caused by epoxy solder void is smaller than total $R_{\theta JA}$ value. In real evaluation, the effect solder void is observed as shown in Figure 45.

Additionally, it is observed that narrow width of the copper pattern leads to increasing $R_{\theta JA}$. The $R_{\theta JA}$ difference between high- and low-side MOSFET is absorbed.

6.7. Evaluation Test

The condition of the evaluation test is the following:

- V_{DC} = 300 V, V_{DD} = V_{BS} = 15 V, f_{SW} = 16.6 kHz
- PWM method: SVPWM
- Output current = 0.3/0.4/0.5 Arms
- No heat sink
- Test board: FR4, 2 layer, 1 oz & 2 oz.

Figure 46 and Figure 47 show the layout of the test board.

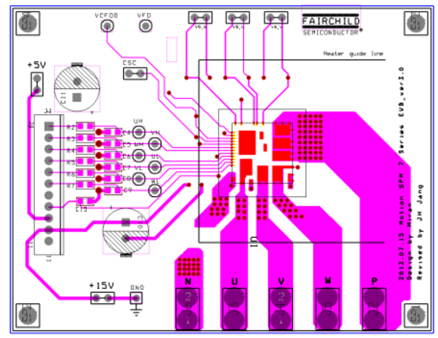


Figure 46. Top Side of the Test Board

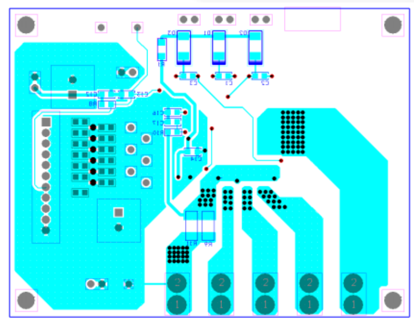


Figure 47. Bottom Side of the Test Board

Figure 48 shows the test bench of the evaluation test.

The top of the case temperature was measured by an infrared camera to evaluate the effect of copper thickness and solder void.

As shown in the Table 13, increasing the thickness of the copper pattern can decrease the temperature of the case because it can reduce the thermal resistance.

As shown in Table 14, increasing solder void can increase the temperature of the case slightly.

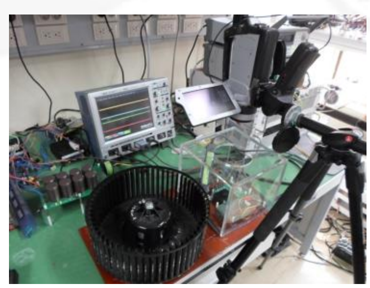
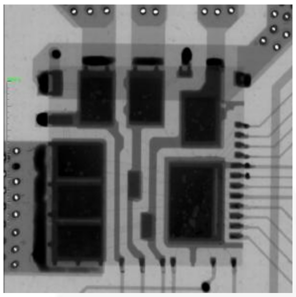
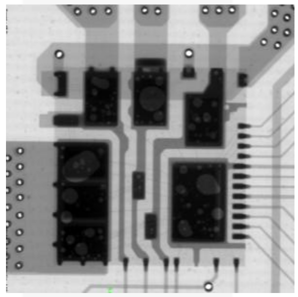
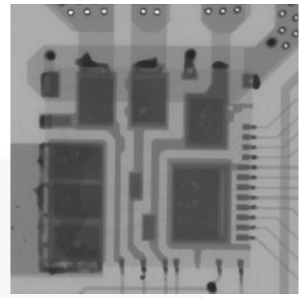
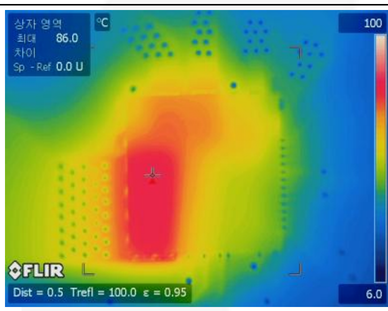
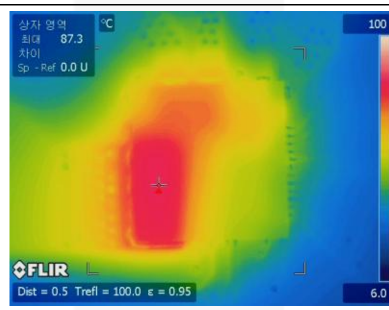
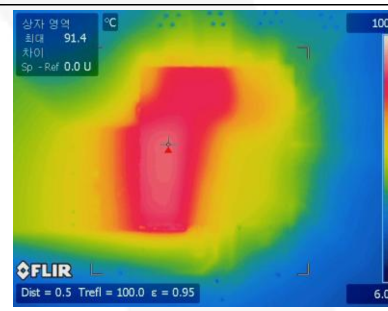


Figure 48. Test Bench

Table 13. Effect of Cu Thickness

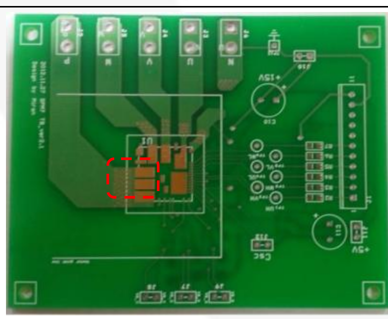
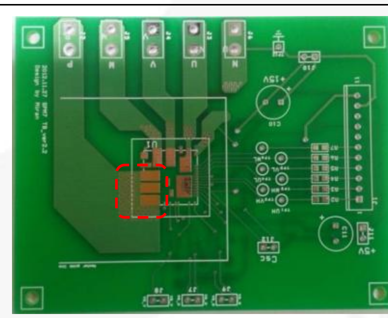
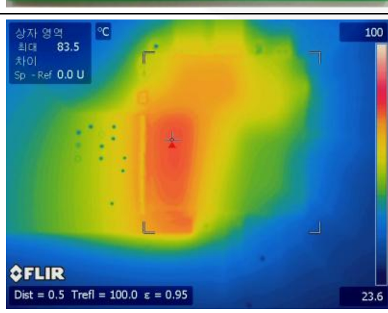
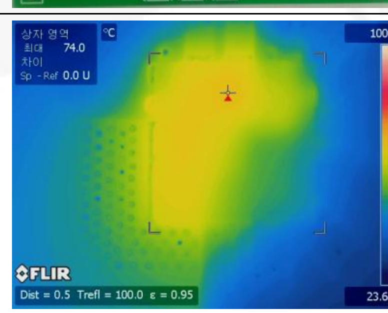
Copper Thickness	0.3 Arms	0.4 Arms	0.5 Arms
1 oz	69.2°C	91.5°C	
2 oz	58.8°C	75.3°C	100°C

Table 14. Effect of Solder Void at I_{rms} = 400 mA, 1 oz, T_A=21°C

Small Void (<15%)	Large Void (15~35%)	Worst Case (>90%)
86°C	87.3°C	91.4°C
		
		

As shown in Table 15, increasing the area of copper pattern for P (positive DC bus) decreases the temperature of the case because it reduces the thermal resistance.

Table 15. Effect of Pattern width at I_{rms} = 400 mA, 1 oz, T_A=21°C

Narrow Width (10 mm)	Wide Width (20 mm)
83.5°C	74°C
	
	

6.8. System Performance

A fan motor for an indoor air-conditioner unit has been tested to provide comparison data between the Motion SPM 7 Series and competition products.

Figure 49 illustrates the power loss of a single power device, such as MOSFET or IGBT. Under the same operating conditions, the FSB70550 shows the lowest conduction loss and switching loss compared to competitive products. Low power loss means better energy efficiency in the system.

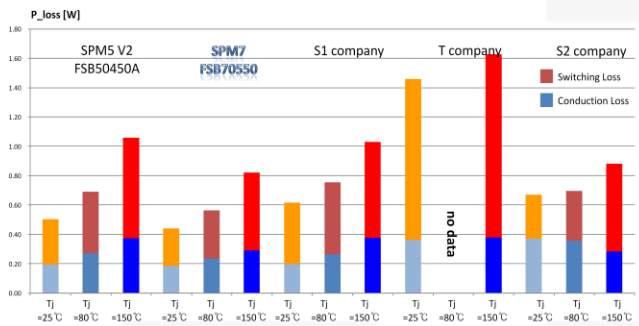


Figure 49. Single MOSFET/IGBT Power Loss Comparison (Simulation Condition: V_{DC}=300 V, V_{DD}=15 V, f_{SW}=16.6 kHz, SVPWM, M_I=0.8, PF=0.9, I_O=500 mArms)

Figure 50 shows the test bench set up and the case temperature comparison. Under the same operating conditions, the FSB70550 shows outstanding thermal performance compared to competitive parts.

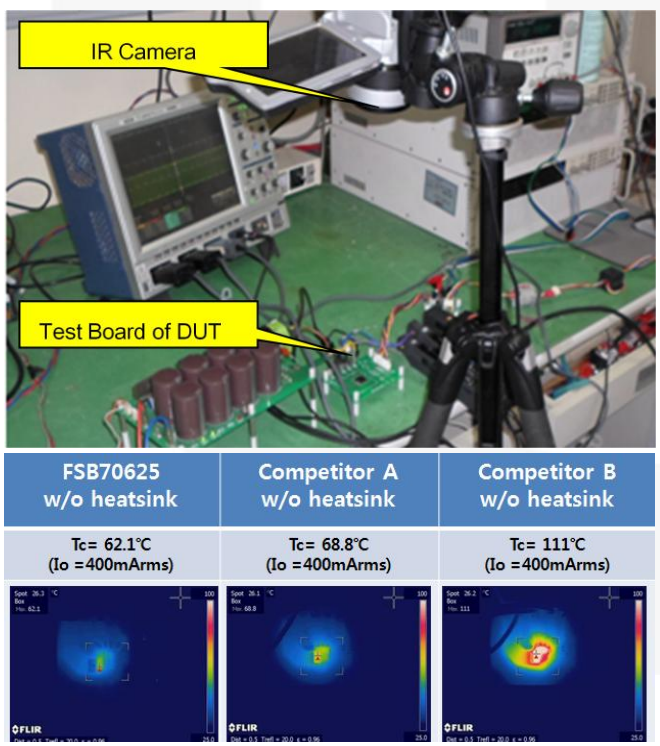


Figure 50. Case Temperature Comparison of Motion SPM 7 Series and Competitors (Test Conditions: V_{DC} = 150 V, V_{DD} = 15 V, f_{SW} = 20 kHz, PWM Method = SVPWM, DT=2 µs, Servo Motor)

7 Packing and Installation Guide

7.1. Handling Precautions

When using semiconductors, the incidence of thermal and/or mechanical stress to the devices due to improper handling may result in significant deterioration of electrical characteristics and/or reliability.

7.1.1 Transportation

Handle the device and packaging material with care. To avoid damage to the device, do not toss or drop. During transport, ensure that the device is not subjected to mechanical vibration or shock. Avoid getting devices wet. Moisture can also adversely affect the packaging (by nullifying the effect of the antistatic agent). Place the devices in conductive trays. When handling devices, hold the package and avoid touching the leads, especially the gate terminal. Put package boxes in the correct direction. Putting them upside down, leaning them, or giving them uneven stress can cause the electrode terminals to be deformed or the resin case to be damaged. Throwing or dropping the boxes can cause the devices to be damaged. Wetting the packaging boxes can cause breakdown of devices when operating. Pay attention not to wet them when transporting on a rainy or a snowy day.

7.1.2 Storage

Avoid locations where devices may be exposed to moisture or direct sunlight. (Be especially careful during periods of rain or snow).

Do not place the device cartons upside down. Stack the cartons on top of one another in an upright position only. Do not place cartons on their sides.

The storage area temperature should be maintained within a range of 5°C to 35°C, with humidity kept within the range from 40% to 75%.

Do not store devices in the presence of harmful (especially corrosive) gases or in dusty conditions.

Ensure storage areas have minimal temperature fluctuation. Rapid temperature changes can cause moisture condensation on stored devices, resulting in lead oxidation or corrosion. As a result, lead solderability is degraded.

When repacking devices, use antistatic containers. Unused devices should be stored no longer than one month.

Do not allow external forces or loads to be applied to the devices while in storage.

7.1.3 Environment

Be aware of the risk of moisture absorption by the products after unpacking from moisture-proof packaging.

As humidity in the work environment decreases, the human body and other insulators become charged with electrostatic electricity due to friction. Maintain the recommended humidity of 40% to 60% in the work environment.

Be sure that all equipment, jigs, and tools in the working area are grounded to earth.

Place a conductive mat on the work area floor, or take other appropriate measures, so the floor surface is grounded to earth and protected against electrostatic electricity.

Cover the workbench surface with a conductive mat, grounded to earth, to disperse electrostatic electricity on the surface through resistive components. Workbench surfaces must not be constructed of low-resistance metallic material that allows rapid static discharge when a charged device touches it directly.

Ensure that work chairs are protected with an antistatic textile cover and are grounded to the floor surface with a grounding chain.

Install antistatic mats on storage shelf surfaces.

For transport and temporary storage of devices, use containers made of antistatic materials or materials that dissipate static electricity.

Ensure that cart surfaces that come into contact with device packaging are made of materials that conduct static electricity and are grounded to the floor surface with a grounding chain.

Operators must wear antistatic clothing and conductive shoes (or a leg or heel strap).

Operators must wear a wrist strap grounded to earth through a resistor of about 1 MΩ.

If tweezers are likely to touch the device terminals, use an antistatic type and avoid metallic tweezers. If a charged device touches such a low-resistance tool, a rapid discharge can occur. When using vacuum tweezers, attach a conductive chucking pad at the tip and connect it to a dedicated ground used expressly for antistatic purposes.

When storing device-mounted circuit boards, use a board container or bag protected against static charge. To prevent static charge/discharge due to friction, keep them separated and do not stack them directly on top of one another.

Ensure that articles (such as clipboards) brought into static electricity control areas are constructed of antistatic materials as far as possible.

In cases where the human body comes into direct contact with a device, be sure to wear finger cots or gloves protected against static electricity.

7.1.4 Electrical Shock

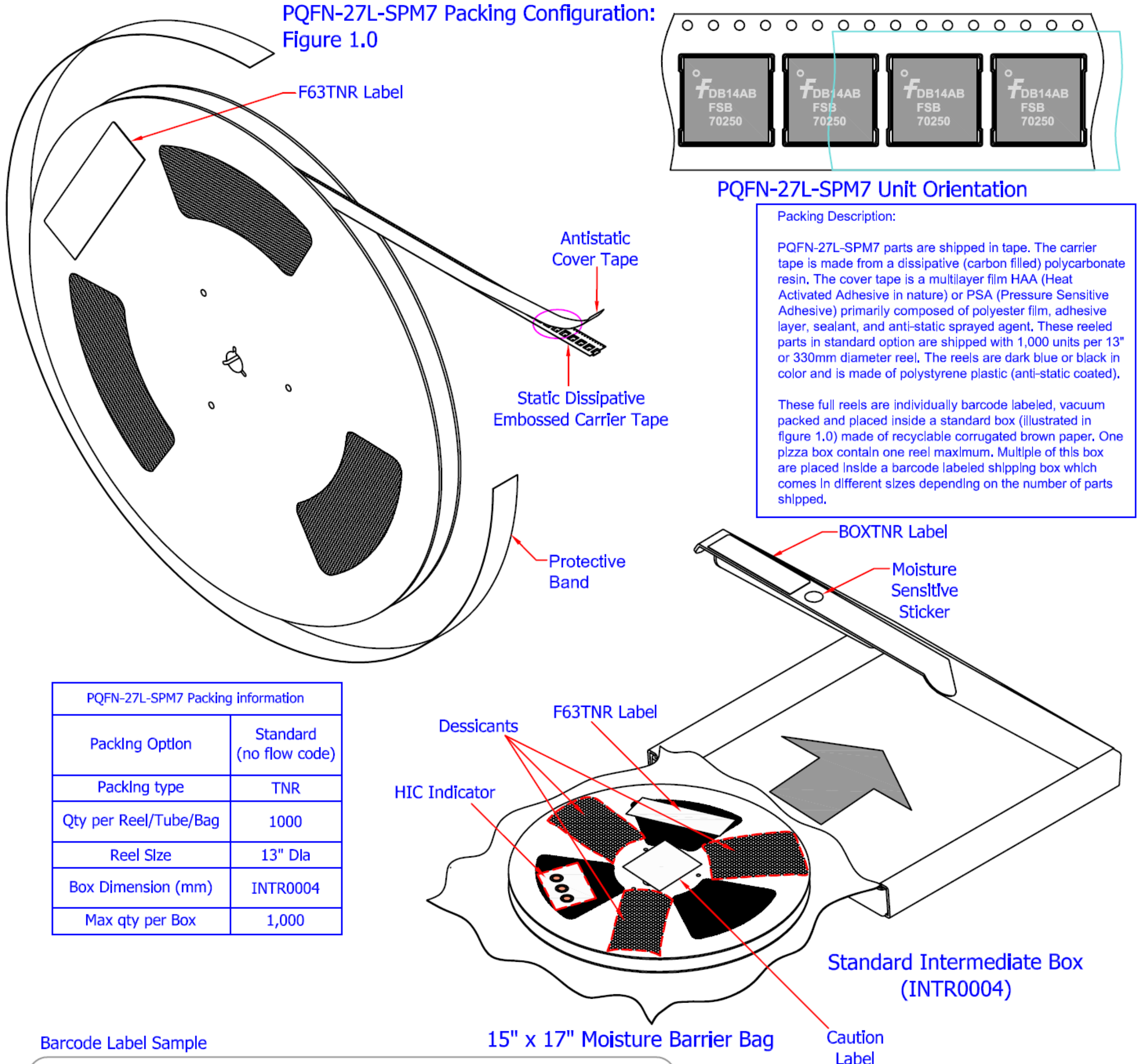
A device undergoing electrical measurement poses the danger of electrical shock. Do not touch a device unless sure that power to the measuring instrument is OFF.

7.1.5 Circuit Board Coating

When using devices in equipment requiring high reliability or in extreme environments (where moisture, corrosive gas, or dust is present), circuit boards can be coated for protection. However, before doing so, carefully examine the possible effects of stress and contamination that may result. There are many and varied types of coating resins whose selection is, in most cases, based on experience. However, because device-mounted circuit boards are used in various ways, factors such as board size, board thickness, and the effects that components have on one another, makes it practically impossible to predict the thermal and mechanical stresses that semiconductor devices encounter.

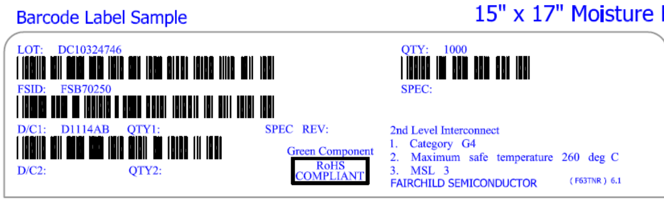
8 Packing Specification

Motion SPM 7 series is shipped in tape. More detailed information can be found in Figure 51.

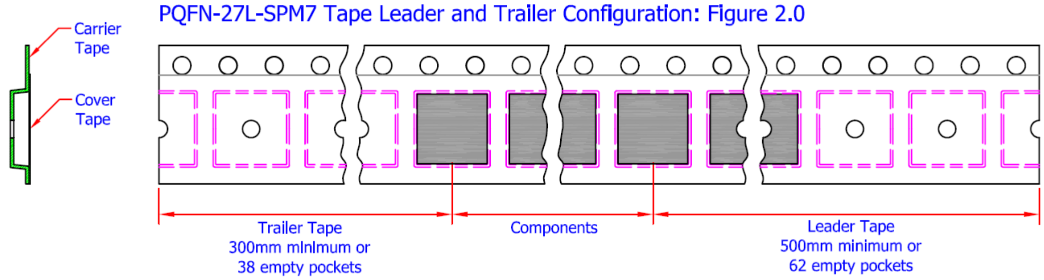


PQFN-27L-SPM7 Packing information	
Packing Option	Standard (no flow code)
Packing type	TNR
Qty per Reel/Tube/Bag	1000
Reel Size	13" Dia
Box Dimension (mm)	INTR0004
Max qty per Box	1,000

Barcode Label Sample



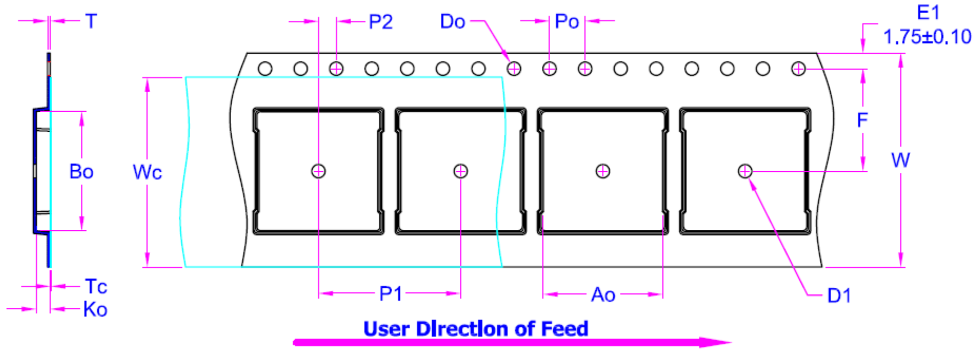
PQFN-27L-SPM7 Tape Leader and Trailer Configuration: Figure 2.0



NOTES:

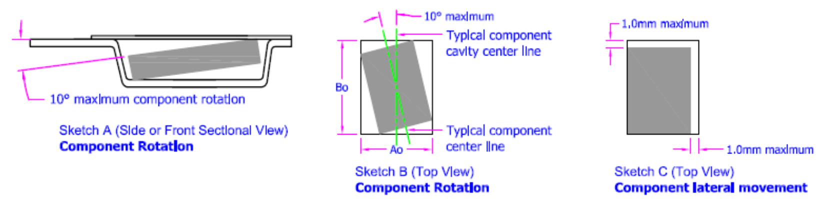
A. ALL DIMENSIONS ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED
B. DRAWING FILENAME: PKG-PQFN27AREV1

PQFN-27L-SPM7 Embossed Carrier Tape Configuration: Figure 3.0

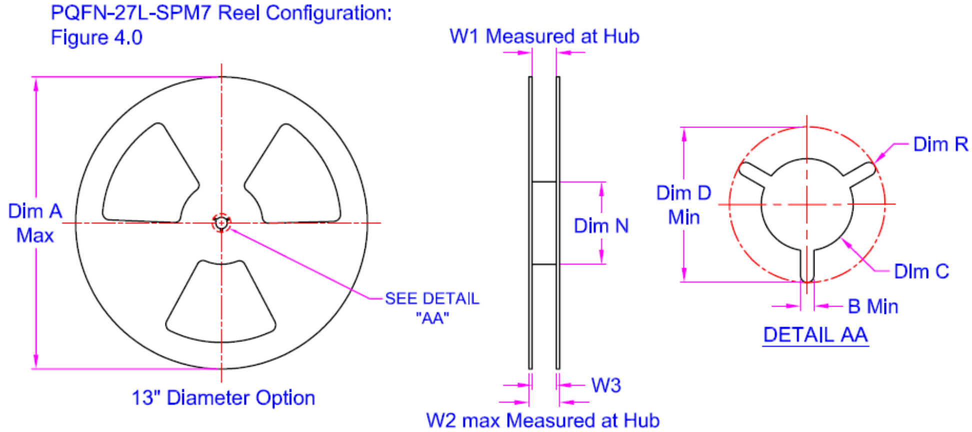


Dimensions are in millimeters															
Pkg type	Ao	Bo	W	Do	D1	E1	F	P1	P2	Po	Ko	K1	T	Wc	Tc
PQFN-27L-SPM7	13.40 ±0.10	13.40 ±0.10	24.00 +0.20 -0.10	1.50 +0.10 -0.00	1.50 Min	1.75 ±0.10	11.50 ±0.10	16.00 ±0.10	2.00 ±0.10	4.00 ±0.10	1.60 ±0.10	2.70 ±0.10	0.30 ±0.05	21.30 ±0.10	0.05 ±0.01

Notes: Ao, Bo, and Ko dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C). Camber requirement is also compliant to above mentioned standards.



PQFN-27L-SPM7 Reel Configuration: Figure 4.0



Dimensions are in millimeters										
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim R	Dim W1	Dim W2	Dim W3 (LSL-USL)
24mm	13" Dia	330	2.0	13+0.5/-0.2	20.8	100	0.5B	24.4+2/-0	28.44	23.9-27.4

NOTES:

A. ALL DIMENSION ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED
B. DRAWING FILE NAME: PKG-PQFN27AREV2
C. PLASTIC REEL W1 DIMENSION CONTROL LIMIT OF; 8MM REEL = ±1.0MM AND 12MM REEL AND ABOVE = ±1.5MM

Figure 51. Packing Information

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:
http://www.fairchildsemi.com/dwg/PQ/PQFN27A.pdf

For current packing container specifications, visit Fairchild Semiconductor's online packaging area:
http://www.fairchildsemi.com/packing_dwg/PKG-PQFN27A.pdf

9 Related Resources

AN-9078 — Surface Mount Guidelines for Motion SPM® 7 Series

RD-356 — Fairchild Motion SPM® 7 Series Reference Design

FSB70325 — Motion SPM® 7 Series

FSB70625 — Motion SPM® 7 Series

FSB70250 — Motion SPM® 7 Series

FSB70450 — Motion SPM® 7 Series

FSB70550 — Motion SPM® 7 Series

SPM® Module Design Guide

Motion Control Design Tool

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