

# High Speed Logic Compatible, Half-Pitch Mini-Flat Optocoupler, FODM8061

## AN-3012/D

### Introduction

The FODM8061, a high-speed, high noise immunity optocoupler, is constructed in a high insulation voltage SO5 mini-flat package. This optocoupler's optical input uses an aluminum gallium arsenide, AlGaAs, LED. The LED is coupled to a high-speed bipolar integrated logic compatible receiver. One major advantage of this product is that the high speed optical IC is specified with guaranteed performance at both 3.3 V and 5 V logic supplies. The optocoupler's open collector Schottky-clamped transistor output insures compatibility with a wide range of logic families. The optocoupler's key AC and DC characteristics are guaranteed over an operating temperature range of  $-40^{\circ}\text{C}$  to  $+110^{\circ}\text{C}$ .

This application note highlights the key electrical and switching performances of the high speed optocoupler, FODM8061. It also explores the data communication signal quality by examining the eye diagrams and the optocoupler's common usage in logic interfacing applications.

### The SO5 Mini-Flat Package Improves PCB Layout

The FODM8061 optocoupler is an enhanced version of the industry standard 6N137. The 6N137 optocoupler's package is an 8-pin dual in-line DIP leadform configuration. [Refer to the **onsemi** Optocoupler Selection Catalog for additional package selections.] The FODM8061's smaller SO5 package results in a more condensed PCB footprint. This small footprint enhances multi-channel packaging density without sacrificing channel-to-channel and input-to-output insulation safety. This is a primary consideration when isolation is needed for parallel and bidirectional data communication and logic interfacing.

This package utilizes **onsemi**'s patented "OPTOPLANAR<sup>®</sup>" co-planar packaging technology. This packaging technology enhances the superior common mode transient immunity of the shielded optical integrated receiver.

This package has received Underwriter's Laboratories 1577 (UL1577) safety approval for an insulation test voltage (VISO) of 3,750 Vac (RMS), and pending IEC60747-5-2 approval status. This mini-flat package is also compatible with  $260^{\circ}\text{C}$  surface mount solder reflow assembly processes.

### FODM8061's Electrical Operation

The FODM8061 is a two chip optical hybrid. The input chip is a high speed, low input current, infrared light

emitting diode, LED. The LED generates an optical flux in direct relationship to the LED's forward current,  $I_F$ . The LED's output is coupled to a high speed bipolar optical receiver through a low capacitance, "co-planar" optical coupling. The receiver IC converts the optical energy into electrical current and amplifies it to drive a load.

Figure 1 shows the block diagram of the FODM8061 optocoupler. The input consists of the anode and cathode of an IR LED. This LED has a typical forward voltage,  $V_F$ , of 1.45 V when the forward current,  $I_F$ , is 10 mA. The photo flux is coupled to a reverse-biased photodiode. The photodiode generates a photocurrent which flows from its anode into the bipolar amplifier. This linear amplifier has a typical current gain of 60 dB and a 40 MHz bandwidth. The output of this amplifier is a Schottky clamped open-collector NPN transistor. High levels of power supply and common mode power noise rejection is insured by including a bias and regulator circuit function. This circuit isolates the photodiode from power supply, common mode noise that can be coupled into the  $V_{CC}$ , and output of the optocoupler.

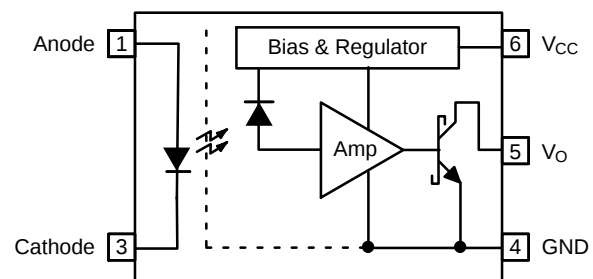


Figure 1. FODM8061 Block Diagram

This optocoupler functions as a logic inverter. A logic input signal which forces a forward current greater than 5 mA through the LED will cause the output transistor to sink current supplied by an external load. Table 1 illustrates the truth table for positive logic.

Table 1. TRUTH TABLE

| LED | Output |
|-----|--------|
| Off | High   |
| On  | Low    |

The “OPTOPLANAR” package increases the common mode noise rejection by reducing the package and common mode coupling capacitance,  $C_{CM}$ . The  $C_{CM}$  is further reduced by a proprietary electric shield that covers the receiver IC. The shield shunts common mode noise away from the input of the optical amplifier to the ground connection of the optical amplifier. This shield is shown as the dotted line between the LED and receiver IC. The combination of “OPTOPLANAR” construction and the electric shield provides a common mode transient immunity, CMTI, in excess of 20 kV/ $\mu$ s for a 1 kV pulse. More details are discussed in application note, “Common Mode Transient Immunity (CMTI) of High Performance Optocoupler”.

### Current Transfer Ratio

The FODM8061 is an optocoupler that includes a linear amplifier that drives the output transistor into saturation. Given this characteristic, it is appropriate to discuss current transfer ratio under non saturated and saturated  $V_{CE}$  conditions.

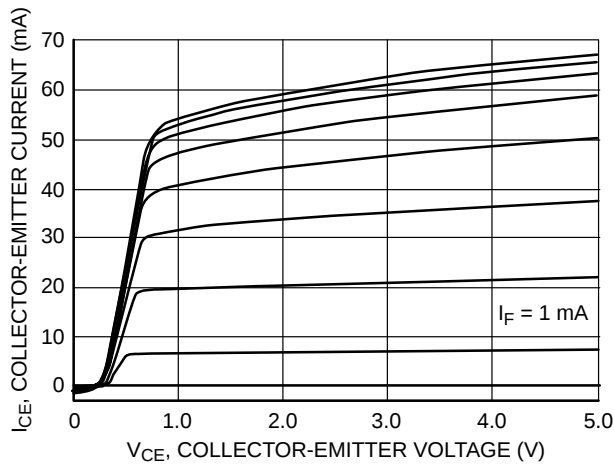


Figure 2.  $I_{CE}$  vs.  $V_{CE}$  Family,  $I_F = 1$  mA Steps

Figure 2 shows the family of collector-emitter current,  $I_{CE}$ , vs collector-emitter voltage,  $V_{CE}$ , as a function of LED forward current,  $I_F$ . The LED is stepped in 1 mA increments. Figure 2 shows the near linear operation for LED current operation from 1 mA through 4 mA. Figure 3 sweeps the LED current and shows the resulting collector current under the linear ( $V_{CE} = 1.5$  V, upper curve) and saturated ( $V_{CE} = 0.4$  V, lower curve) operation. Note that the output  $I_{CE}$  when in saturation ( $V_{CE} = 0.4$  V) is 8.05 mA with a LED current of 5 mA. The non saturated  $I_{CE}$  is 33 mA under the same LED drive. This difference in output current is a function of the output transistor, not the photo-amplifier.

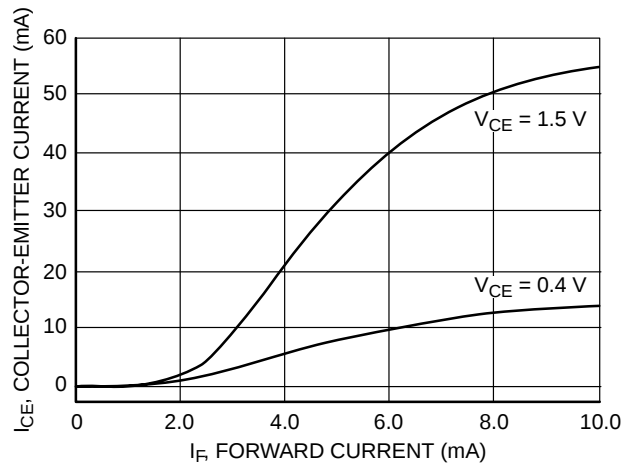


Figure 3. Saturated & Non-Saturated  $I_{CE}$  vs.  $I_F$

Figure 4 shows the saturated and non-saturated CTR for the FODM8061. This curve illustrates the consistency of the saturated CTR (approx 160%) over an LED forward current of 4 mA through 10 mA. This curve can be used to estimate the minimum LED current required to force a specific load into saturation at a given operating  $V_{CC}$ . The data sheet uses a 350  $\Omega$  collector load resistor for most of the switching specifications. If the  $V_{CC}$  is 3.3 V, then the saturated, ( $V_{CE} = 0.4$  V)  $I_{CE}$  is 8.3 mA for a 350  $\Omega$  load. The saturated CTR from Figure 4 is 160%. Recall that the LED current is equal to the  $I_{CE}$  divided by the CTR, or 8.3 mA/160%. Given this, the LED current should be 5.2 mA or greater to insure a logic level low at room temperature. When the  $V_{CC}$  is increased to 5 V and the same load is used, the LED current must be increased to insure saturated operation. With  $V_{CC} = 5$  V, the 350  $\Omega$  load current is 13 mA. Again, assuming a typical saturated CTR ( $V_{CE} = 0.4$  V) of 160%, the LED current should be 8.2 mA or greater.

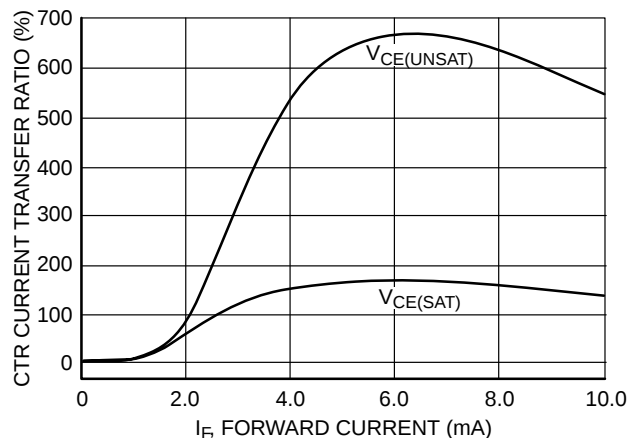


Figure 4. Saturated & Non-Saturated CTR

The data sheet offers a minimum CTR of 260% and a typical CTR of 380% for  $V_{CE} = 6$  V. This data is consistent with the expected CTR sensitivity to  $V_{CE}$  operation as presented in Figure 4.

### LED Forward Current Switching Threshold

The CTR of the FODM8061 can be discussed in terms of an LED threshold current. Figure 5 illustrates the required LED current for an  $I_{OL}$  of 10 mA, under the condition of  $V_{CC} = 3.3$  V (lower curve) and 5 V (upper curve). These curves illustrate that  $V_{CC}$  has a minor effect on the LED switching threshold.

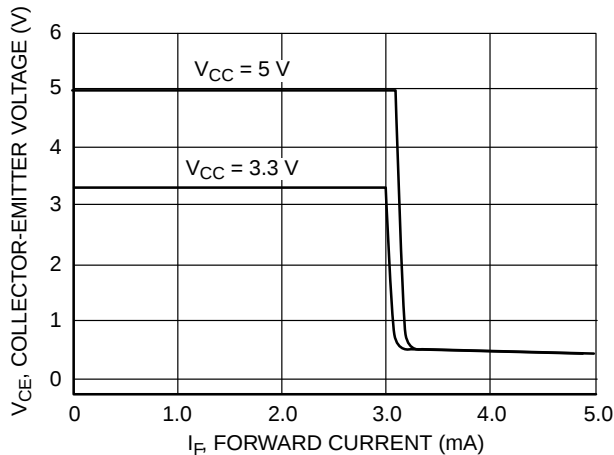


Figure 5. LED Threshold Current at  $V_{CC} = 3.3$  and 5 V

The threshold does have modest temperature dependence. This is shown in Figure 6.

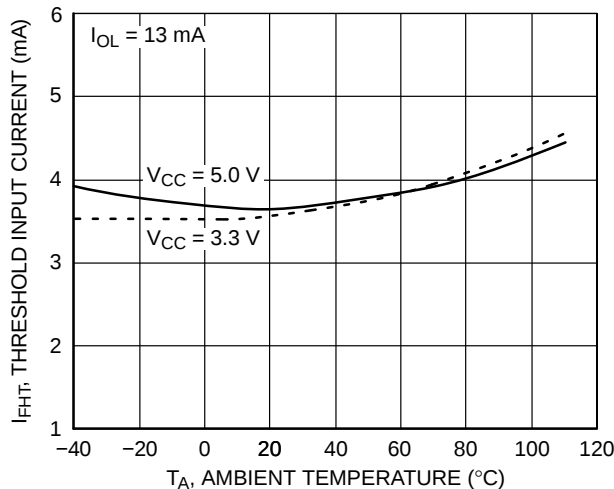


Figure 6. Input Threshold Current vs. Ambient Temperature

The LED's light output will decrease with increased junction temperature when driven by a constant drive current. The photo amplifier's DC gain increases with increased ambient temperature. In most cases, these two relationships are designed to cancel each other, as is the case for the FODM8061.

### Switching Performance

The FODM8061 is an optocoupler that contains a linear optical amplifier which is designed to function as an isolated logic inverter. The switching performance of the FODM8061 optocoupler is quantified in terms of propagation delay, pulse width distortion, and pulse skew.

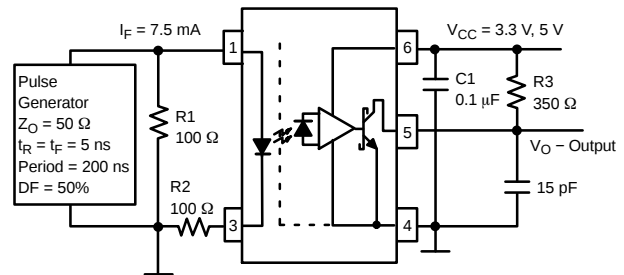


Figure 7. Switching Test Circuit

Propagation delay through this optocoupler is related to peak LED drive, power supply voltage, load resistor, and temperature. As shown in Figure 7, this device is optimized for operation with 7.5 mA of LED drive, a 5 V supply voltage, and a 350  $\Omega$  load resistor. Under this condition, a typical device offers a symmetrical high-to-low and low-to-high propagation delay of approximately 36 ns. Figure 8 shows the typical delay performance over the recommended operating temperature range of  $-40^{\circ}\text{C}$  to  $110^{\circ}\text{C}$ .

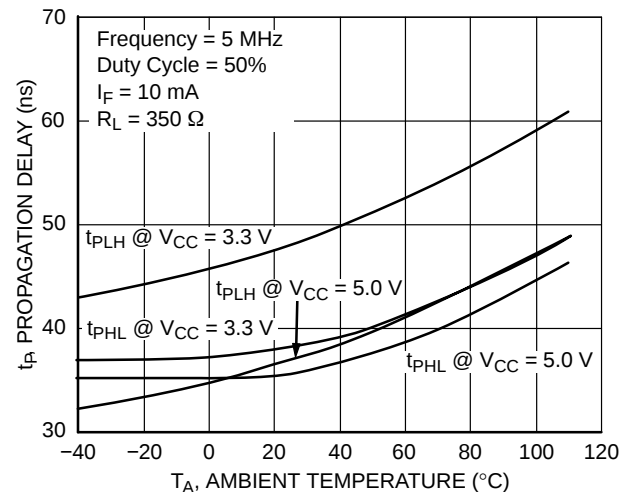


Figure 8. Propagation Delay vs. Temperature

Figure 9 provides insight on how the pulse width distortion changes with temperature. The typical pulse width distortion, PWD, [ $t_{PHL} - t_{PLH}$ ] is 2 ns. These performance characteristics allow high serial data (>20 Mbaud) communication through the optocoupler.

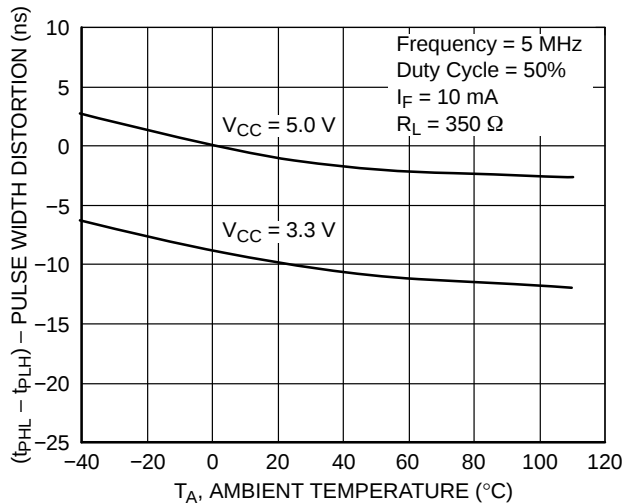


Figure 9. Pulse Width Distortion vs. Temperature

There are various assumptions which are made in relation of switching speed to baud rate, such as binary Non-Return-Zero (NRZ) data stream, 1 bit time equating 1 baud (or signaling rate) and a square wave pattern. Therefore, a 5 MHz square wave (duty factor of 50%) is a 10 Mbit or 10 MBaud signal.

For serial communications (RS standards), propagation delay only affects latency or data throughput. The maximum data rate is related to PWD performance and the number of samples per bit used by the UART to validate the 1 or 0 data. The minimum acceptable sample rate is 4, which is half the Nyquist recommended rate. Thus, the recommended maximum data rate is usually 4 times that of the PWD. In the case of FODM8061, with a maximum PWD of 25 ns the maximum data rate is 10 MBd.

Ideally, the delay skew,  $t_{PSK}$ , should be specified at about 2 times the maximum PWD. It is important to note that  $t_{PSK}$  is equal to the magnitude of the worst case difference in  $t_{PHL}$  and/or  $t_{PLH}$  that will be seen between any two units from the same manufacturing date code that are operated at same operating conditions; same case temperature, equal loads ( $R_L = 350 \Omega$  and  $C_L = 15$  pF), and with an input rise time less than 5 ns.

### Signal Performance

One of the best indicators of data communication signal quality is an eye diagram. The eye diagram is created by driving the LED with a pseudorandom binary data sequence,

PRBS, and triggering the scope with the serial data clock. Figure 10 shows a 10 MBd eye diagram using the test circuit found in Figure 7. This diagram shows a duty cycle distortion of only 2.18 ns. This is very close to the typical PWD of 2 ns. The LED current was adjusted for optimal crossing, under this condition, the rise and fall times are symmetrical and less than 20 ns.



Figure 10. 10 MBd Eye Diagram

Figure 11 illustrates the typical and respectable eye diagram for 20 MBd PRBS data.



Figure 11. 20 MBd Eye Diagram

### Output Power Consumption versus Propagation Delay

The passive resistive pull-up resistor does dissipate power when the output of the optocoupler is switched into the logic low state. Increasing the collector load resistor does reduce power consumption at the price of longer turn-off delay and larger pulse width distortion. Figure 12 shows the expected increase propagation delay from the logic low to logic high.

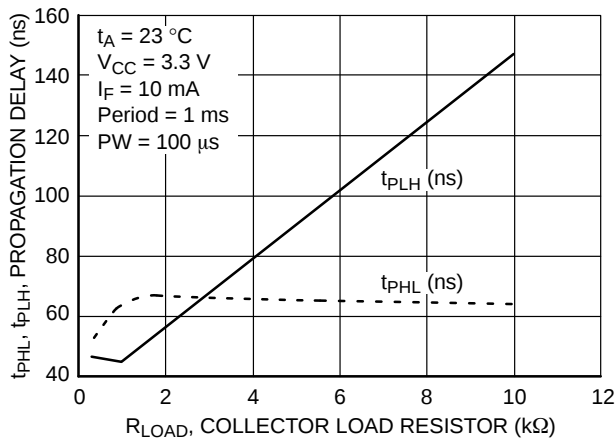


Figure 12. Propagation vs. Collector Load Resistor

### Logic Interfacing

The FODM8061 is a versatile logic-to-logic interface optocoupler. The low forward voltage of the LED permits operation among logic families with supply ranges from 2.3 V to 15 V. Figure 13 shows an inverting interface between a 3 V 74LCX07 open drain buffer to output logic families from 3.3 V to 5 V. The current to the LED is set by R1 (82 Ω) to approximately 10 mA. R2 (430 Ω) provides the pull-up needed by the open drain '07 gate.

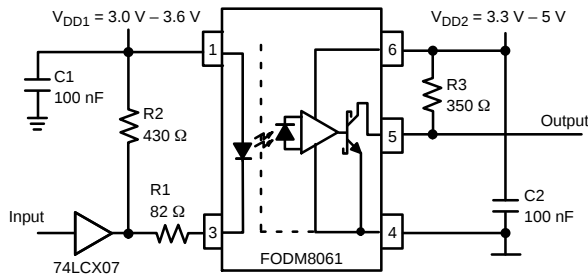


Figure 13. Inverting Series LED Drive

When a non-inverting interface is needed, the LED shunt drive is used. This circuit schematic is shown in Figure 14.

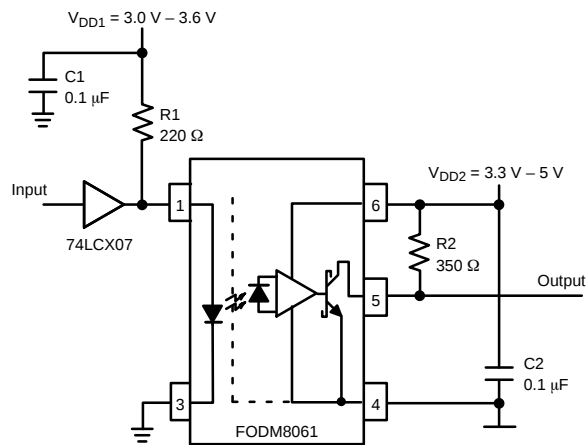


Figure 14. Non-inverting Logic Interface

The output transistor of the 74LCX07 shunts the drive current away from the LED when its output is forced low. This type of interface offers the lowest LED off-state impedance resulting in improved LED noise immunity.

### Interface Circuit for $V_{CC}$ Greater than 5.5 V

Industrial systems today still use the 15 V CD4xxx logic gates, which offer exceptional logic noise immunity, mainly due to their high switching thresholds and slow operating speed. When a low voltage high speed optocoupler is needed to interface into logic families with supply voltages greater than 5.5 V, a buffer transistor is needed. Figure 15 shows the use of a cascode amplifier interface, which uses an inexpensive bipolar 2N2222 NPN transistor with a Schottky "Baker Clamp". This circuit switches a 25 V load from a 25 V supply. The cascode circuit maintains the same logic sense as the original optocoupler interface and as Figure 16 shows the rise and fall times, and the propagation delays well under 100 ns. The 5 V supply voltage of the optocoupler can be supplied by a Zener diode, from a regulated supply.

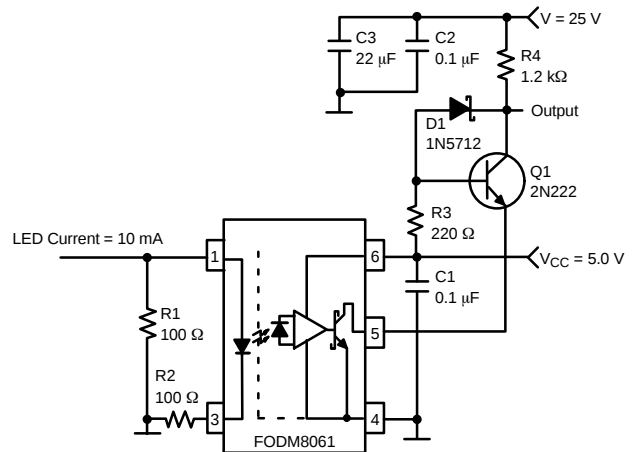


Figure 15. Bipolar Cascode Interface

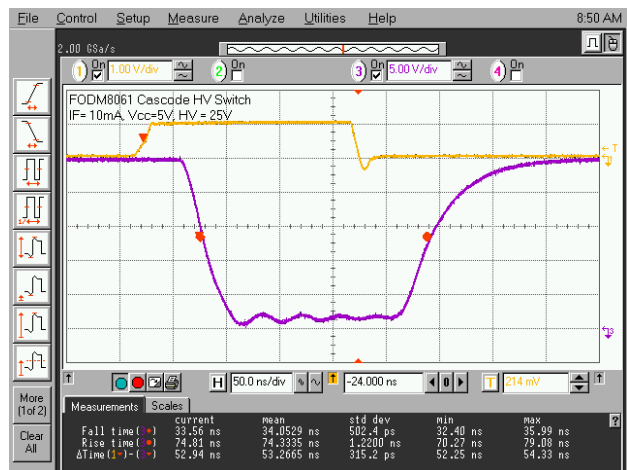


Figure 16. Bipolar HV Cascode Timing

### Interfacing to Voltages Greater than 25 V

Using a high voltage low current signal MOSFET, it is possible to drive loads with supply voltages much greater than 25 V. The BSS123 can be used for supplies up to 100 V. If higher interface voltages are needed the BSS125 can support supplies to 600 V.

Figure 17 shows a MOSFET cascode interface operating from a 50 V source. The load current is 25 mA. The 5 V supply voltage needed by the FODM8061 can be supplied from an external regulated power supply or via a Zener or other regulator deriving its power from the high voltage source.

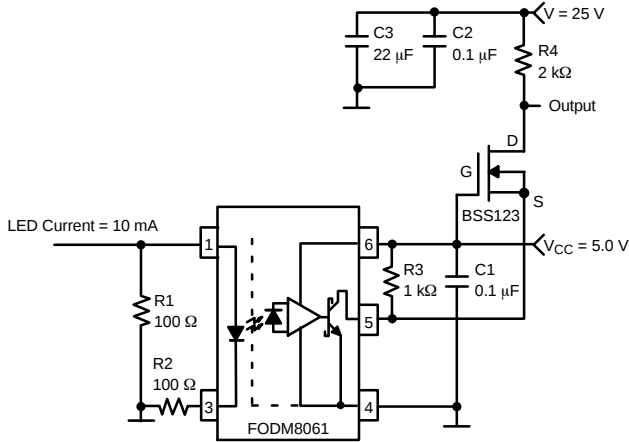


Figure 17. Optocoupler MOSFET Cascode Interface

Figure 18 shows the timing performance of the MOSFET high voltage cascode interface. The  $dv/dt$  of the leading falling edge is about  $1.5 \text{ kV}/\mu\text{s}$ , which is a respectable transition time.

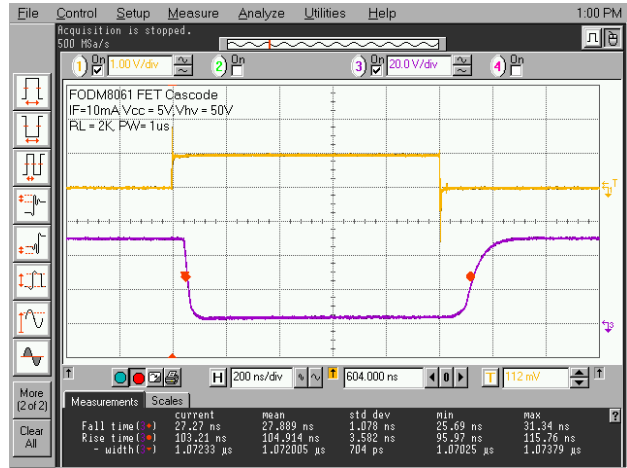


Figure 18. HV MOSFET Cascode Interface

### Conclusion

The FODM8061 high speed optocoupler is an easy to use, multi-purpose optocoupler ideal for isolating communication links with bandwidths of 10 MBaud. The FODM8061's compact package and proven reliable galvanic isolation makes it ideal ensuring safe operation in terms of both safety and signal integrity.

## REVISION HISTORY

| Revision | Description of Changes                      | Date      |
|----------|---------------------------------------------|-----------|
| 2        | Document converted to <b>onsemi</b> format. | 8/26/2026 |

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

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