Product Overview

NBSG53A: 2.5 V / 3.3 V Selectable Differential Clock / Data D Flip-Flop / Clock Divider with Reset and OLS

For complete documentation, see the data sheet.

The NBSG53A is a multi-function differential D flip-flop (DFF) or fixed divide by 2 (DIV/2) clock generator. This is part of the GigaComm family of high performance Silicon Germanium products. A strappable control pin is provided to select between the two functions. The device is housed in a low profile 4x4 mm 16-pin Flip-Chip BGA (FCBGA) package.

The NBSG53A is a device with data, clock, OLS, reset, and select inputs. Differential inputs incorporate internal 50-ohm termination resistors and accept NECL (Negative ECL), PECL (Positive ECL), CMOS, CML, or LVDS. The OLS input is used to program the peak-to-peak output amplitude between 0 and 800 mV in five discrete steps. The RESET and SELECT inputs are single-ended and can be driven with either LVECL or LVCMOS input levels.

Data is transferred to the outputs on the positive edge of the clock. The differential clock inputs of the NBSG53A allow the device to also be used as a negative edge triggered device.

Features

- Maximum Input Clock Frequency (DFF) > 8 GHz Typical
- Maximum Input Clock Frequency (DIV/2) > 10 GHz Typical
- 210 ps Typical Propagation Delay (OLS = FLOAT)
- 45 ps Typical Rise and Fall Times (OLS = FLOAT)
- Selectable Output Level (0 V, 200 mV, 400 mV, 600 mV, or 800 mV Peak-to-Peak Output)
- 50 Ω Internal Input Termination Resistors on all Differential Input
- DIV/2 Mode (Active with Select Low)
- D Flip Flop Mode (Active with Select High)
- Selectable Swing PECL Output with Operating Range: V_{CC} = 2.375 V to 3.465 V with V_{EE} = 0 V
- Selectable Swing NECL Output with NECL Inputs with Operating Range: V_{CC} = 0 V with V_{EE} = -2.375 V to -3.465 V

  For more features, see the data sheet

Applications

- High Performance Logic for ATE and Networking

End Products

- ATE Instrumentation, Networking

Part Electrical Specifications

Product	Compliance	Status	Type	Bits	Input Level	Output Level	V_{CC} Typ (V)	t_{Jitter} Typ (ps)	t_{pd} Typ (ns)	t_{su} Min (ns)	t_h Min (ns)	t_{rec} Typ (ns)	t_R & t_F Max (ps)	f_{Toggle} Typ (MHz)	Package Type
NBSG53AMNG	Pb-free Halide free	Active	D-Type	1	CMOS CML LVDS ECL	ECL	2.5 3.3	0.5	0.215	0.03	0.025	0.012	65	10000	QFN-16
NBSG53AMNHTBG	Pb-free Halide free	Active	D-Type	1	LVDS CMOS ECL CML	ECL	2.5 3.3	0.5	0.215	0.03	0.025	0.012	65	10000	QFN-16

For more information please contact your local sales support at www.onsemi.com.

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