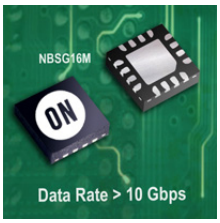
Product Overview



NBSG16M: Multilevel Input to CML Clock/Data Receiver/ Driver/Translator Buffer

For complete documentation, see the data sheet.

The NBSG16M is a differential current mode logic (CML) receiver/driver. The device is functionally equivalent to the EP16, LVEP16, or SG16 devices with CML output structure and lower EMI capabilities.
Inputs incorporate internal 50 Ω termination resistors and accept NECL (Negative ECL), PECL (Positive ECL), LVTTL, LVCMOS, CML, or LVDS. The CML output structure contains internal 50 Ω source termination resistor to VCC. The device generates 400 mV output amplitude with 50 Ω receiver resistor to V_{CC}.
The V_{BB} pin is internally generated voltage supply available to this device only. For all single−ended input conditions, the unused complementary differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, VBB output should be left open.

Features

- Maximum Input Clock Frequency > 10 GHz Typical
- Maximum Input Data Rate > 10 Gb/s Typical
- 120 ps Typical Propagation Delay
- 35 ps Typical Rise and Fall Times
- Positive CML Output with Operating Range: V_{CC} = 2.375 V to 3.465 V with V_{EE} = 0 V
- Negative CML Output with RSNECL or NECL Inputs with Operating Range: V_{CC} = 0 V with V_{EE} = -2.375 V to -3.465 V
- CML Output Level; 400 mV Peak-to-Peak Output with 50 _ Receiver Resistor to V_{CC}
- 50 Ω Internal Input and Output Termination Resistors
- Compatible with Existing 2.5 V/3.3 V LVEP, EP, LVEL and SG Devices
- V_{BB} Reference Voltage Output
  For more features, see the data sheet

Applications

- Backplane buffering
- OC-3 through OC-192 clock or data distribution/driver
- Gigabit Ethernet clock or data driver
- Fibre Channel distribution/driver

Part Electrical Specifications

Product	Compliance	Status	Type	Channels	Input / Output Ratio	Input Level	Output Level	V_{CC} Typ (V)	t_{jitter} RMS Typ (ps)	$t_{skew(o-o)}$ Max (ps)	t_{pd} Typ (ns)	t_R & t_F Max (ps)	f_{max} Clock Typ (MHz)	f_{max} Data Typ (Mbps)	Package Type
NBSG16MMNG	Pb-free Halide free	Active	Signal Driver	1	1:1	LVDS CMOS CML ECL TTL	CML	2.5 3.3	0.2		0.12	53	10000	10000	QFN-16

For more information please contact your local sales support at www.onsemi.com.

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