Product Overview

NBSG14: SiGe Clock / Data Fanout Buffer, 1:4 Differential, 2.5 V / 3.3 V, with RSECL Outputs

For complete documentation, see the data sheet.

The NBSG14 is a 1-to-4 clock/data distribution chip, optimized for ultra-low skew and jitter. Inputs incorporate internal 50-ohm termination resistors and accept

</bR>NECL (Negative ECL), PECL (Positive ECL), LVTTL, LVCMOS, CML, or LVDS. Outputs are RSECL (Reduced Swing ECL), 400 mV.

Features

- Maximum Input Clock Frequency up to 12 GHz
- Maximum Input Data Rate up to 12 Gb/s Typical
- 50 Ω Internal Input Termination Resistors
- 30 ps Typical Rise and Fall Times
- 125 ps Typical Propagation Delay
- RSPECL Output with Operating Range: V<subCC</sub> = 2.375 V to 3.465 V with V_{EE} = 0 V
- RSNECL Output with RSNECL or NECL Inputs with Operating Range: V_{CC} = 0 V with V_{EE} = -2.375 V to -3.465 V
- RSECL Output Level (400 mV Peak-to-Peak Output),
- Compatible with Existing 2.5 V/3.3 V LVEP, EP, and LVEL Devices

End Products

Part Electrical Specifications

Product	Compliance	Status	Type	Channels	Input / Output Ratio	Input Level	Output Level	V_{CC} Typ (V)	t_{jitter} RMS Typ (ps)	$t_{skew(o-o)}$ Max (ps)	t_{pd} Typ (ns)	t_R & t_F Max (ps)	f_{max} Clock Typ (MHz)	f_{max} Data Typ (Mbps)	Package Type
NBSG14MNG	Pb-free Halide free	Active	Buffer	1	1:4	CML LVDS TTL CMOS ECL	ECL	2.5 3.3	0.2	15	0.125	55	12000	12000	QFN-16
NBSG14MNHTBG	Pb-free Halide free	Active	Buffer	1	1:4	LVDS TTL CML CMOS ECL	ECL	2.5 3.3	0.2	15	0.125	55	12000	12000	QFN-16
NBSG14MNR2G	Pb-free Halide free	Active	Buffer	1	1:4	LVDS TTL ECL CML CMOS	ECL	3.3 2.5	0.2	15	0.125	55	12000	12000	QFN-16

For more information please contact your local sales support at www.onsemi.com.

Created on: 2/15/2019