# Product Overview

## NB7L32M: ÷·2 Divider with CML Output

For complete documentation, see the data sheet.

The NB7L32M is an integrated /2 divider with differential clock inputs and asynchronous reset.

Differential clock inputs incorporate internal 50 Ω termination resistors and accept LVPECL (Positive ECL), CML, or LVDS. The high frequency reset pin is asserted on the rising edge. Upon power-up, the internal flip-flops will attain a random state; the reset allows for the synchronization of multiple NB7L32M's in a system.

The differential 16 mA CML output provides matching internal 50 Ω termination which guarantees 400 mV output swing when externally receiver terminated 50 Ω to VCC (See Figure 16).

The device is housed in a small 3x3 mm 16 pin QFN package.

## Features

- Maximum Input Clock Frequency 14 GHz Typical
- 200 ps Max Propagation Delay
- 30 ps Typical Rise and Fall Times
- < 0.5 ps Maximum (RMS) Random Clock Jitter
- Operating Range: $V_{CC}$ = 2.375 V to 3.465 V with $V_{EE}$ = 0 V
- CML Output Level (400 mV Peak-to-Peak Output), Differential Output Only
- 50 Ω Internal Input and Output Termination Resistors
- Functionally Compatible with Existing 2.5 V / 3.3 V LVEL, LVEP, EP, and SG Devices
- Full RoHS Compliance.

## Applications

- High frequency clock division in Automated Test Equipment.
- Ultra precise clock division in networking and telecomm applications.

## Part Electrical Specifications

| Product | Compliance | Status | Type | Input Level | Output Level | $V_{CC}$ Typ (V) | $f_{Max}$ Typ (MHz) | $t_{pd}$ Typ (ns) | $t_R$ & $t_F$ Max (ps) | Package Type |
|---|---|---|---|---|---|---|---|---|---|---|
| NB7L32MMNG | Pb-free<br>Halide free | Active | Divider | CML<br>ECL<br>LVDS | CML | 2.5<br>3.3 | 14000 | 0.155 | 45 | QFN-16 |

**For more information please contact your local sales support at www.onsemi.com.**

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