Product Overview

MC100LVE310: Clock / Data Fanout Buffer, 2:8 Differential, ECL, 3.3 V

For complete documentation, see the data sheet.

The MC100LVE310 is a low voltage, low skew 2:8 differential ECL fanout buffer designed with clock distribution in mind. The device features fully differential clock paths to minimize both device and system skew. The LVE310 offers two selectable clock inputs to allow for redundant or test clocks to be incorporated into the system clock trees. To ensure that the tight skew specification is met it is necessary that both sides of the differential output are terminated into 50, even if only one side is being used. In most applications all eight differential pairs will be used and therefore terminated. In the case where fewer than eight pairs are used it is necessary to terminate at least the output pairs adjacent to the output pair being used in order to maintain minimum skew. Failure to follow this guideline will result in small degradations of propagation delay (on the order of 10-20 ps) of the outputs being used, while not catastrophic to most designs this will result in an increase in skew. Note that the package corners isolate outputs from one another such that the guideline expressed above holds only for outputs on the same side of the package. The MC100LVE310, as with most ECL devices, can be operated from a positive VCC supply in LVPECL mode. This allows the LVE310 to be used for high performance clock distribution in +3.3 V systems. Designers can take advantage of the LVE310's performance to distribute low skew clocks across the backplane or the board. In a PECL environment series or Thevenin line terminations are typically used as they require no additional power supplies, if parallel termination is desired a terminating voltage of VCC-2.0 V will need to be provided. For more information on using PECL, designers should refer to Application Note AN1406/D. The VBB pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connecte

Features

- 200ps Part-to-Part Skew
- 50ps Output-to-Output Skew
- The 100 Series Contains Temperature Compensation
- ESD Protection: >2 KV HBM, >200 V MM
- PECL Mode Operating Range: VCC = 3.0 V to 3.8 V with VEE = 0 V
- NECL Mode Operating Range: VCC = 0 V with VEE = -3.0 V to -3.8 V
- Internal Input Pulldown Resistors
- Q Output will Default LOW with All Inputs Open or at VEE
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1For Additional Information, see Application Note AND8003/D

  For more features, see the data sheet

Part Electrical Specifications

Product	Compliance	Status	Type	Channels	Input / Output Ratio	Input Level	Output Level	V_{CC} Typ (V)	t_{jitter} RMS Typ (ps)	$t_{skew(o-o)}$ Max (ps)	t_{pd} Typ (ns)	t_R & t_F Max (ps)	f_{max} Clock Typ (MHz)	f_{max} Data Typ (Mbps)	Package Type
MC100LVE310FNR2G	Pb-free Halide free	Active	Buffer	1	2:1:8	ECL	ECL	3.3	1.5	75	0.65	600	1000		PLCC-28

For more information please contact your local sales support at www.onsemi.com.

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