Product Overview

MC100EL34: 5.0 V ECL ÷2, ÷4, ÷8 Clock Generation Chip

For complete documentation, see the data sheet.

The MC10/100EL34 is a low skew divide by 2, divide by 4, divide by 8 clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The device can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal. In addition, by using the VBB output, a sinusoidal source can be AC coupled into the device (see Interfacing section of the ECLinPS Data Book DL140/D). If a single-ended input is to be used, the VBB output should be connected to the CLK input and bypassed to ground via a 0.01 F capacitor. The VBB output is designed to act as the switching reference for the input of the EL34 under single-ended input conditions, as a result, this pin can only source/sink up to 0.5mA of current. The common enable (EN) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input. Upon startup, the internal flip-flops will attain a random state; the master reset (MR) input allows for the synchronization of the internal dividers, as well as multiple EL34s in a system.The 100 Series contains temperature compensation.

Features

- 50ps Output-to-Output Skew
- Synchronous Enable/Disable
- Master Reset for Synchronization
- PECL Mode Operating Range: VCC = 4.2 V to 5.7 V with VEE = 0 V
- NECL Mode Operating Range: VCC = 0 V with VEE = -4.2 V to -5.7 V
- Internal Input Pulldown Resistors on CLK(s), ENbar, and MR
- Pb-Free Packages are Available

Part Electrical Specifications

Product	Compliance	Status	Type	Input Level	Output Level	V_{CC} Typ (V)	f_{Max} Typ (MHz)	t_{pd} Typ (ns)	t_R & t_F Max (ps)	Package Type
MC100EL34DG	Pb-free Halide free	Active	Divider	ECL	ECL	5	1100	1080	475	SOIC-16

For more information please contact your local sales support at www.onsemi.com.

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