The Future of Semiconductor System Level Integration

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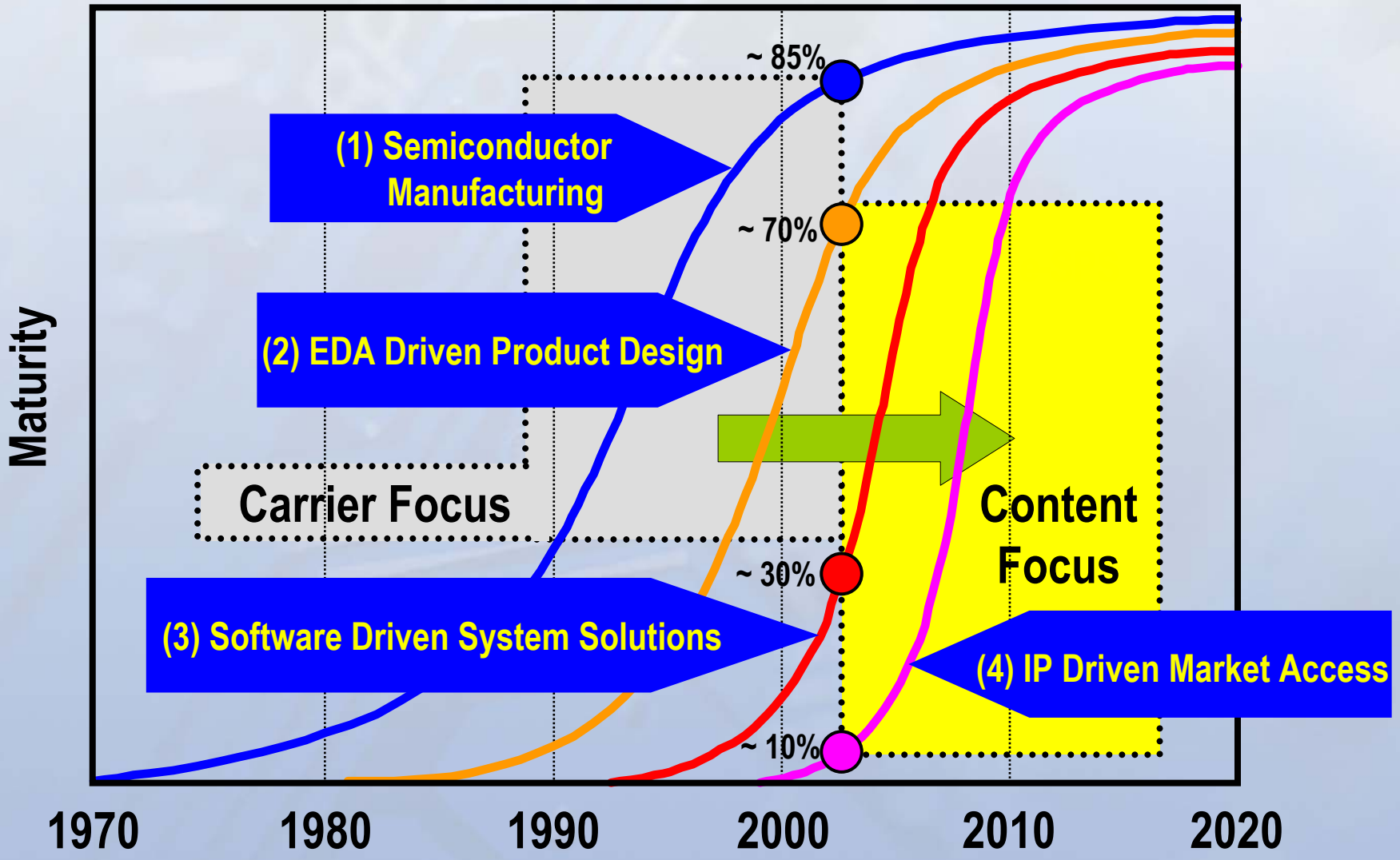
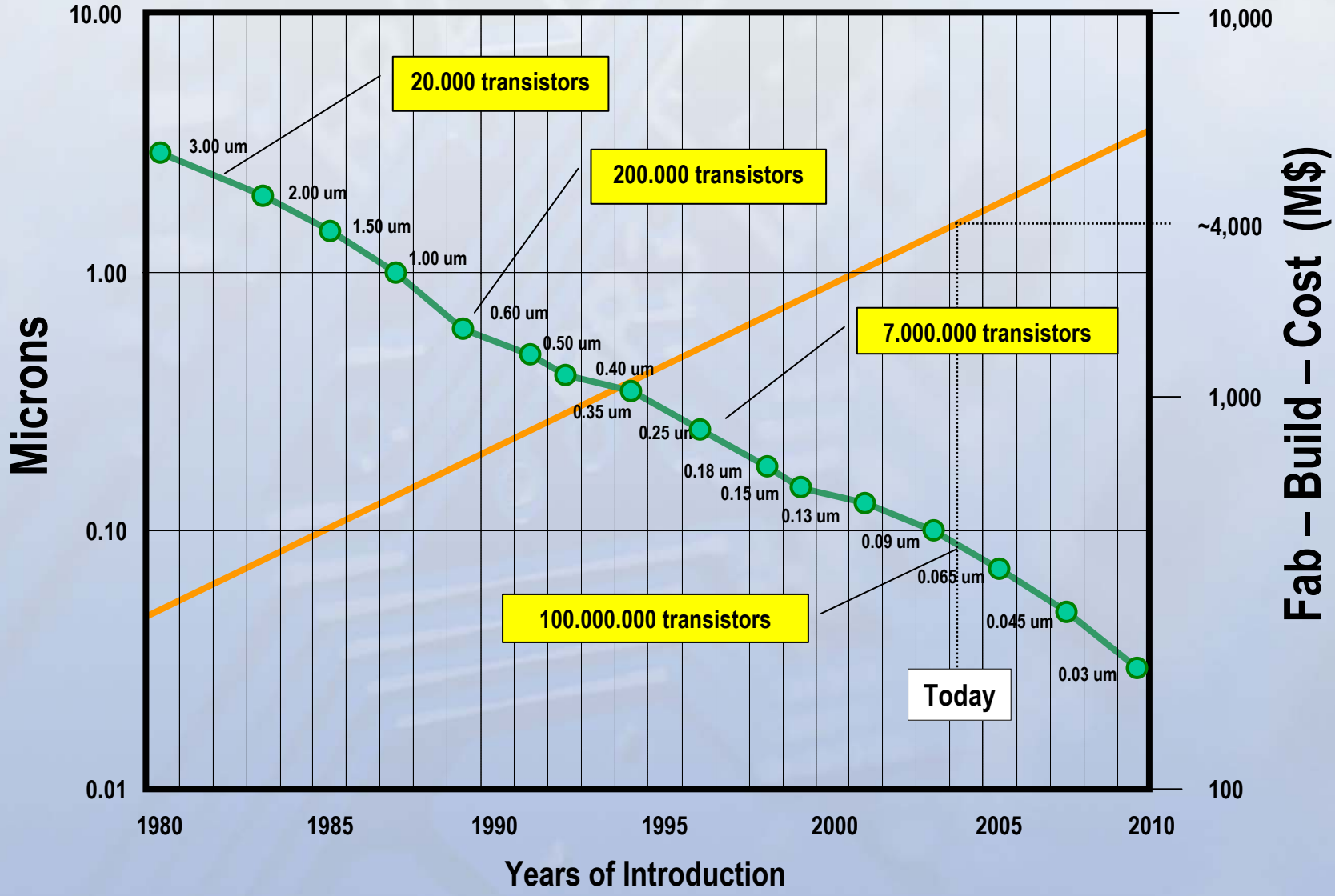
Semiconductor Industry Productivity Drivers
- Four Curve Maturity Model -



Moore's Law and Fab Investments



Debate over Moore's Law and Economics

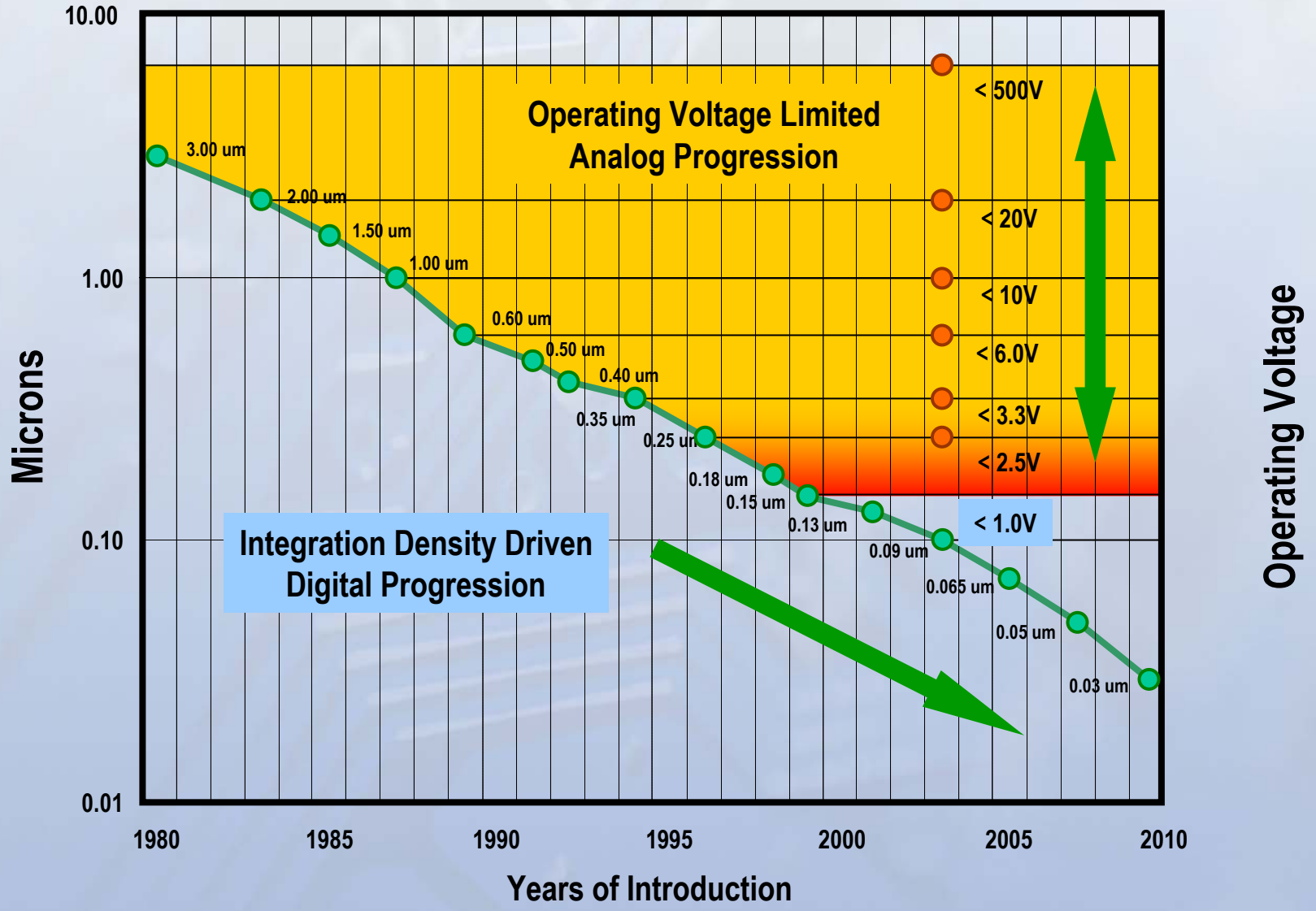
- Intel's co-founder Gordon Moore accurately predicted the number of transistors on a chip to double every 18 months
- Moore's Law appropriately applies to transistor size affecting the area of Silicon, which a transistor occupies
- To further execute Moore's Law, fundamentally new processes need to be developed, adding huge additional costs for the industry
- No exponential progress continues forever. However, it is technically entirely feasible to develop the next four to five technology nodes
- Economics will potentially drive a slower rate of Moore's Law. Cumulative industry revenues are replacing time as the factor for tracking Moore's Law
- Moore's Law today is more about wafer costs as compared to integrating more transistors per chip over the past decade
- Moore's Law remains relevant; It is just a matter of affordability of investments

300 mm Wafer Fab Indices

Fab Indices	Low End	Typical	High End	Unit
Wafer Diameter	300	300	300	mm
Line Width	90	65	45	nm
Number of Transistors per Chip	25	100	400	Million
Supply Voltage	1.0	0.8	0.5	Volt
Chip Size	35	50	100	mm^2
Wafer Capacity	6,000	8,000	10,000	Wafers/week
Process Cycle Time	30	40	60	Days
Production Volume in Units		500		Million/year
Production Volume in Value	2	5	10	Billion $
Average Selling Price		10		$
Cost of Mask Set	0.6	1.0	2.0	Million $
Fab Investment	2	4	6	Billion $

- Increasingly higher mask costs require extremely high unit volumes to amortize costs
- Increasingly higher process complexities stretch process cycle times

Digital versus Analog Integration Progression

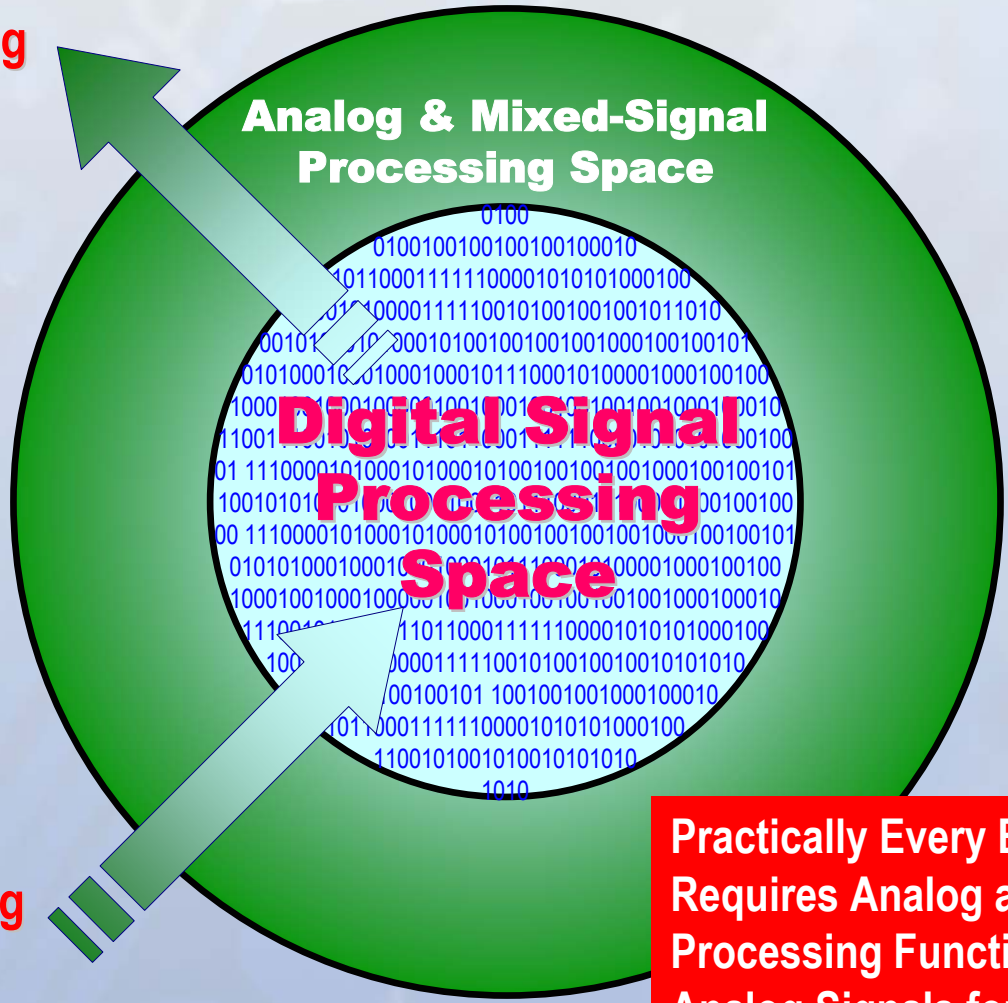


Analog Separation from Digital Integration

- Technology Conflicts: Analog and digital functions cannot always be co-integrated
- Scaling Separation: Analog integration does not scale like digital integration, deep sub-micron devices degrade in analog performance characteristics
- Signal-to-Noise Ratio: Voltage scaling presents limits to required analog S/N ratios
- Signal Integrity: Digital signals interfere with low level analog signals
- Signal Resolution Limits: Decreasing digital supply voltage levels will result in the disintegration of some analog and mixed-signal functions from the Digital Integration Space
- Digital Product Vulnerability: Deeply scaled device dimensions associated with smaller line width increase susceptibility and vulnerability of digital integrated products to electrical upset events, i.e. ESD
- Digital Product Protection: Analog devices can protect against larger than 20KV ESD events, scaled digital devices are destroyed at a few hundred volts
- Black Art: Analog integration has been lagging digital integration for one decade
- The Mix: Most analog solutions are a mix of ICs, discrete components, power devices

Translation Layers between Analog Signal Transport and Digital Signal Processing

Signal Conditioning Outgoing Signals



Analog Signal Transport Outside the Electronic System in various Media:

- ❑ Wires
- ❑ Cables
- ❑ Fibers
- ❑ Air (Wireless)

Most Signals Are Analog Out Here:

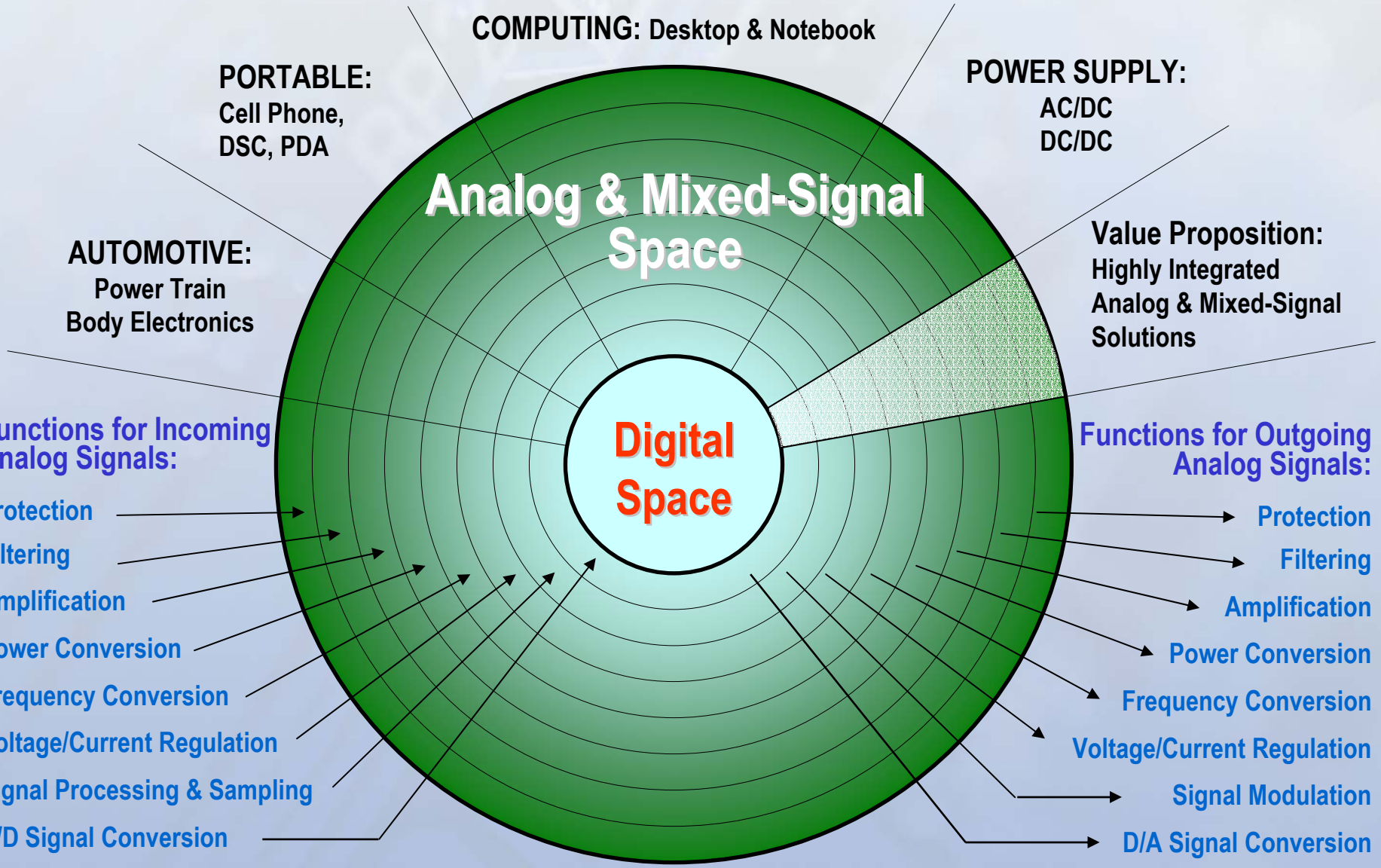
Signal Strength:
- ❑ From uV to KV

Signal Frequency:
- ❑ From DC to Optical

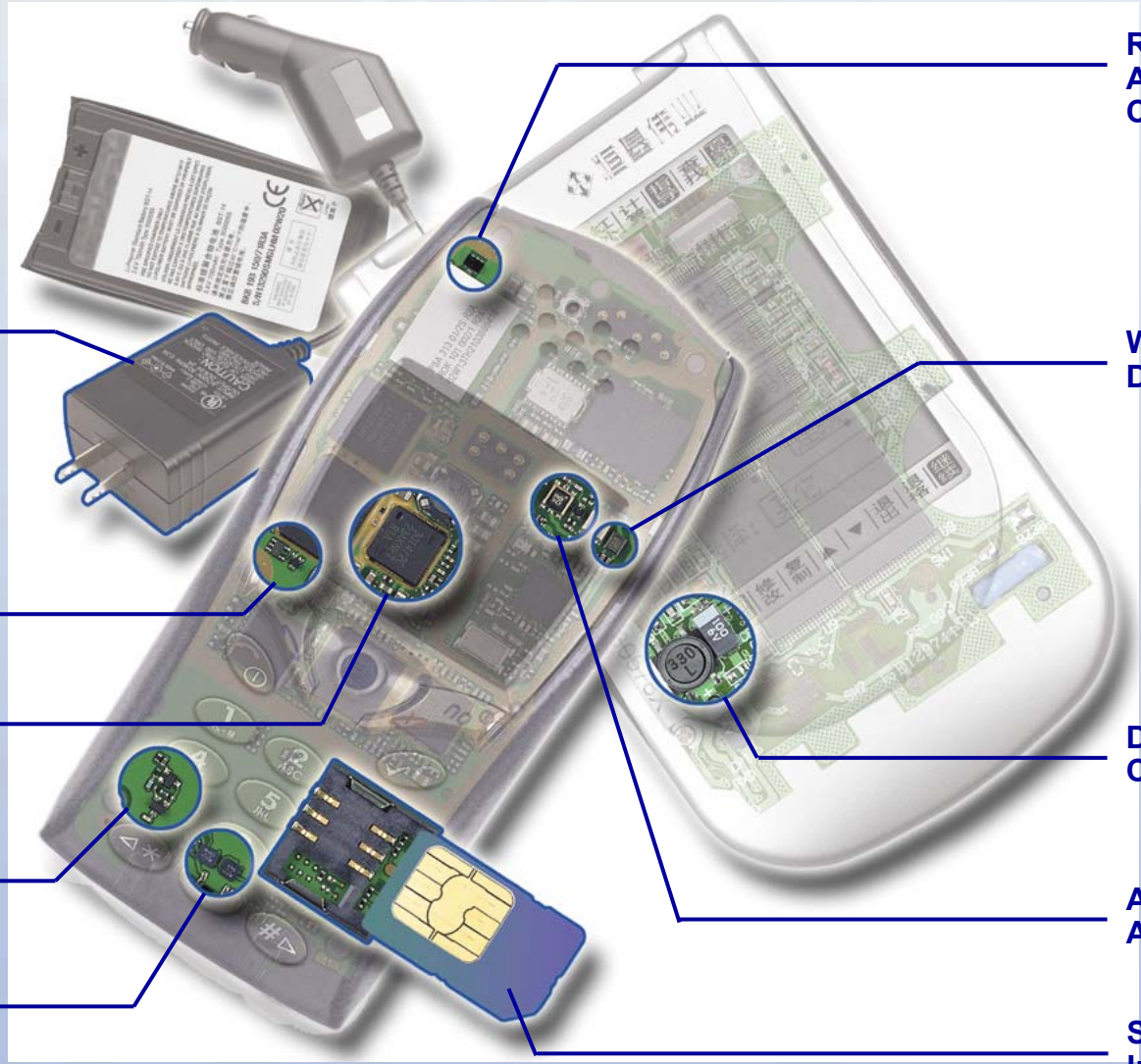
Signal Conditioning Incoming Signals

Practically Every Electronic System Requires Analog and Mixed-Signal Processing Functions to Condition Analog Signals for Digital Processing

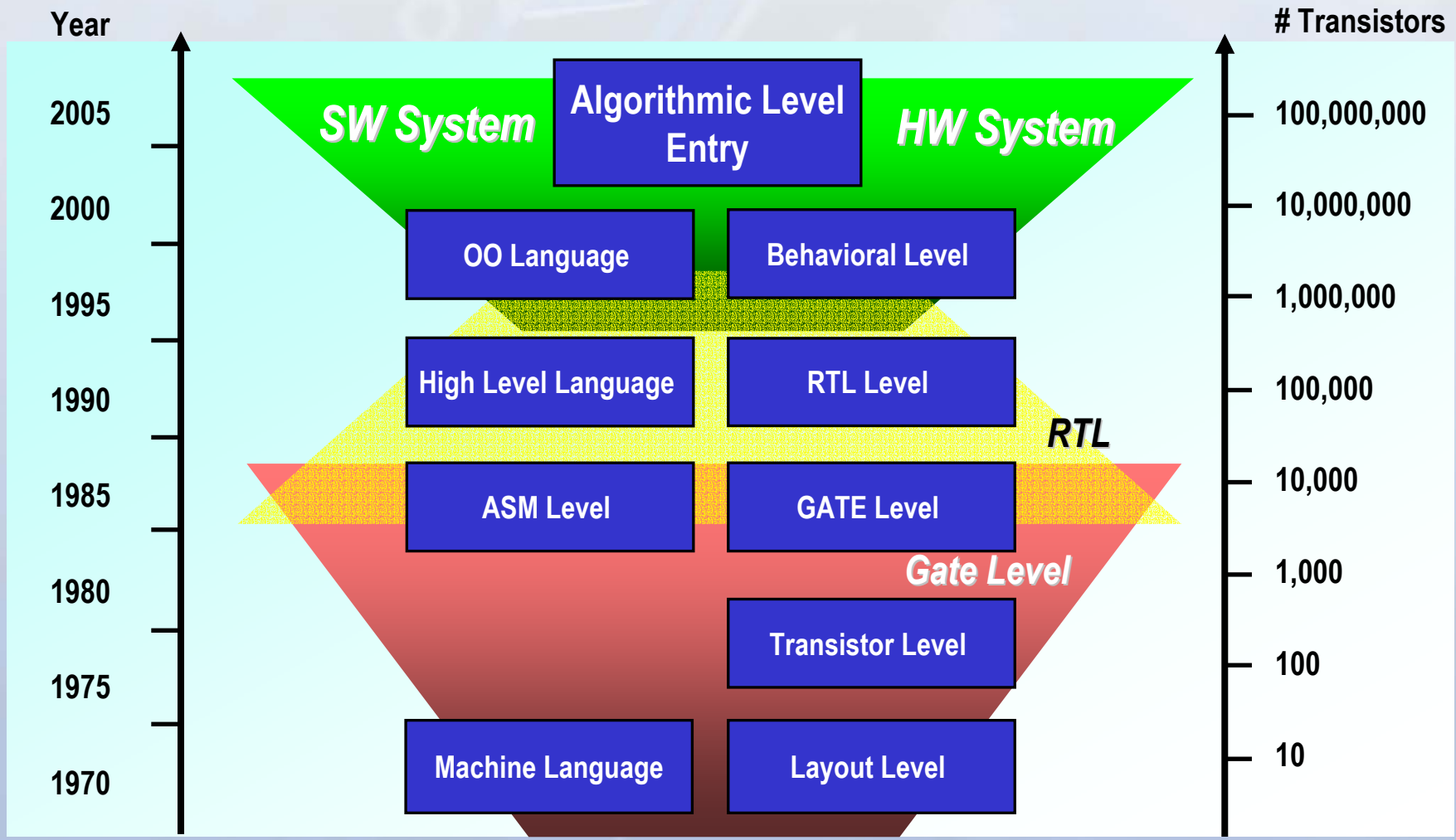
Analog Super-Integration Around the Digital Space



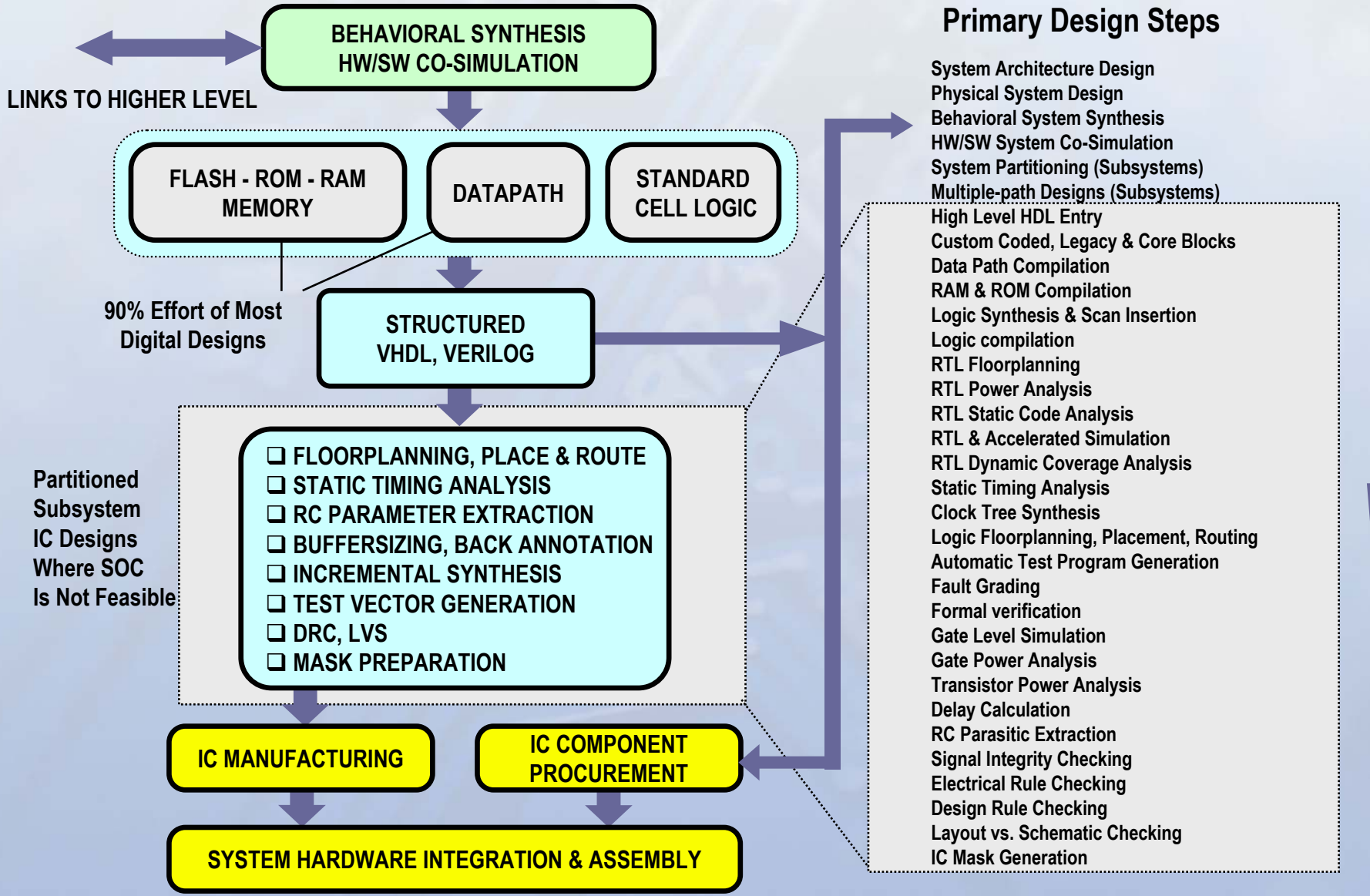
Examples of Analog Content in Portable Power Management Products



Curve 2:
How Have Design Methodologies Changed?



Advanced HW System Design Flow



Primary Design Steps

System Architecture Design
Physical System Design
Behavioral System Synthesis
HW/SW System Co-Simulation
System Partitioning (Subsystems)
Multiple-path Designs (Subsystems)
High Level HDL Entry
Custom Coded, Legacy & Core Blocks
Data Path Compilation
RAM & ROM Compilation
Logic Synthesis & Scan Insertion
Logic compilation
RTL Floorplanning
RTL Power Analysis
RTL Static Code Analysis
RTL & Accelerated Simulation
RTL Dynamic Coverage Analysis
Static Timing Analysis
Clock Tree Synthesis
Logic Floorplanning, Placement, Routing
Automatic Test Program Generation
Fault Grading
Formal verification
Gate Level Simulation
Gate Power Analysis
Transistor Power Analysis
Delay Calculation
RC Parasitic Extraction
Signal Integrity Checking
Electrical Rule Checking
Design Rule Checking
Layout vs. Schematic Checking
IC Mask Generation

Curve 2:
EDA Driven Product Design

Evolution of Highly Automated and Synthesized Design Flows:

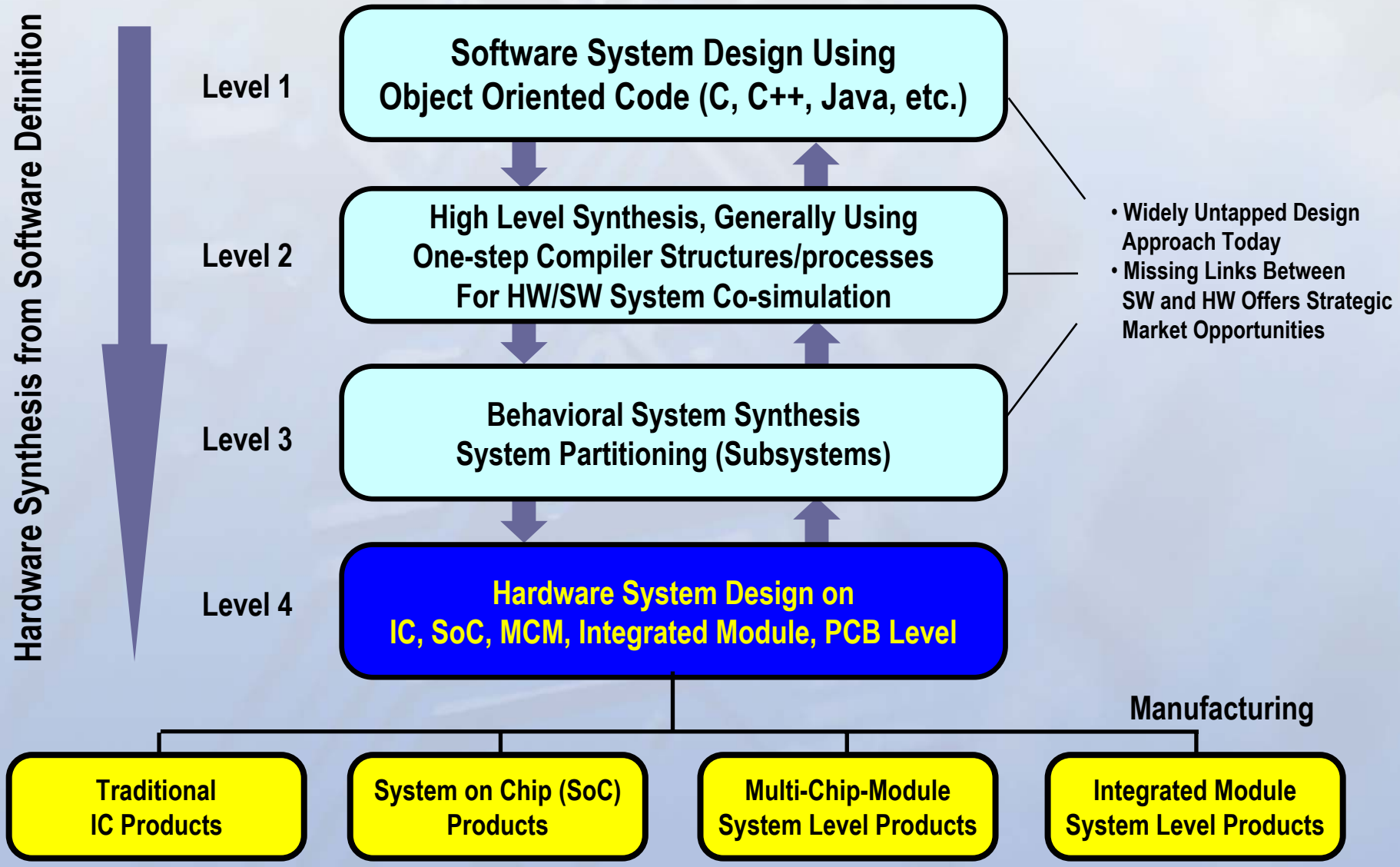
- Synthesized Register Transfer Level (RTL) design methodology
- Availability of proven and qualified library components
- Portability of designs to alternative IC manufacturing processes
- Automated formal verification methods

Curve 3:
Software Driven System Solutions

Systems on Chip (SoC) Design Dictates a New Order:

- The longest cycle, namely SOC design, is becoming a bigger and bigger fraction of what is going into applications
- All HW and SW levels are derived from application specifications
- Virtual Prototyping is needed with application flows modeled at the highest level (cost of design error is prohibitive)
- All SW development will require a common language
- HW development will have to be completely automated
- All software and hardware engineers will have to communicate
- Software, not Hardware, will provide IP leverage in the future

Integrated Design System from SW to HW

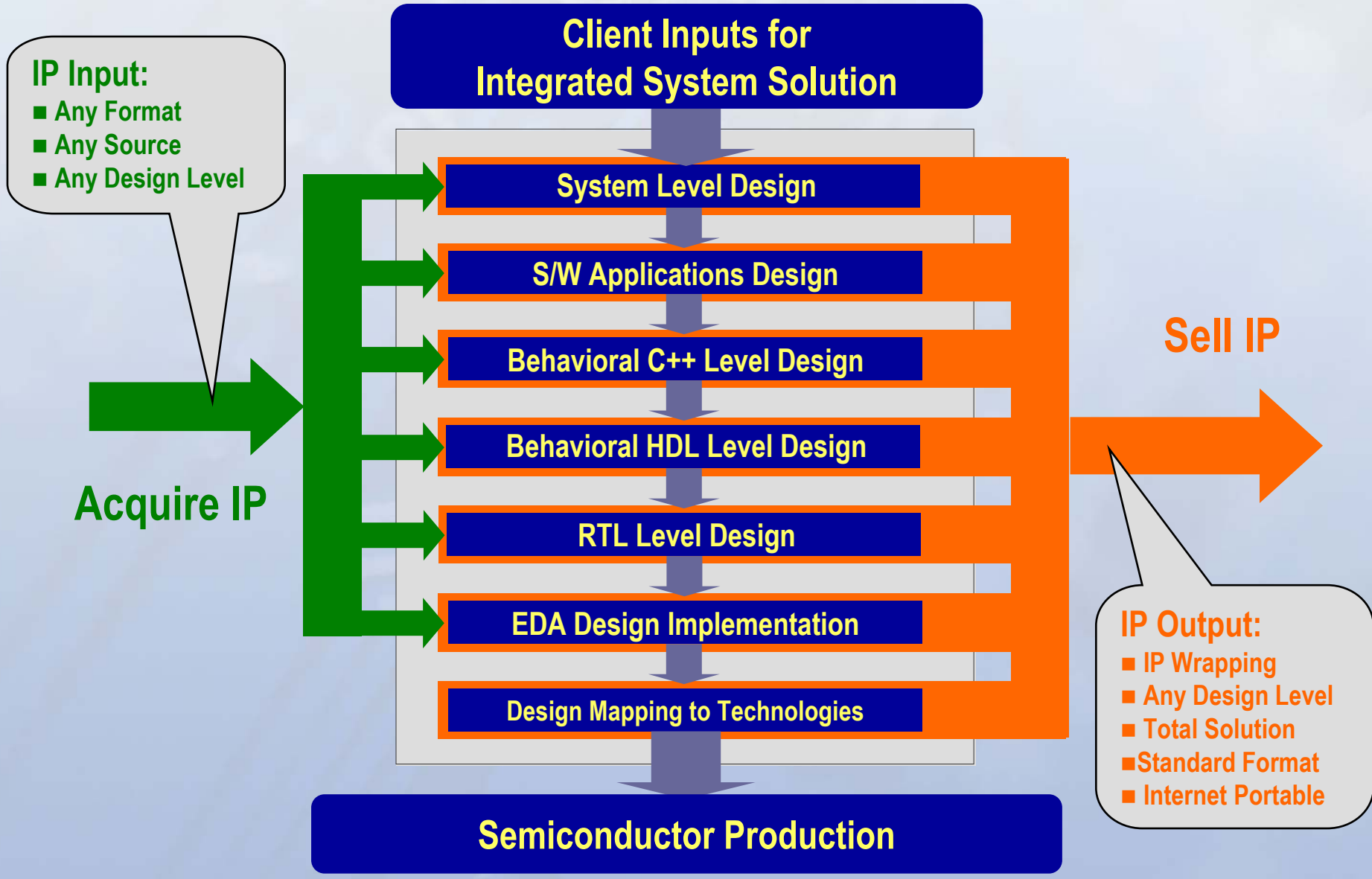


Curve 4:
Intellectual Property Driven Market Access

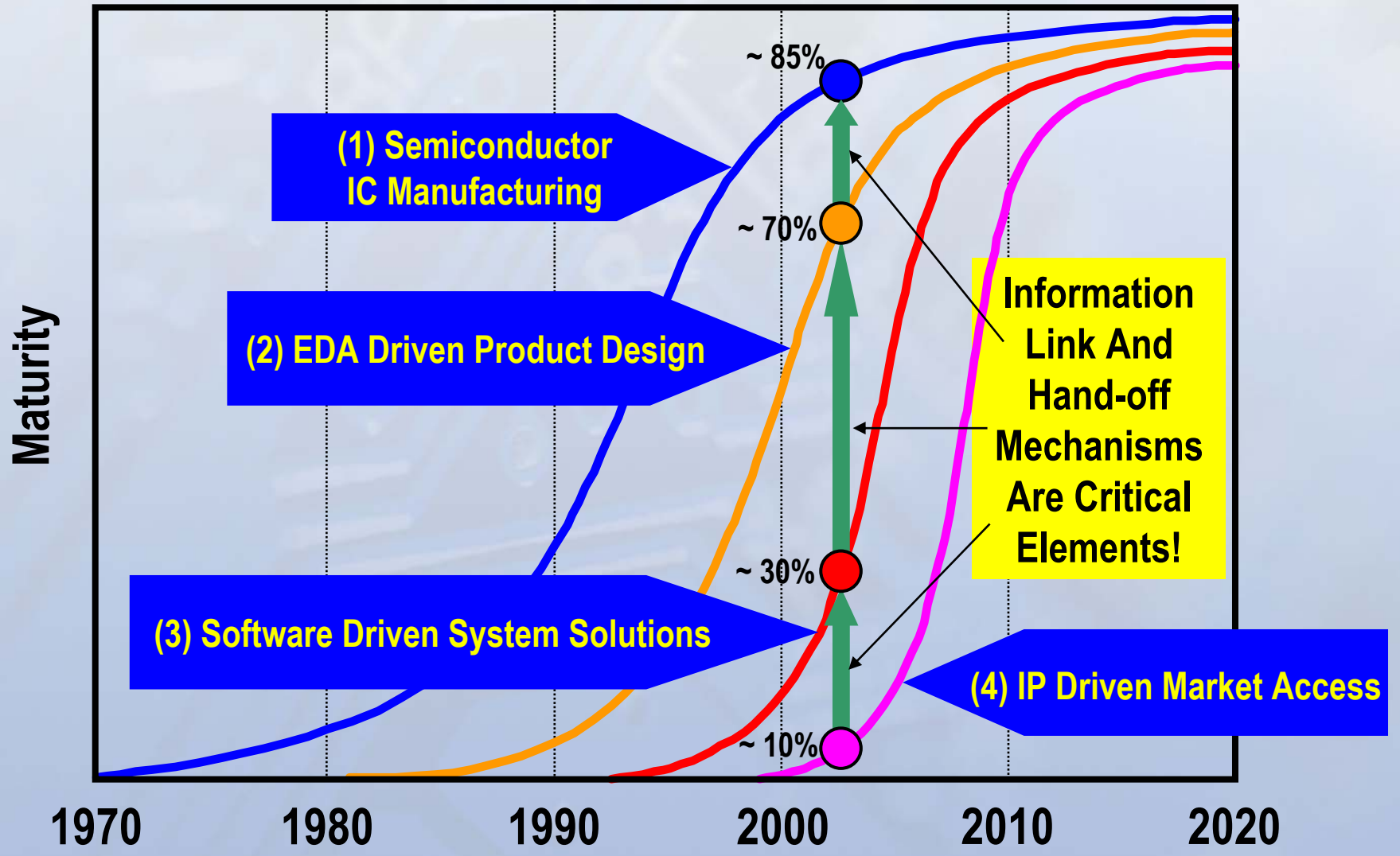
Implications of IP on the Semiconductor Industry:

- Content (knowledge, software, end-applications) will be increasingly separated from carrier (silicon delivery channel)
- Vertically integrated structures will be challenged by open and networked organizational structures
- More and more internet-centric companies will be fabless
- Systems-solution providers will build on IP Driven Market Access
- Cycle time will be reduced by purchasing outside IP at all levels
- Synthesis tools are needed to generate new IP and new products
- The creation of IP as a product will drive company market value

Design Engine and Marketable IP Generator



Semiconductor Industry Productivity Drivers
- Four Curve Linkage -



Summary and Outlook

Below the Inflection Points:

- Invest In Technology And Networked Businesses
- By Year 2010, 95% Of All Systems Shipped Will Use IP Procured From Outside Sources (Source: Dataquest)

Near The Inflection Point:

- Dominate The Space Or Exit!

Above The Inflection Point:

- Reduce Or Abandon R&D Investments
- Create Partnerships And Relationships For Outsourcing

Connecting All Four Maturity Curves:

- The Prosperity Of The Semiconductor Industry Depends On The Effective Linkage Of All Disciplines On All Four Curves With Value-added Distribution And Access To The Market
- With Many Different Suppliers In This Food Chain, The Development Of A Well-established Data and Information Flow Is Essential