Predicting Fusing Current for Encapsulated Wire Bonds under Transient Loads

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Abstract

For high power IC chips, as device size inevitably decreases, the wire diameter unfortunately must decrease due to the need of finer pitch wires. Fusing or melting of wirebonds thus increasingly becomes one of the potential failure issues for such IC's. Experiments were performed under transient loads on dummy packages having aluminum, gold, or copper wires of different dimensions. A finite element model was constructed that correlates very well with the observed maximum operating currents for such wirebonds under actual experimental test conditions. A qualitative observation of typical current profiles, as fusing conditions were approached, was that current would reach a maximum value very early in the pulse, and then fall gradually. One goal achieved through the modeling was to show that the current in the wire falls with time due to the heating of the wire material. Correspondingly, the wire reaches the melting temperature not at the peak current but rather at the end of pulse. Further, modeling shows that knowledge of external resistance and inductance of the experimental set up are highly significant in determining the details of a fusing event, but if known along with the temperature-dependent wire properties, the simulation can predict the correct voltage and current response of the part with 2% error. On the other hand, lack of external circuit characteristics may lead to completely incorrect results. For instance, the assumption that current is constant until the wire heats to fusing temperature, or that current and temperature both rise monotonically to maximum values until the wire fuses, are almost certain to be wrong. The work has been carried out for single pulse events as well as pulse trains.

Key words: Bond wire fusing, wire melting, fusing current

I. Introduction

Fusing of bond wires in IC packages has drawn the attention of many researchers over the last few years [1-6]. However most of the analytical equations used in these papers have been developed for bare wires (wires surrounded by air). For IC packages, when the wires are encapsulated in the molding compounds, these equations are no longer valid. Fusing occurs because of joule heating (I^2R) and this excessive energy cannot be dissipated outside the wire. The wire fails when the temperature of hottest point in the wire reaches the melting temperature of the material of the wire, and the molten material flows away and disrupts the current path.

Often it is important to predict the maximum amount of current a bond wire can carry in an IC package without causing it to melt. More specifically one would like to know the time and the maximum current that caused a wire of certain type to fuse. We however found that under transient loads, the maximum current carrying capacity depends upon the test set up; for example knowing the exact external resistance, inductance of the external circuit as well as how the power supply was varied is important in order to determine the fusing current of a given wire type. If these parameters are known along with the temperature-dependent wire properties, we have shown that ANSYS simulation can predict the correct voltage and current response of the part with 2%

error. On the other hand, lack of external circuit characteristics may lead to completely incorrect results. For instance, the assumption that current is constant until the wire heats to fusing temperature, or that current and temperature both rise monotonically to maximum values until the wire fuses, are wrong.

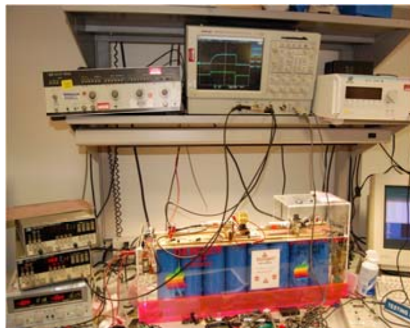
We have performed some experiments under transient loads on dummy packages (no die is present in the package; the wire is directly bonded to the flag). Wires of different material (Al, Au and Cu) with varying lengths and diameters have been tested. The experimental set up is discussed in section II. We have tested the parts under a single pulse as well as under a pulse train containing up to 10 pulses. For the pulse train, parts were tested under two different conditions. In one test the external resistance was kept fixed and power supply voltage was increased monotonically. In the other, the power supply was kept fixed but the gate voltage of the driver was changed. This will become clearer when we explain the experimental set up in the section II.

Next we simulated all the above mentioned experimental conditions with ANSYS finite element methods, which are discussed in section III.

II. Experimental Procedure

All of these encapsulated packages contain usually either one or two wire bonds. For packages with two wirebonds only one was tested at a time. The packages are molded with sumitomo G600 molding compound.

Figure 1 shows the test set up; the schematic diagram is shown on the right hand side. There are 16 10,000 μF capacitors in parallel, which are charged by the power supply. A pulse generator is connected to the gate of a fast, low Rds(on) power MOSFET. When the gate is turned on, the capacitor bank is shorted across the device under test (DUT). A test ends either when the DUT fails, or the pulse generator reaches the end of the preprogrammed pulse.



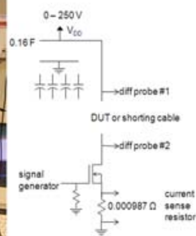


Figure 1. Experimental Set Up for Wire Fuse, and Schematic Diagram for the Circuit

The set up is designed to provide a very high constant current up to 600 A This was tested by inserting a shorting cable. The tester was designed with the goals of having very low resistance and inductance. It will be seen that, knowing these values fairly accurately is important in understanding the observed fusing behavior of the samples actually tested.

Next, the wire-only sample device, soldered onto a circuit board, was tested as shown in Figure 2(a). The initial (before the test) and the final (after the wire fused) resistance of the wire was also measured. Later, X-ray pictures of the fused parts were also taken to attempt to identify the precise location of a break in the wire corresponding to the open in the circuit. Figure 2(b) displays the voltage probe across the part.

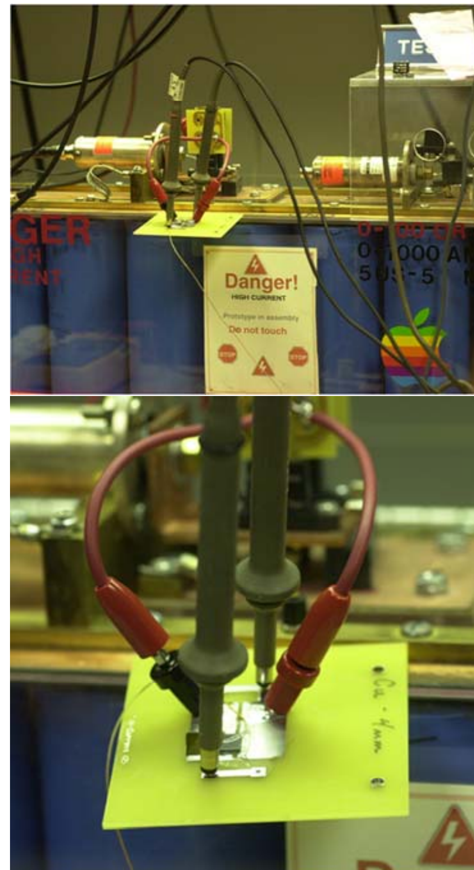


Figure 2(a) Experimental Set Up with the Actual Part, (b) Zoomed in Picture Across the Part

The voltage across the part, and the current through the shunt, was monitored on the oscilloscope screen. For the single pulse experiment, using constant 100 μs width gate pulses, the power supply

voltage was increased in steps till the circuit showed an open. The screen shots for voltage and the current characteristics for different wire types at the respective highest current are shown in Figure 3(a)-(c). Note that the scale of the y-axis is different for each graph.

Six samples for each type of wire were tested and all six samples fused roughly at the same value of the maximum current.

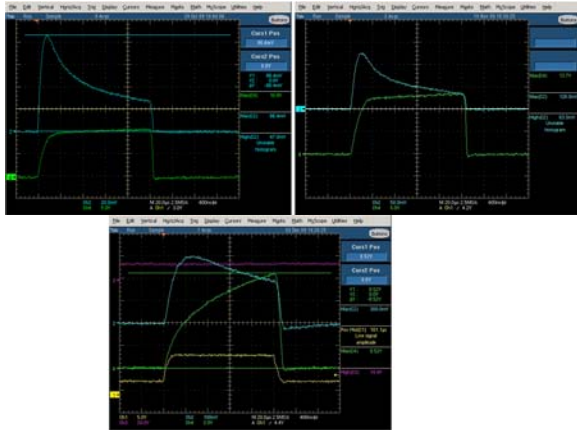


Figure 3. Current and Voltage Response for (a) Au at V_{max} = 10.3 V, I_{max} = 86.4 A, (b) Cu at V_{max} = 11.27 V, I_{max} = 114 A, (c) Al at V_{max} = 14.4 V, I_{max} = 300 A.

A qualitative observation of typical current profiles as fusing conditions were approached, was that current would reach a maximum value very early in the pulse, and then fall gradually. One goal of the modeling was to show whether, as seen in Figure 3(a)-(c), the current in the wire (the top trace) falls with time due to the heating of the wire material. It did indeed, as will be discussed subsequently.

Another qualitative observation is related to the DUT voltage profiles. For Au or Cu wires (and also the very low resistance shorting cable), the voltage across the DUT reaches essentially a constant value within the first 20 µs. In dramatic contrast, the voltage across Al wire samples keeps increasing with time, Figure 3(c), and never attains a constant value. More details on the single pulse experimental results have been discussed in our previous paper [7].

Having successfully matched model with experiment for single-pulse events, we next tested some parts under a pulse train containing 10 pulses of 100us width and 40us off time. Figure 11 (later in the paper) shows the oscilloscope screen shots of the voltage and the current characteristic of Au wire under two different conditions. The picture on the left is representative of tests wherein the external circuit resistance was constant throughout the pulse train (as in the single-pulse tests), and the power supply voltage was increased from one run to the next until fusing occurred. The picture on the right represents tests where the external power supply voltage was fixed throughout, and only the gate voltage of the MOSFET switch was adjusted from one run to the next (refer to schematic, Figure 1); this had the effect of introducing a variable resistance into the external circuit as the pulse train would advance. Clearly, the current (top most trace) and the voltage across the DUT (middle trace) for the two different set ups are entirely different. In the next section we simulate all the above mentioned experimental conditions using ANSYS.

III. ANSYS Simulations

A half axisymmetric model was created using ANSYS®. PLANE67 (coupled thermal-electric solid) elements are used. In Figure 4, the violet elements represent the wire and the teal colored elements represent the surrounding molding compound. The end of the wire is fixed at ambient temperature (298 K) and 0 V, a reasonable approximation because in reality the wires are welded at both the ends to large thermal mass. The element size of the surrounding mold is chosen such that the time constant (l^2/α) is the same for the wire and mold, where α is the thermal diffusivity and l is the element length measured in the direction of the temperature gradient (that is, the radial dimension in most of the model). The time constant chosen for the elements was 0.1 µs to ensure adequate response, so as not to artificially delay the heating of the wire (a typical error in transient thermal simulations).

The rise in the voltage with time on the screen shots of the oscilloscope clearly indicates the inductive nature of the test circuit. We therefore measured the resistance (*R1*) and inductance (*L1*) of the circuit in our experimental setup, then added circuit elements (CIRCU124) in our model as shown in Figure 4.

The inductance (*L2*) of the sample wire itself [8] was calculated using equation (1):

$$L2 = 2l[2.303\log(4l/d) - l + \mu/4 + (d/2l)] \quad (1)$$

L2 is the inductance in nH, *l* is the length and *d* is the diameter of the wire in cm, μ is permeability of the material which is chosen to be 1 (for all materials except for ferromagnetic materials). Material data are defined as functions of temperature to consider their sensitivity towards temperature. Since there is a

phase change when the wire melts, using enthalpies instead of specific heats (c_p) allows direct accounting for the correct heat of fusion. Since the model is half symmetry, we take half of the experimental measured voltage values. To simulate the experimental set up where we varied the power supply voltage, we can apply a fixed voltage V_PS (half of the power supply voltage) at the top node of *R1,* and measure the current response as a reaction force at this node. The voltage across the part Vdut is measured at the node at the end of *L2*.

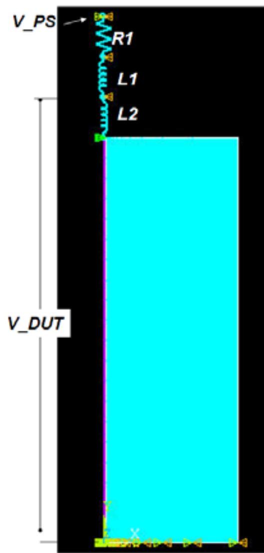
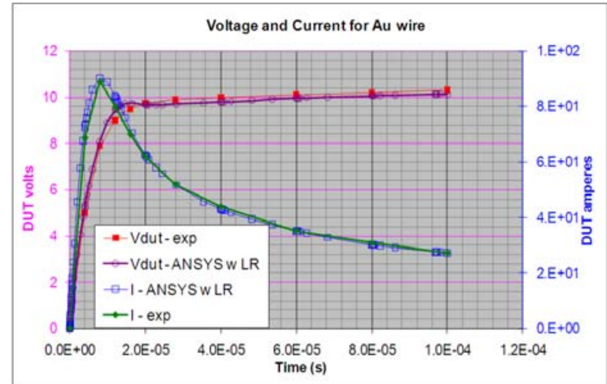
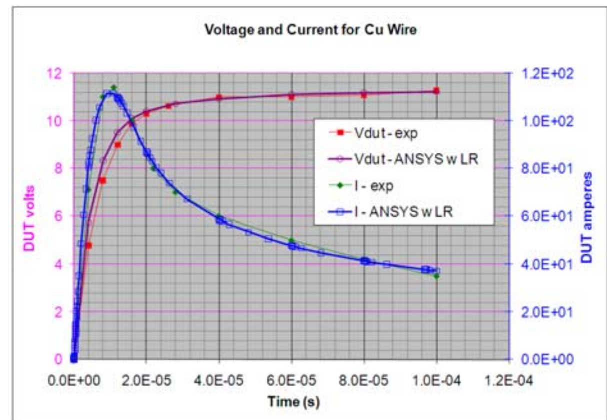


Figure 4. ANSYS Model of the wire surrounded by molding compound along with *L1, L2* and *R1* circuit elements.

III (a) Results for a Single Pulse

The comparison of voltage and current of the wire model with experimental values for a single pulse are shown in Figure 5a, 5b and 5c for Au, Cu and Al wires respectively. The voltage across the wire (Vdut) is plotted on primary y axis where as the current response is plotted on the secondary y axis. The diameter for the Au and the Cu wires are 0.0508 mm (2 mils) where as that for the Al wire is 0.127 mm (5 mils). The wires were 4 mm and 6 mm long; however, the transient results didn't depend upon the length.





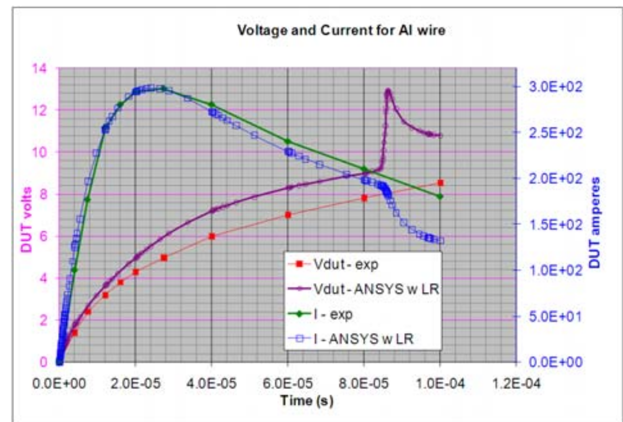


Figure 5. Comparison of Voltage and Current Response in ANSYS model with Experiment for (a) Au, (b) Cu and (c) Al wires.

Figure 6 shows the rise of the temperature of the midpoint of the wire with time. Referring back to Figure 5 it is interesting to note that the wire doesn't melt when the current is maximum. Rather, it reaches the melting temperature at end of the 100 μs pulse, when actually the wire fuses. The temperature of most of the mold (except for that at the wire interface) remains at ambient temperature. In early

tests, the DUT case temperature was monitored with a thermocouple to ensure that the device always began each new test at the same ambient temperature. (Not surprisingly, the DUT temperature was never measurably distinct from room temperature, so this experimental detail was subsequently discontinued.) We observe very similar behavior for the Au and Al wires as well. For these two cases, too, we see at the end of 100 µs, most of the wire has reached its melting point.

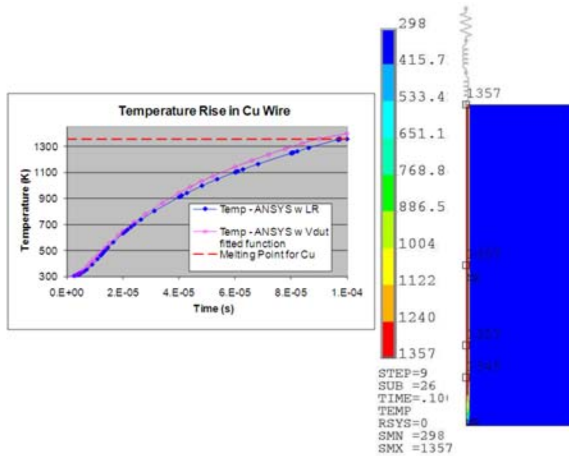


Figure 6. Temperature vs. Time curve for Model having L, R Circuit Elements, and Temperature Contour Plot at 100 µs for Cu Wire.

III (b) Results for Pulse Trains

We next applied a pulse train of 10 pulses with 100 us width and 40 us off time at the top node of R1. Figures 7 and 10 compare the experimental and simulation results for Au (2 mil diameter) and Al (10 mil diameter) wires.

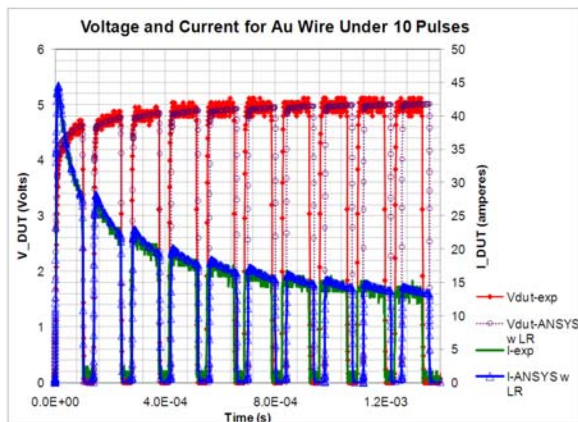


Figure 7. Comparison of Voltage and Current Response in ANSYS model with Experiment for Au wire for a Pulse Train.

As in the single pulse experiment we see for the Au wire the current falls in time and the Vdut attains a constant value, but for the Al wire the Vdut never attains a constant value.

Figure 8 shows screen shots of the current and the voltage before and after the DUT fused. The top trace represents the voltage across the DUT, the middle one the current and the bottom one the power supply voltage.

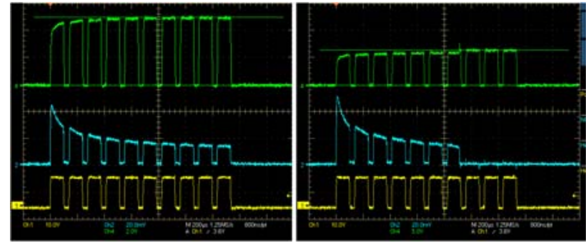


Figure 8. Voltage and Current Behavior before and after the fire fused.

We see the wire fused after 6th pulse and at a maximum *starting* current of 50 A, though as mentioned previously, current at the actual moment of fusing was only approximately 15 A. ANSYS simulations in Figure 9 also show that the temperature of the midpoint of the wire reached melting temperature after 6 pulses.

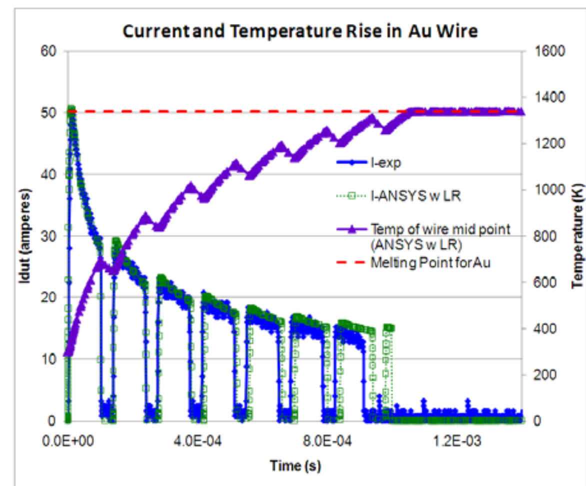


Figure 9. Current and Temperature of the Au wire at the Fusing Current.

Similarly Figure 10 shows the voltage and current behavior for Al wire. We see that although the current and voltage matched within 0.4% for the

2 mil Au wire, it didn't match quite as well for the 10 mil Al wire. In the simulations the wire melted after 8 pulses, whereas in the experiment the part survived all 10 pulses. The simulation assumes the wire fuses as soon as temperature of the midpoint reaches the melting point, but in real world a significant portion of the wire might have melted before it fused.

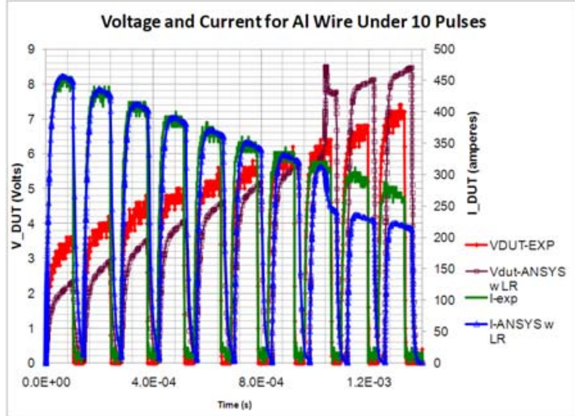


Figure 10. Comparison of Voltage and Current Response in ANSYS model with Experiment for Al wire for a Pulse Train.

Pulses with fixed power supply voltage

In the next set up, the parts were tested under 10 pulses where the power supply voltage was held constant and the gate voltage of the driver was varied till the wire fused. Figure 11 contrasts the current and the voltage behavior when the power supply voltage was varied to when the gate voltage was varied. It is interesting to see that while the Au wire was able to withstand a maximum current of 44 A for the former condition it was able to withstand a maximum current of only 23 A for the latter before fusing.

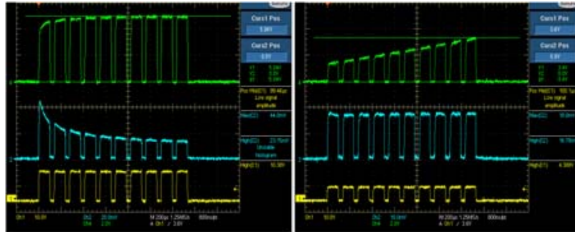


Figure 11. Voltage and Current Behavior under Two Different Experimental Set Ups.

Also we note that in one case the current is falling with time while the Vdut voltage is more or less constant, but for the other case the current is constant and the Vdut voltage keeps rising. Hence we see the maximum fusing current for a given type of wire depends upon the experimental conditions. Since there isn't a way to model nonlinear circuit elements in ANSYS, the measured Vdut voltage data from the oscilloscope output was directly applied to the top nodes of the wire, thus for this ANSYS model we don't have the external resistor *R1* or the inductor *L1*. Again we found that there is a good match in the current for the Au wire (figure 12), whereas the current in Al wires differs by 12% from the experimental conditions.

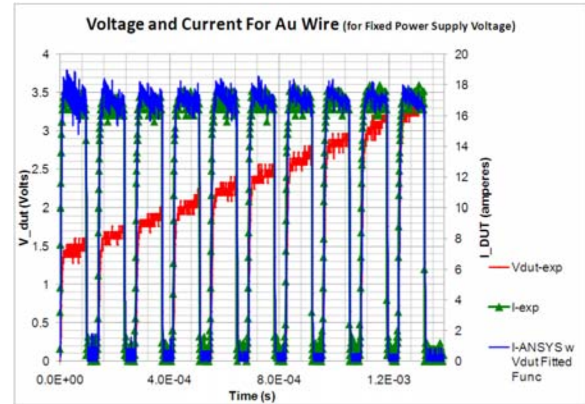


Figure 12. Comparison of Current Response for a Fitted Voltage function in Au wire.

For a single pulse the voltage Vdut can be approximated by a dual-time-constant exponential function of the form

$$V_i = V_{\max}\,(v_{ratio}\,(1-\exp(t_i/\tau_1)+(1-v_{ratio})\,(1-\exp(t_i/\tau_2)) \qquad (2)$$

where v_{ratio}, τ_1 and τ_2 were solved iteratively to fit the experimental profile within about 1% over the pulse duration. This form allows us to quickly vary the voltage boundary conditions to match any of the experimental data sets with just a few parameters. For each given wire material, the time constants and v_{ratio} ended up fairly consistent over a wide range of power supply settings, reducing the boundary condition variable to essentially just one value: $V_{\max}$, for each different wire material. See our previous paper [7] for details.

Conclusions

The final results are summarized in Table 1 and 3 below.

The ANSYS model for the Au and the Cu wire show excellent correlation with the experimental

results, however for Al wire we observe some discrepancies. The results hold true where the parts were tested for a single pulse, or a train of 10 pulses, whether the power supply voltage was varied or the gate voltage of the driver was varied. For Al, the model with L, R circuits elements, the current response matches well with the experimental result, and the overall form of the voltage drop matches very nicely the experimental observations (especially with regard to the stark qualitative difference between Au and Cu, versus the Al). However, the magnitude of the voltage drop across the wire predicted by ANSYS differs by approximately 11% as compared to the experimental results. Also, the wire melts earlier in the simulation. (That the wire in reality did not melt earlier, yet continue to conduct current rather than fuse into an open circuit, is argued against from the smooth nature of the current profile. The simulations make it clear that wire undergoing a complete phase change results in a very rapid decrease in current, yet that doesn't go all the way to zero.)

Given the success of the Au and Cu models, and the fact that the experiments were carried out on the same experimental apparatus in all cases, this suggests that the temperature-dependent thermal or electrical properties of the Al wire actually used, differ somewhat from the published properties assumed in the finite-element models. Attempts at modifying these properties to better match the experimental results have not yet been fruitful.

Table 1. Comparison of the Max Peak Current (I_{max}) and Voltage V_{max} across the wire (Peak Value of Vdut) when the power supply voltage was varied.

Pulse	Wire Material	Dimension		Peak Current I_{max} (A)			Peak Voltage Across the wire (V)		
		length (mm)	diameter (mm)	Expt	ANSYS with L, R circuit elements	% error	Exp	ANSYS with L, R circuit elements	% error
1	Au	6	0.0508	89	90.2	1.3	10.3	10.1	2
1	Cu	6	0.0508	114	112	1.7	11.27	11.24	0.3
1	Al	6	0.127	298	297	0.3	8.52	9.28	8.9
10	Au	7	0.0508	44	44	0	5.04	5.01	0.6
10	Al	10.2	0.254	520	455	12	7.6	8.2	8

Table 2. Comparison of the Max Peak Current (I_{max}) and Voltage (V_{max}) for Two different Set Up Conditions

Pulse	Wire Material	Dimension		Peak Current I_{max} (A)				Peak Voltage (V_{max}) Across the wire		
		length (mm)	diameter (mm)	when power supply voltage was varied		when gate voltage was varied		when power supply voltage was varied		when gate voltage was varied
				Expt	ANSYS	Expt	ANSYS	Expt	ANSYS	Expt
10	Au	7	0.0508	44	44	23.2	22.6	5.04	5.01	7.4
10	Al	10.2	0.254	520	456	480	489	7.6	8.2	8.4

We conclude that it is very important to know the exact external circuit characteristics in order to predict the fusing current. Knowing the test set up and the circuit parameters such as the external circuit resistance and inductance, along with the temperature-dependent wire properties, suffices to construct a model that explains transient voltage, current, and temperature behavior during fusing events, without resort to ancillary internal voltage (or any other) measurements. On the other hand, lack of external circuit characteristics may lead to completely incorrect assumptions about the nature of the current profiles that will be seen in an actual customer application, and wrong conclusions about maximum current carrying capability of wires.

Acknowledgments

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