

# NTMFS4926N

## Power MOSFET

30 V, 44 A, Single N-Channel, SO-8 FL

### Features

- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- Optimized for 5 V, 12 V Gate Drives
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications

- CPU Power Delivery
- DC-DC Converters

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	$V_{DSS}$	30	V	
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	V	
Continuous Drain Current $R_{\theta JA}$ (Note 1)	$I_D$	$T_A = 25^\circ\text{C}$	15.5	A
		$T_A = 100^\circ\text{C}$	9.8	
Power Dissipation $R_{\theta JA}$ (Note 1)	$P_D$	2.70	W	
Continuous Drain Current $R_{\theta JA} \leq 10$ s (Note 1)	$I_D$	$T_A = 25^\circ\text{C}$	23.4	A
		$T_A = 100^\circ\text{C}$	14.8	
Power Dissipation $R_{\theta JA} \leq 10$ s (Note 1)	$P_D$	6.13	W	
Continuous Drain Current $R_{\theta JA}$ (Note 2)	$I_D$	$T_A = 25^\circ\text{C}$	9.0	A
		$T_A = 100^\circ\text{C}$	5.7	
Power Dissipation $R_{\theta JA}$ (Note 2)	$P_D$	0.92	W	
Continuous Drain Current $R_{\theta JC}$ (Note 1)	$I_D$	$T_C = 25^\circ\text{C}$	44	A
		$T_C = 100^\circ\text{C}$	28	
Power Dissipation $R_{\theta JC}$ (Note 1)	$P_D$	21.6	W	
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	$I_{DM}$	182	A
Current Limited by Package	$T_A = 25^\circ\text{C}$	$I_{Dmax}$	100	A
Operating Junction and Storage Temperature	$T_J, T_{STG}$	-55 to +150		$^\circ\text{C}$
Source Current (Body Diode)	$I_S$	21	A	
Drain to Source DV/DT	$dV/dt$	6.0	V/ns	
Single Pulse Drain-to-Source Avalanche Energy ( $T_J = 25^\circ\text{C}, V_{DD} = 24$ V, $V_{GS} = 20$ V, $I_L = 21$ A <sub>pk</sub> , $L = 0.1$ mH, $R_G = 25 \Omega$ )	$E_{AS}$	22	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

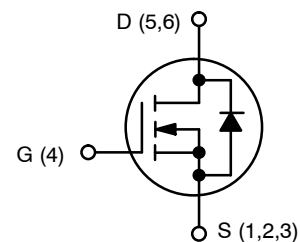
1. Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
2. Surface-mounted on FR4 board using the minimum recommended pad size.



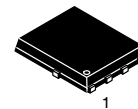
ON Semiconductor®

<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	$I_D$ MAX
30 V	7.0 m $\Omega$ @ 10 V	44 A
	11.2 m $\Omega$ @ 4.5 V	

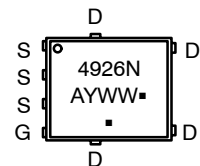


N-CHANNEL MOSFET



SO-8 FLAT LEAD  
CASE 488AA  
STYLE 1

### MARKING DIAGRAM



- A = Assembly Location
  - Y = Year
  - WW = Work Week
  - = Pb-Free Package
- (Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping†
NTMFS4926NT1G	SO-8 FL (Pb-Free)	1500 / Tape & Reel
NTMFS4926NT3G	SO-8 FL (Pb-Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTMFS4926N

## THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	5.8	°C/W
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	46.3	
Junction-to-Ambient – Steady State (Note 4)	$R_{\theta JA}$	136.2	
Junction-to-Ambient – ( $t \leq 10$ s) (Note 3)	$R_{\theta JA}$	20.4	

- Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
- Surface-mounted on FR4 board using the minimum recommended pad size.

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage (transient)	$V_{(BR)DSSt}$	$V_{GS} = 0\text{ V}, I_{D(aval)} = 8.8\text{ A}, T_{case} = 25^\circ\text{C}, t_{transient} = 100\text{ ns}$	34			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			25		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$			1.0	$\mu\text{A}$
		$T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$			10	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA

## ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.32	1.6	2.2	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			3.8		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 30\text{ A}$	5.6	7.0	m $\Omega$
			$I_D = 15\text{ A}$	5.6		
		$V_{GS} = 4.5\text{ V}$	$I_D = 30\text{ A}$	9.0	11.2	
			$I_D = 15\text{ A}$	8.7		
Forward Transconductance	$g_{FS}$	$V_{DS} = 1.5\text{ V}, I_D = 15\text{ A}$		40		S

## CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 15\text{ V}$		1004		pF
Output Capacitance	$C_{OSS}$			390		
Reverse Transfer Capacitance	$C_{RSS}$			119		
Capacitance	$C_{RSS}/C_{ISS}$	$V_{GS} = 0\text{ V}, V_{DS} = 15\text{ V}, f = 1\text{ MHz}$		0.119	0.237	
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}; I_D = 30\text{ A}$		8.7		nC
Threshold Gate Charge	$Q_{G(TH)}$			1.4		
Gate-to-Source Charge	$Q_{GS}$			3.0		
Gate-to-Drain Charge	$Q_{GD}$			3.5		
Total Gate Charge	$Q_{G(TOT)}$		$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}; I_D = 30\text{ A}$		17.3	

## SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 15\text{ A}, R_G = 3.0\ \Omega$		8.6		ns
Rise Time	$t_r$			36.9		
Turn-Off Delay Time	$t_{d(OFF)}$			14.7		
Fall Time	$t_f$			5.5		

- Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Switching characteristics are independent of operating junction temperatures.

# NTMFS4926N

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>SWITCHING CHARACTERISTICS</b> (Note 6)						
Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V},$ $I_D = 15\text{ A}, R_G = 3.0\ \Omega$		6.6		ns
Rise Time	$t_r$			31.8		
Turn-Off Delay Time	$t_{d(OFF)}$			18.3		
Fall Time	$t_f$			4.0		

## DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V},$ $I_S = 30\text{ A}$	$T_J = 25^\circ\text{C}$		0.87	1.1	V
			$T_J = 125^\circ\text{C}$		0.76		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s},$ $I_S = 30\text{ A}$		21.9		ns	
Charge Time	$t_a$			11.0			
Discharge Time	$t_b$			10.9			
Reverse Recovery Charge	$Q_{RR}$			8.0		nC	

## PACKAGE PARASITIC VALUES

Source Inductance	$L_S$	$T_A = 25^\circ\text{C}$		1.00		nH
Drain Inductance	$L_D$			0.005		nH
Gate Inductance	$L_G$			1.84		nH
Gate Resistance	$R_G$			1.0	2.2	$\Omega$

5. Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

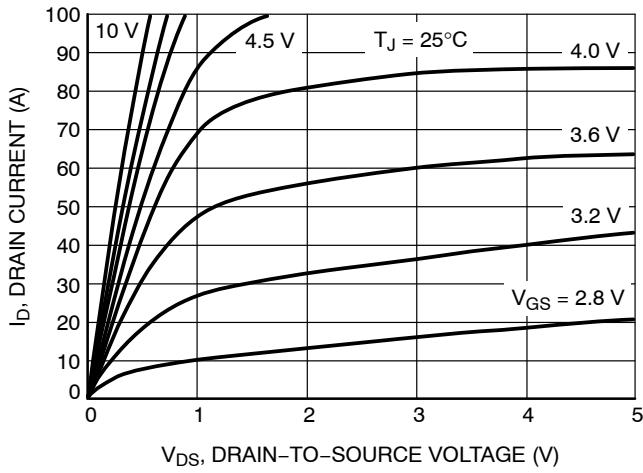


Figure 1. On-Region Characteristics

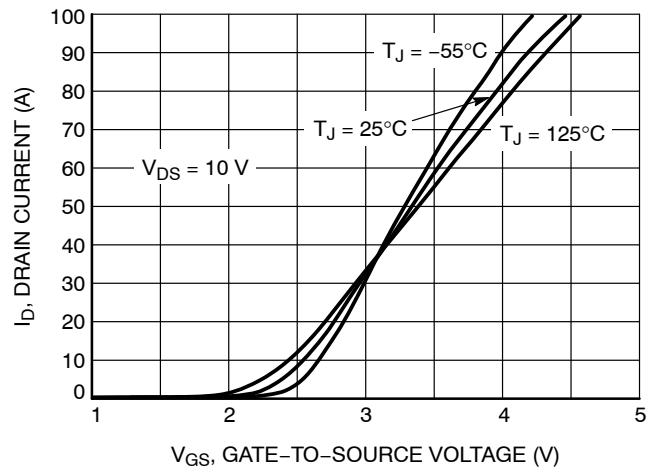


Figure 2. Transfer Characteristics

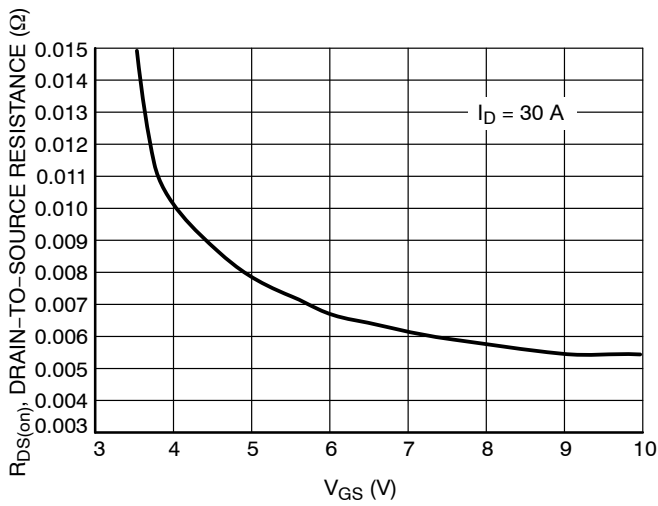


Figure 3. On-Resistance vs.  $V_{GS}$

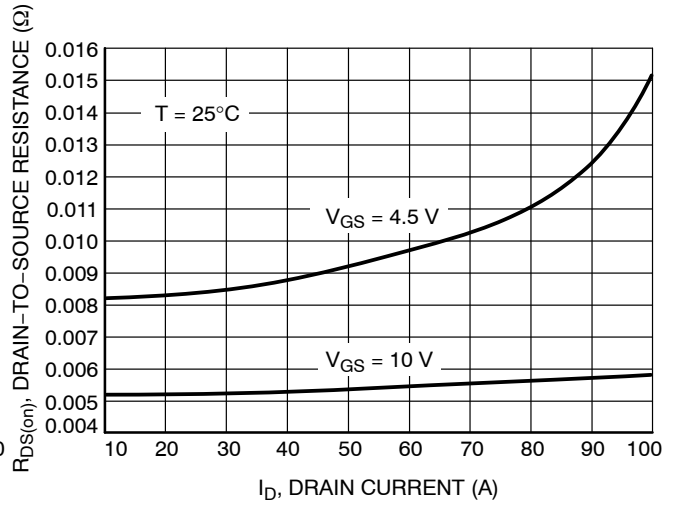


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

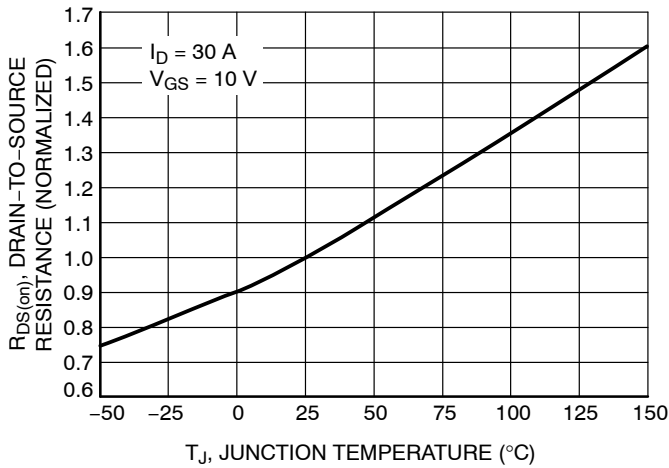


Figure 5. On-Resistance Variation with Temperature

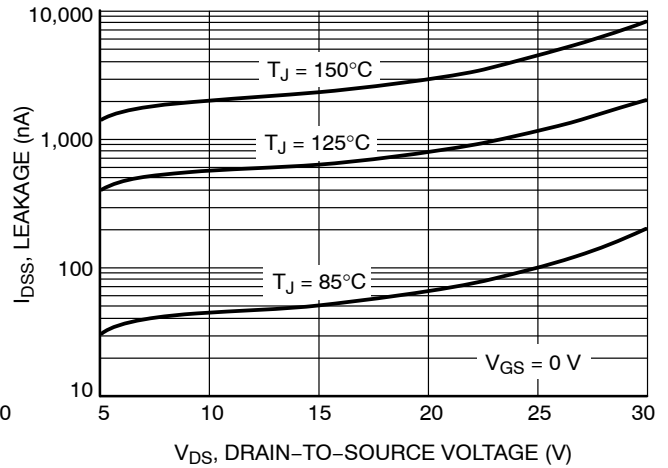


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

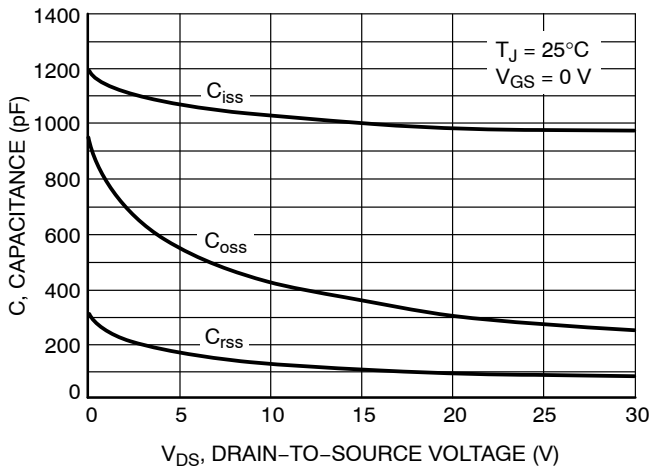


Figure 7. Capacitance Variation

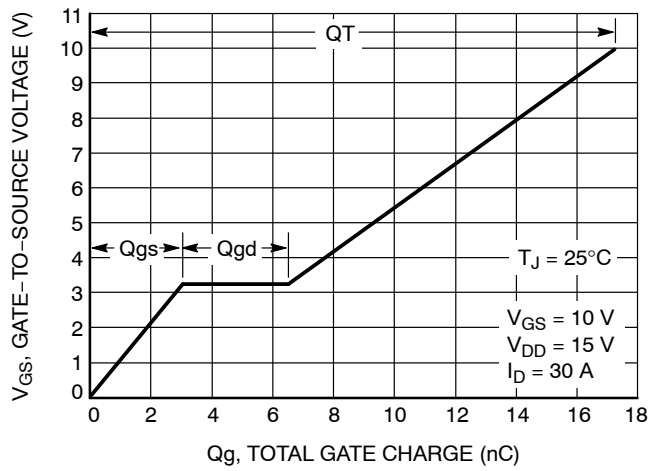


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

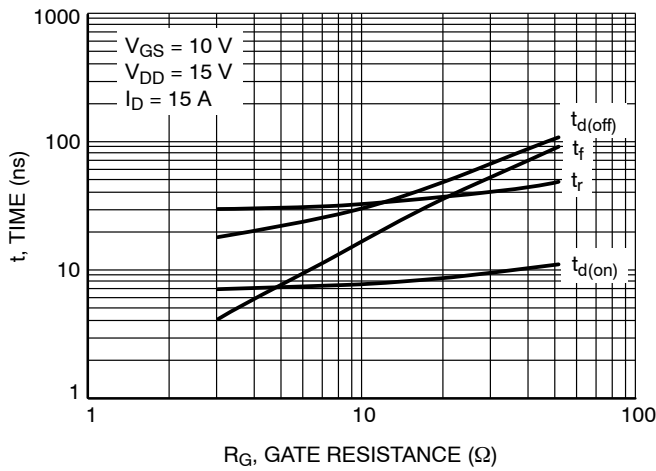


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

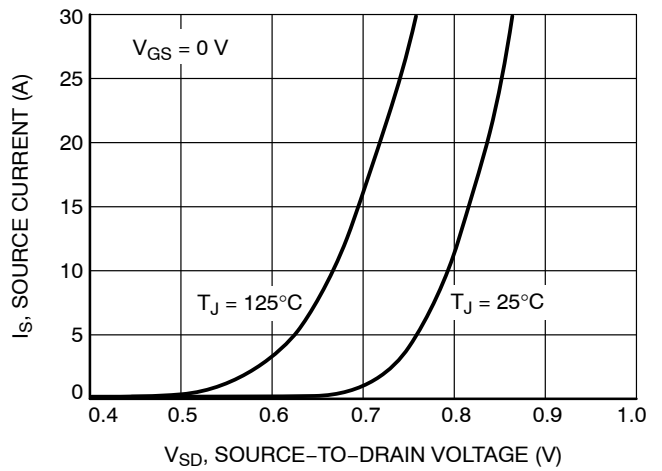


Figure 10. Diode Forward Voltage vs. Current

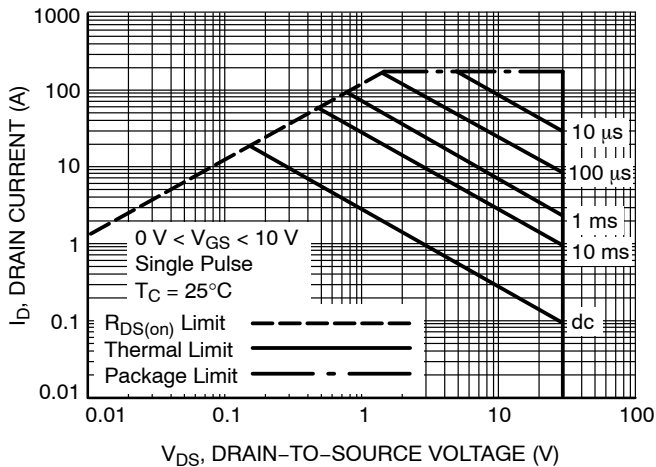


Figure 11. Maximum Rated Forward Biased Safe Operating Area

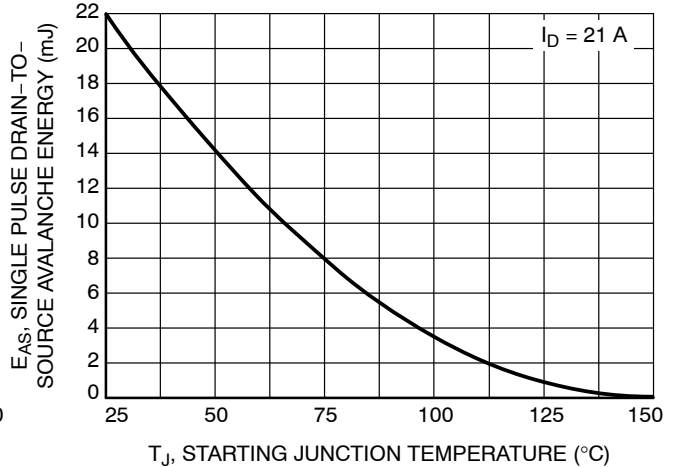


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

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## TYPICAL CHARACTERISTICS

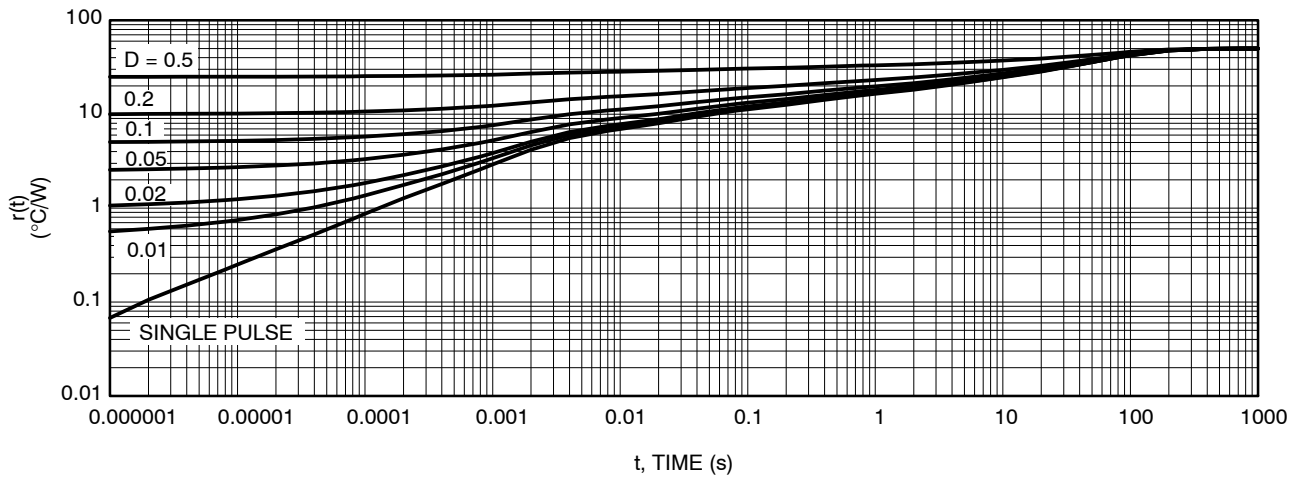
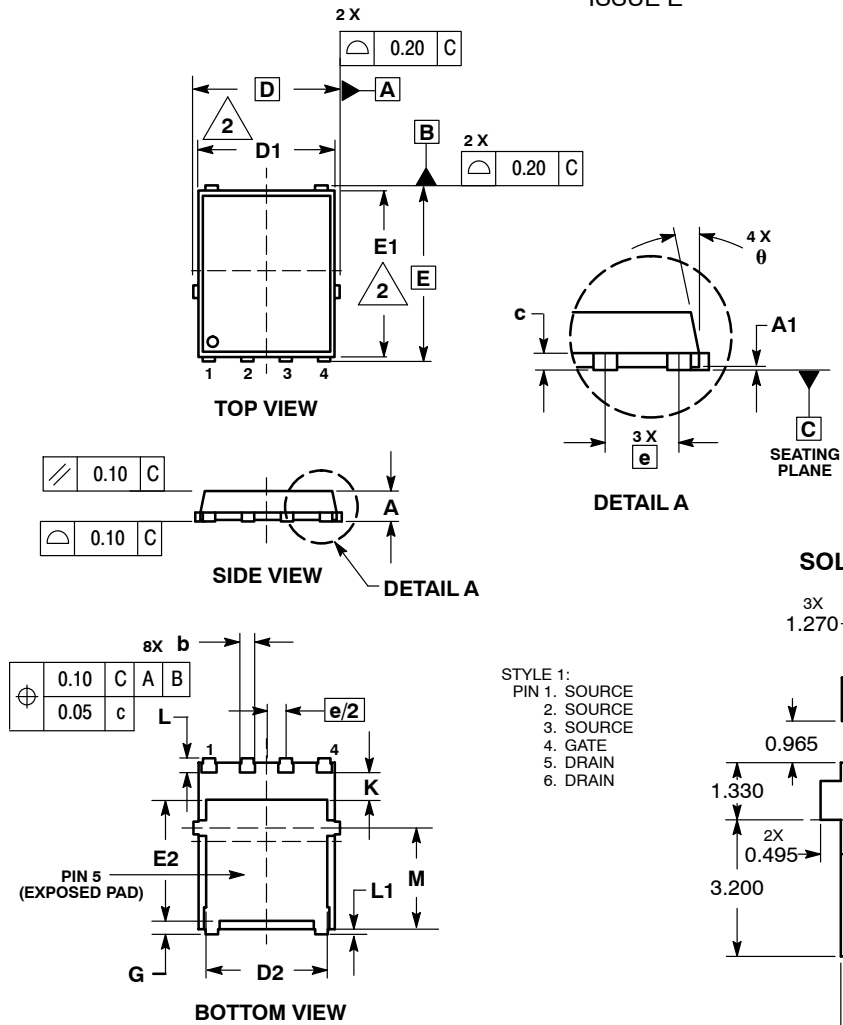


Figure 13. Thermal Response

# NTMFS4926N

## PACKAGE DIMENSIONS

DFN5 5x6, 1.27P (S08 FL)  
CASE 488AA  
ISSUE E

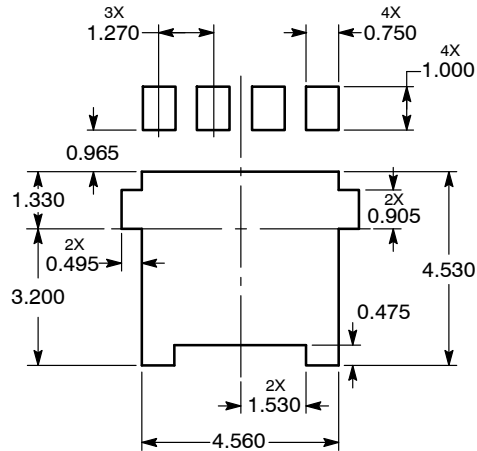


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.15 BSC		
D1	4.50	4.90	5.10
D2	3.50	---	4.22
E	6.15 BSC		
E1	5.50	5.80	6.10
E2	3.45	---	4.30
e	1.27 BSC		
G	0.51	0.61	0.71
K	0.51	---	---
L	0.51	0.61	0.71
L1	0.05	0.17	0.20
M	3.00	3.40	3.80
θ	0°	---	12°

### SOLDERING FOOTPRINT\*



- STYLE 1:  
PIN 1. SOURCE  
PIN 2. SOURCE  
PIN 3. SOURCE  
PIN 4. GATE  
PIN 5. DRAIN  
PIN 6. DRAIN

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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