

# NCV8401, NCV8401A

## Self-Protected Low Side Driver with Temperature and Current Limit

NCV8401/A is a three terminal protected Low-Side Smart Discrete device. The protection features include overcurrent, overtemperature, ESD and integrated Drain-to-Gate clamping for overvoltage protection. This device offers protection and is suitable for harsh automotive environments.

### Features

- Short Circuit Protection
- Thermal Shutdown with Automatic Restart
- Over Voltage Protection
- Integrated Clamp for Inductive Switching
- ESD Protection
- dV/dt Robustness
- Analog Drive Capability (Logic Level Input)
- AEC-Q101 Qualified and PPAP Capable
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements
- These Devices are Pb-Free and are RoHS Compliant

### Typical Applications

- Switch a Variety of Resistive, Inductive and Capacitive Loads
- Can Replace Electromechanical Relays and Discrete Circuits
- Automotive / Industrial

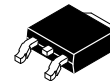
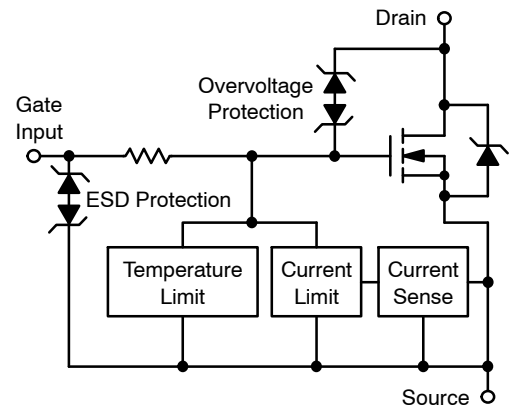


ON Semiconductor®

<http://onsemi.com>

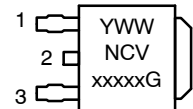
V <sub>DSS</sub> (Clamped)	R <sub>DS(ON)</sub> TYP	I <sub>D</sub> MAX (Limited)
42 V	23 mΩ @ 10 V	33 A*

\*Max current may be limited below this value depending on input conditions.



**DPAK  
CASE 369C  
STYLE 2**

### MARKING DIAGRAM



Y	= Year	1	= Gate
WW	= Work Week	2	= Drain
xxxxx	= 8401 or 8401A	3	= Source
G	= Pb-Free Package		

### ORDERING INFORMATION

Device	Package	Shipping†
NCV8401DTRKG	DPAK (Pb-Free)	2500/Tape & Reel
NCV8401ADTRKG	DPAK (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NCV8401, NCV8401A

## MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage Internally Clamped	$V_{DSS}$	42	V
Drain-to-Gate Voltage Internally Clamped ( $R_{GS} = 1.0\text{ M}\Omega$ )	$V_{DGR}$	42	V
Gate-to-Source Voltage	$V_{GS}$	$\pm 14$	V
Drain Current - Continuous	$I_D$	Internally Limited	
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 1) @ $T_A = 25^\circ\text{C}$ (Note 2)	$P_D$	1.1 2.0	W
Thermal Resistance, Junction-to-Case Junction-to-Ambient (Note 1) Junction-to-Ambient (Note 2)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	1.6 110 60	$^\circ\text{C/W}$
Single Pulse Drain-to-Source Avalanche Energy ( $V_{DD} = 25\text{ Vdc}$ , $V_{GS} = 5.0\text{ Vdc}$ , $I_L = 3.65\text{ Apk}$ , $L = 120\text{ mH}$ , $R_G = 25\ \Omega$ , $T_{Jstart} = 150^\circ\text{C}$ ) (Note 3)	$E_{AS}$	800	mJ
Load Dump Voltage ( $V_{GS} = 0$ and $10\text{ V}$ , $R_I = 2.0\ \Omega$ , $R_L = 3.0\ \Omega$ , $t_d = 400\text{ ms}$ )	$V_{LD}$	65	V
Operating Junction Temperature	$T_J$	-40 to 150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to 150	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Minimum FR4 PCB, steady state.
2. Mounted onto a 2" square FR4 board (1" square, 2 oz. Cu 0.06" thick single-sided,  $t = \text{steady state}$ ).
3. Not subject to production testing.

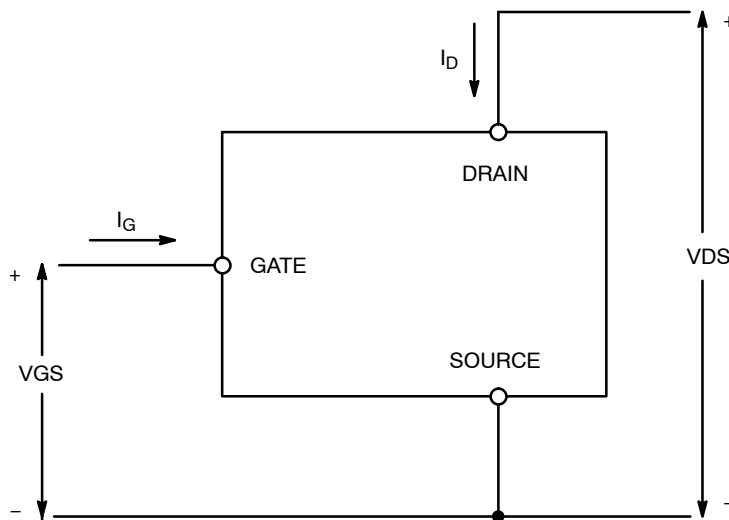


Figure 1. Voltage and Current Convention

# NCV8401, NCV8401A

## MOSFET ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Drain-to-Source Clamped Breakdown Voltage (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = 250 μAdc) (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = 250 μAdc, T <sub>J</sub> = 150°C) (Note 4)	V <sub>(BR)DSS</sub>	42 42	46 44	50 50	Vdc
Zero Gate Voltage Drain Current (V <sub>DS</sub> = 32 Vdc, V <sub>GS</sub> = 0 Vdc) (V <sub>DS</sub> = 32 Vdc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 150°C) (Note 4)	I <sub>DSS</sub>		1.5 6.5	5.0	μAdc
Gate Input Current (V <sub>GS</sub> = 5.0 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSSF</sub>		50	100	μAdc

## ON CHARACTERISTICS

Gate Threshold Voltage (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 1.2 mAdc) Threshold Temperature Coefficient	V <sub>GS(th)</sub>	1.0	1.8 5.0	2.0	Vdc -mV/°C
Static Drain-to-Source On-Resistance (Note 5) (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 5.0 Adc, T <sub>J</sub> @ 25°C) (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 5.0 Adc, T <sub>J</sub> @ 150°C) (Note 4)	R <sub>DS(on)</sub>		23 43	29 55	mΩ
Static Drain-to-Source On-Resistance (Note 5) (V <sub>GS</sub> = 5.0 Vdc, I <sub>D</sub> = 5.0 Adc, T <sub>J</sub> @ 25°C) (V <sub>GS</sub> = 5.0 Vdc, I <sub>D</sub> = 5.0 Adc, T <sub>J</sub> @ 150°C) (Note 4)	R <sub>DS(on)</sub>		28 50	34 60	mΩ
Source-Drain Forward On Voltage (I <sub>S</sub> = 5 A, V <sub>GS</sub> = 0 V)	V <sub>SD</sub>		0.80	1.1	V

## SWITCHING CHARACTERISTICS (Note 4)

Turn-ON Time (10% V <sub>IN</sub> to 90% I <sub>D</sub> )	V <sub>IN</sub> = 0 V to 5 V, V <sub>DD</sub> = 25 V I <sub>D</sub> = 1.0 A, Ext R <sub>G</sub> = 2.5 Ω	t <sub>ON</sub>	41	50	μs
Turn-OFF Time (90% V <sub>IN</sub> to 10% I <sub>D</sub> )		t <sub>OFF</sub>	129	150	
Turn-ON Time (10% V <sub>IN</sub> to 90% I <sub>D</sub> )	V <sub>IN</sub> = 0 V to 10 V, V <sub>DD</sub> = 25 V, I <sub>D</sub> = 1.0 A, Ext R <sub>G</sub> = 2.5 Ω	t <sub>ON</sub>	16	25	
Turn-OFF Time (90% V <sub>IN</sub> to 10% I <sub>D</sub> )		t <sub>OFF</sub>	164	180	
Slew-Rate ON (20% V <sub>DS</sub> to 50% V <sub>DS</sub> )	V <sub>in</sub> = 0 to 10 V, V <sub>DD</sub> = 12 V, R <sub>L</sub> = 4.7 Ω	-dV <sub>DS</sub> /dt <sub>ON</sub>	1.27		V/μs
Slew-Rate OFF (80% V <sub>DS</sub> to 50% V <sub>DS</sub> )		dV <sub>DS</sub> /dt <sub>OFF</sub>	0.36		

## SELF PROTECTION CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Current Limit	V <sub>GS</sub> = 5.0 V, V <sub>DS</sub> = 10 V V <sub>GS</sub> = 5.0 V, T <sub>J</sub> = 150°C (Note 4)	I <sub>LIM</sub>	25 11	30 16	35 21	Adc
	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 10 V V <sub>GS</sub> = 10 V, T <sub>J</sub> = 150°C (Note 4)		30 18	35 25	40 28	
Temperature Limit (Turn-off)	V <sub>GS</sub> = 5.0 V (Note 4)	T <sub>LIM(off)</sub>	150	175	200	°C
Thermal Hysteresis	V <sub>GS</sub> = 5.0 V	ΔT <sub>LIM(on)</sub>		15		°C
Temperature Limit (Turn-off)	V <sub>GS</sub> = 10 V (Note 4)	T <sub>LIM(off)</sub>	150	165	185	°C
Thermal Hysteresis	V <sub>GS</sub> = 10 V	ΔT <sub>LIM(on)</sub>		15		°C

## GATE INPUT CHARACTERISTICS (Note 4)

Device ON Gate Input Current	V <sub>GS</sub> = 5 V I <sub>D</sub> = 1.0 A	I <sub>GON</sub>		50		μA
	V <sub>GS</sub> = 10 V I <sub>D</sub> = 1.0 A			400		
Current Limit Gate Input Current	V <sub>GS</sub> = 5 V, V <sub>DS</sub> = 10 V	I <sub>GCL</sub>		0.1		mA
	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 10 V			0.7		
Thermal Limit Fault Gate Input Current	V <sub>GS</sub> = 5 V, V <sub>DS</sub> = 10 V	I <sub>GTL</sub>		0.6		mA
	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 10 V			2.0		

## ESD ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted) (Note 4)

Electro-Static Discharge Capability Human Body Model (HBM) Machine Model (MM)	ESD	4000 400			V
---	-----	-------------	--	--	---

4. Not subject to production testing.  
5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL PERFORMANCE CURVES

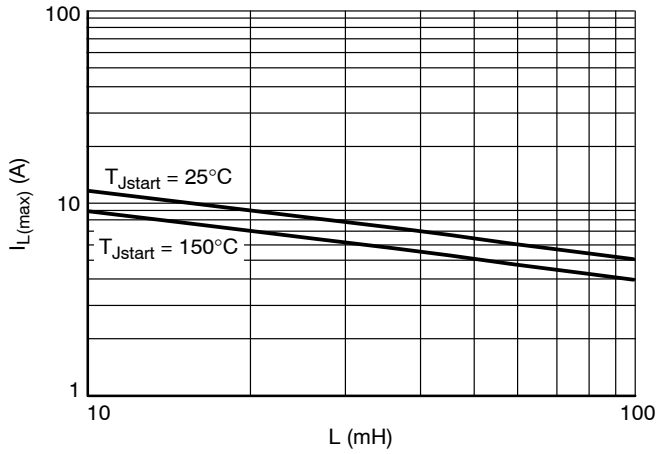


Figure 2. Single Pulse Maximum Switch-off Current vs. Load Inductance

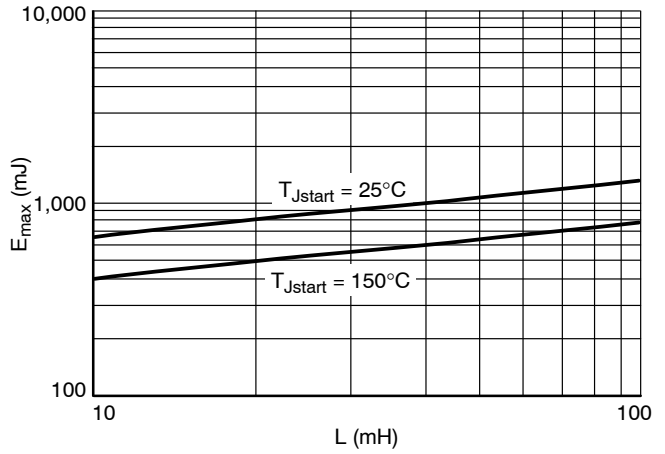


Figure 3. Single Pulse Maximum Switching Energy vs. Load Inductance

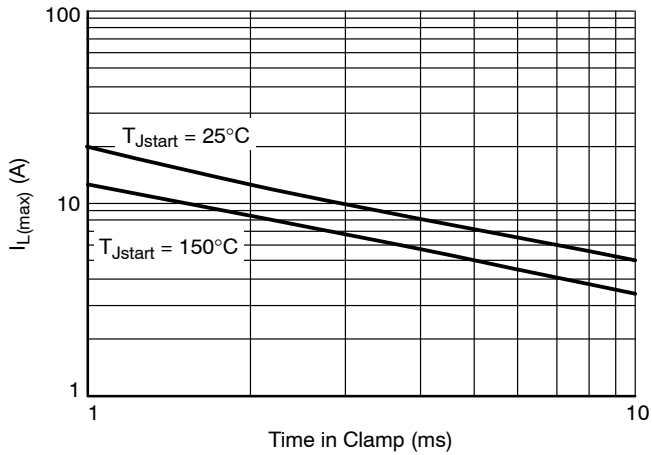


Figure 4. Single Pulse Maximum Inductive Switch-off Current vs. Time in Clamp

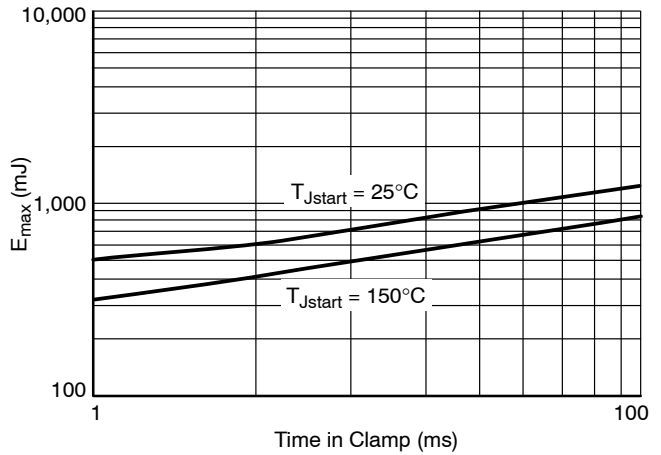


Figure 5. Single Pulse Maximum Inductive Switching Energy vs. Time in Clamp

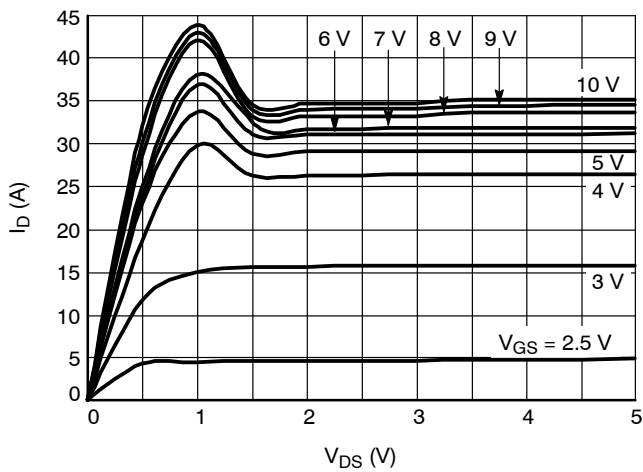


Figure 6. On-state Output Characteristics at 25°C

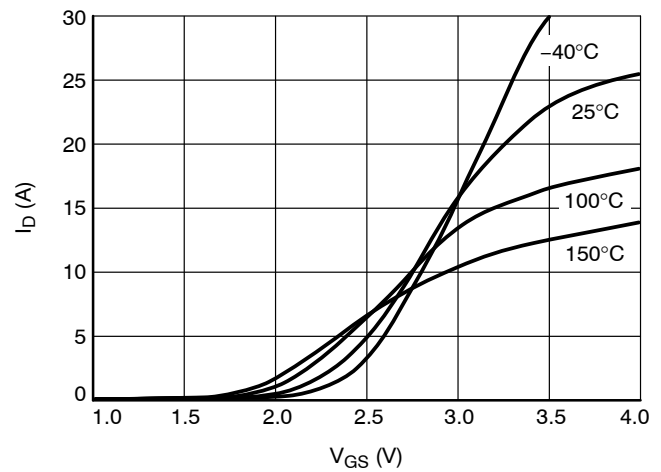


Figure 7. Transfer Characteristics ( $V_{DS} = 10\text{ V}$ )

# NCV8401, NCV8401A

## TYPICAL PERFORMANCE CURVES

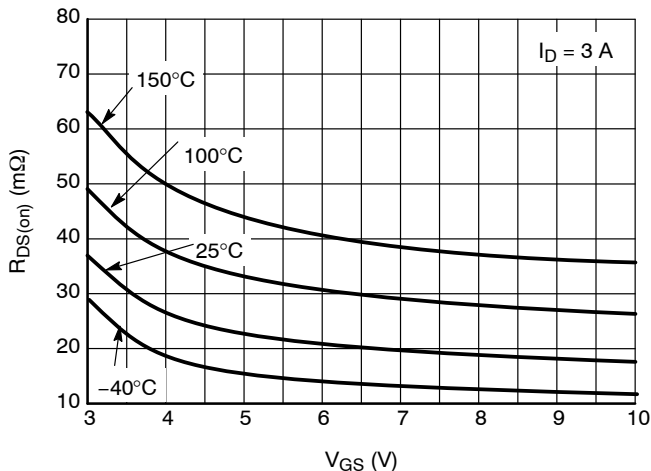


Figure 8.  $R_{DS(on)}$  vs. Gate-Source Voltage

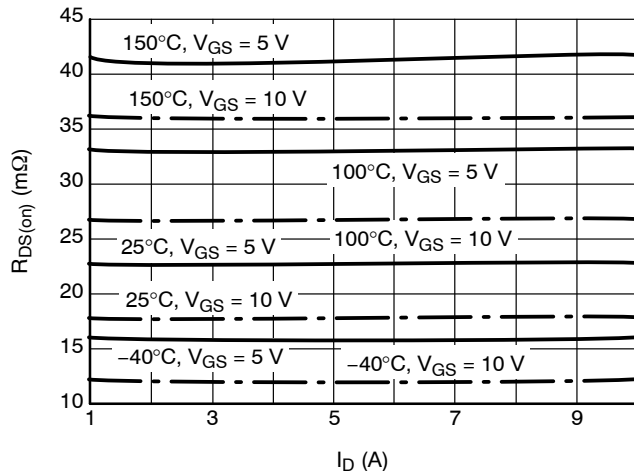


Figure 9.  $R_{DS(on)}$  vs. Drain Current

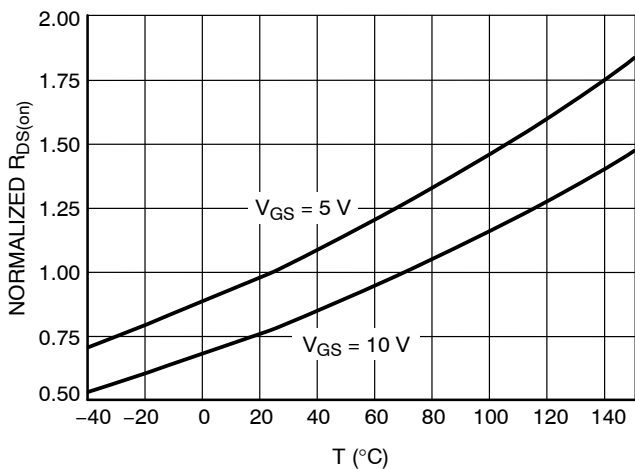


Figure 10. Normalized  $R_{DS(on)}$  vs. Temperature ( $I_D = 5 A$ )

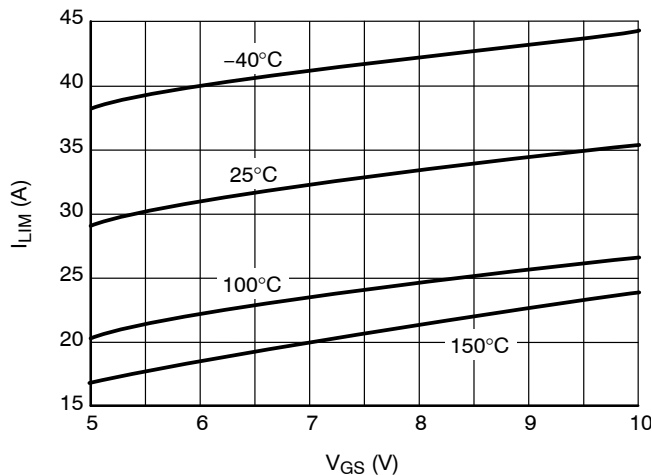


Figure 11. Current Limit vs. Gate-Source Voltage ( $V_{DS} = 10 V$ )

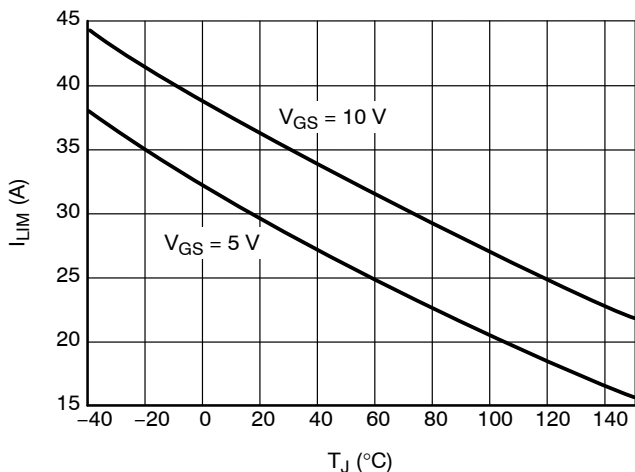


Figure 12. Current Limit vs. Junction Temperature ( $V_{DS} = 10 V$ )

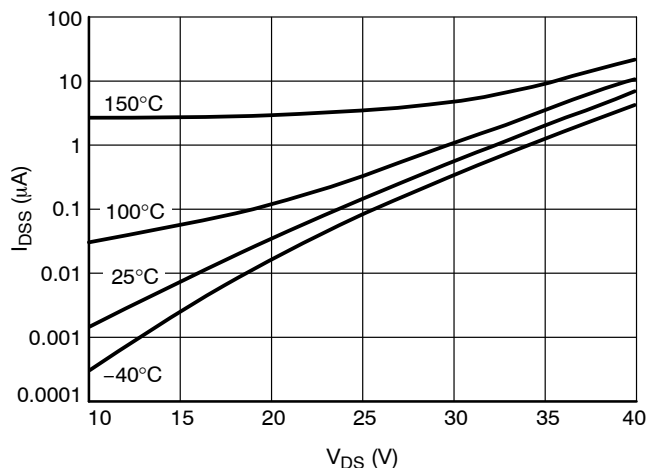


Figure 13. Drain-to-Source Leakage Current ( $V_{GS} = 0 V$ )

TYPICAL PERFORMANCE CURVES

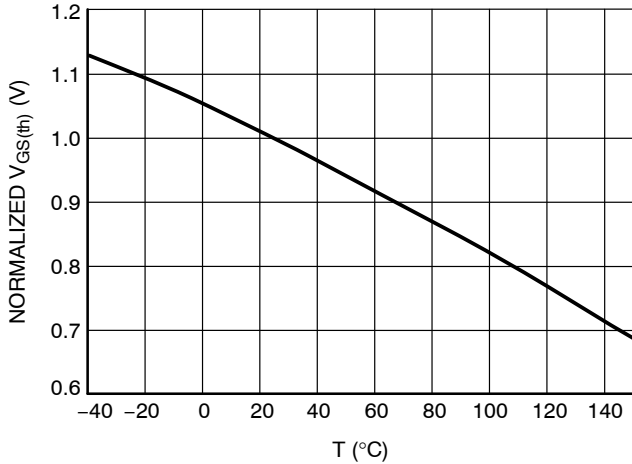


Figure 14. Normalized Threshold Voltage vs. Temperature ( $I_D = 1.2 \text{ mA}$ ,  $V_{DS} = V_{GS}$ )

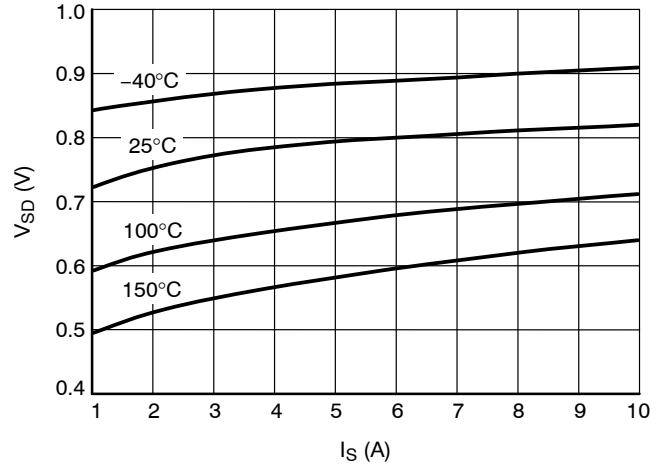


Figure 15. Source-Drain Diode Forward Characteristics ( $V_{GS} = 0 \text{ V}$ )

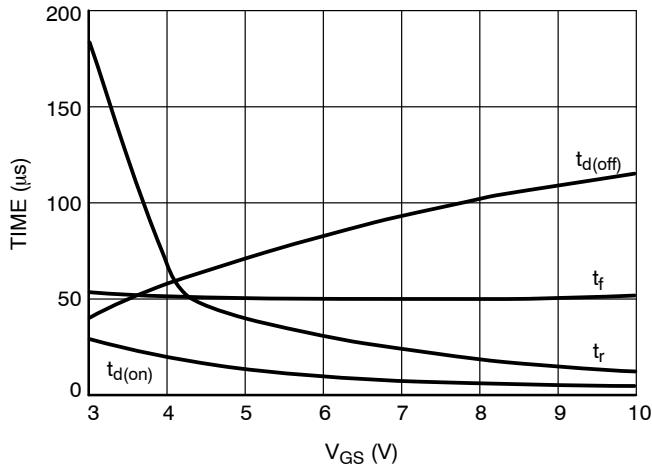


Figure 16. Resistive Load Switching Time vs. Gate-Source Voltage ( $V_{DD} = 25 \text{ V}$ ,  $I_D = 5 \text{ A}$ ,  $R_G = 0 \Omega$ )

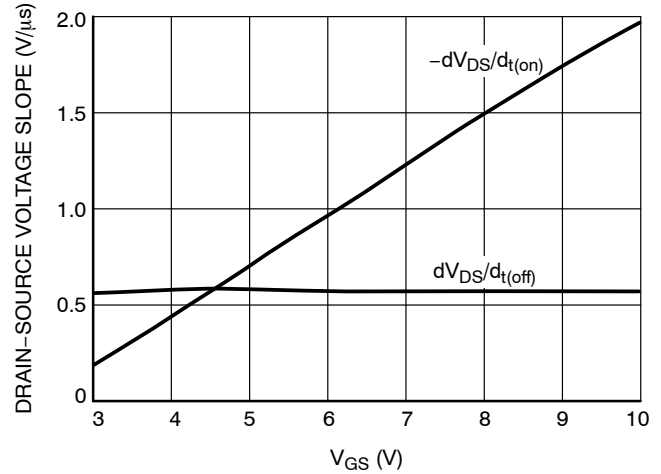


Figure 17. Resistive Load Switching Drain-Source Voltage Slope vs. Gate-Source Voltage ( $V_{DD} = 25 \text{ V}$ ,  $I_D = 5 \text{ A}$ ,  $R_G = 0 \Omega$ )

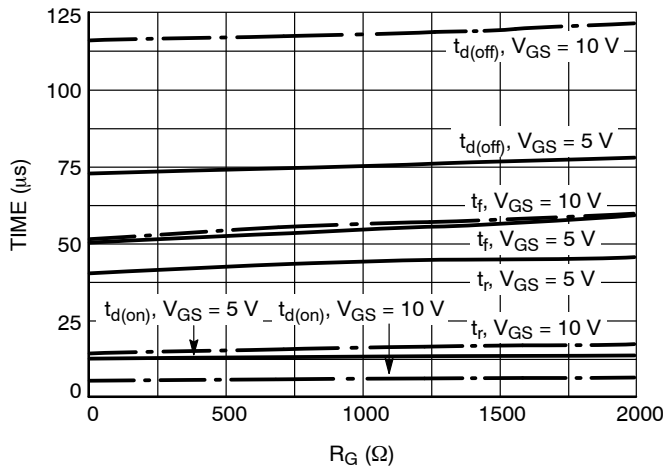


Figure 18. Resistive Load Switching Time vs. Gate Resistance ( $V_{DD} = 25 \text{ V}$ ,  $I_D = 5 \text{ A}$ )

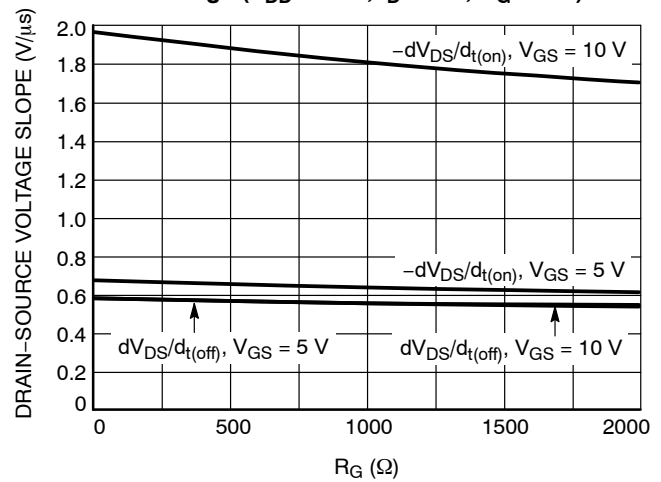


Figure 19. Drain-Source Voltage Slope during Turn On and Turn Off vs. Gate Resistance ( $V_{DD} = 25 \text{ V}$ ,  $I_D = 5 \text{ A}$ )

# NCV8401, NCV8401A

## TYPICAL PERFORMANCE CURVES

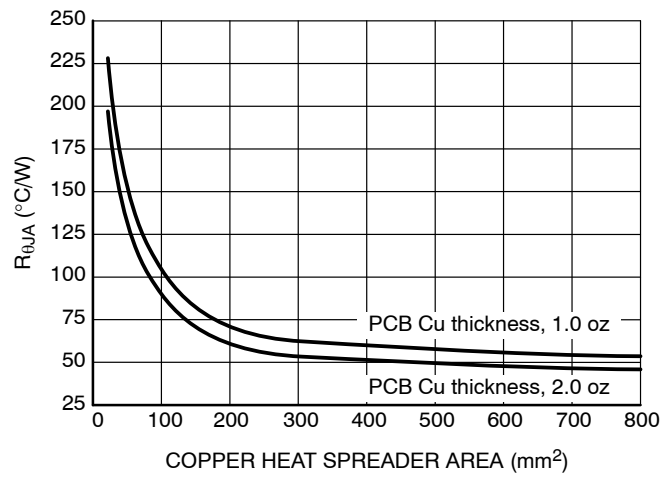


Figure 20.  $R_{\theta JA}$  vs. Copper Area

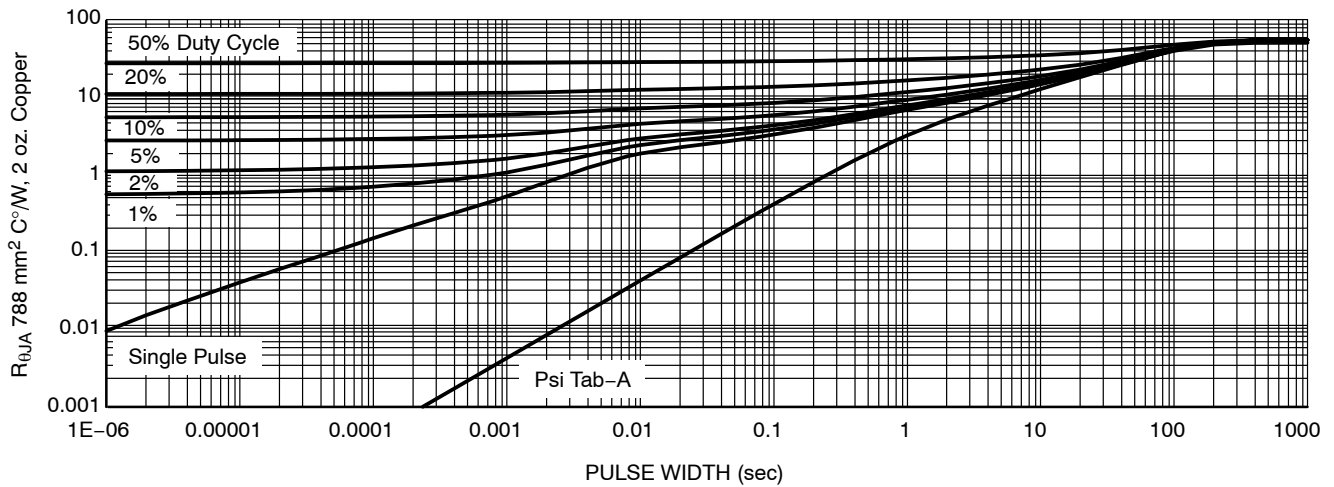


Figure 21. Transient Thermal Resistance

# NCV8401, NCV8401A

## TEST CIRCUITS AND WAVEFORMS

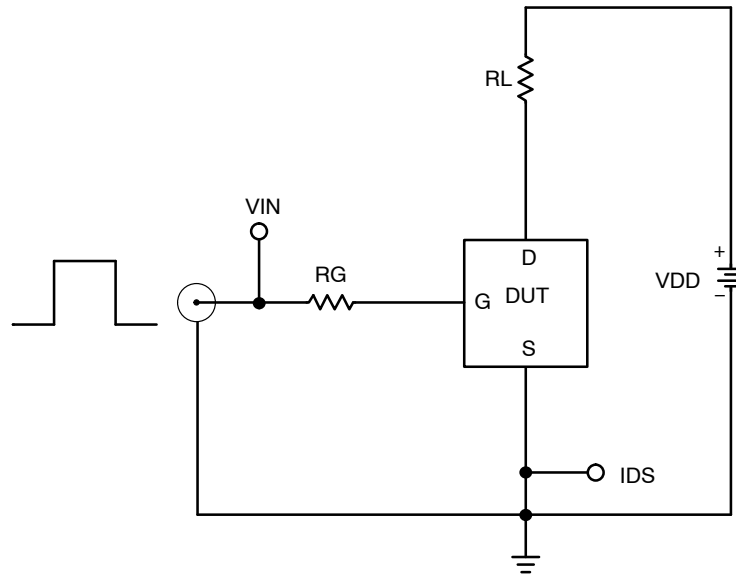


Figure 22. Resistive Load Switching Test Circuit

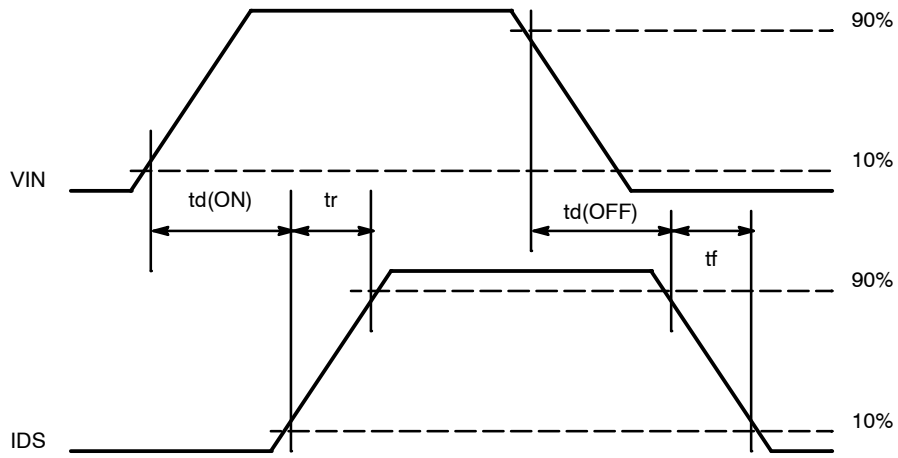


Figure 23. Resistive Load Switching Waveforms

# NCV8401, NCV8401A

## TEST CIRCUITS AND WAVEFORMS

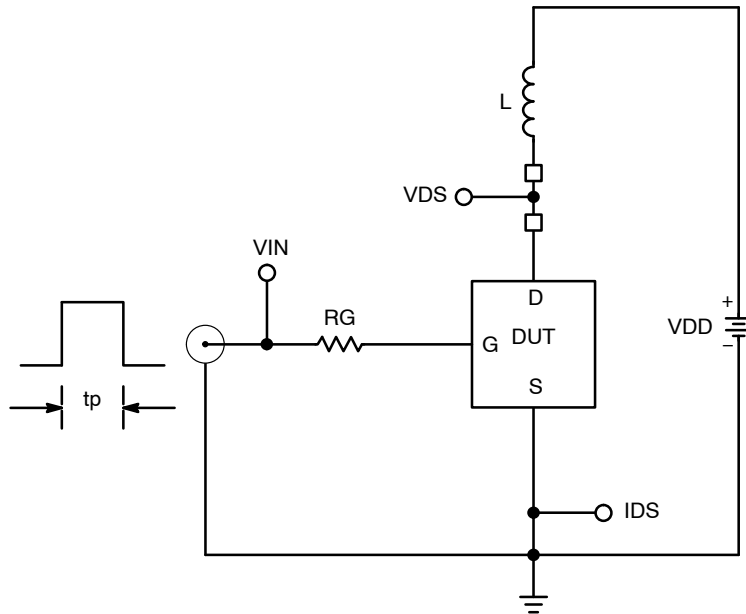


Figure 24. Inductive Load Switching Test Circuit

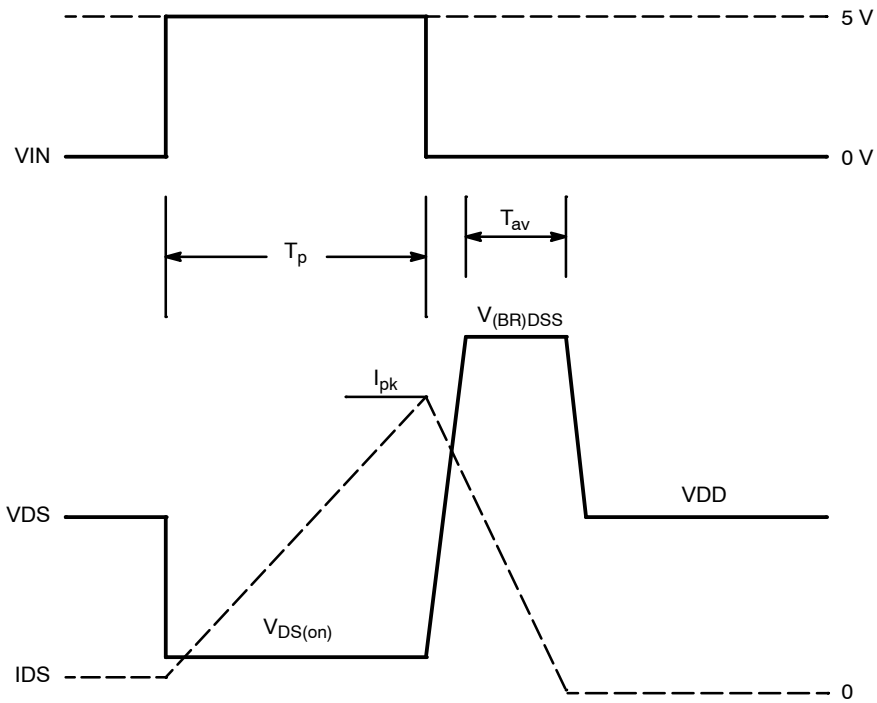
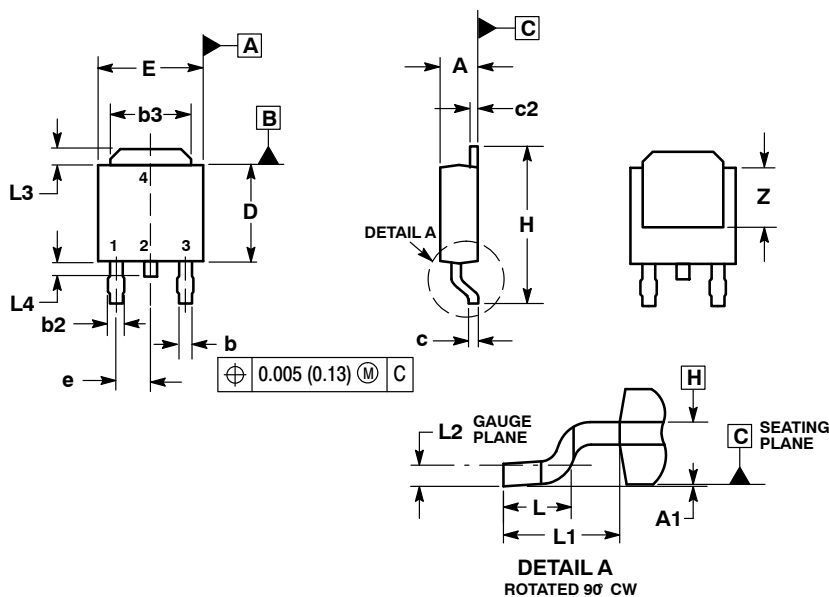


Figure 25. Inductive Load Switching Waveforms

# NCV8401, NCV8401A

## PACKAGE DIMENSIONS

### DPAK CASE 369C ISSUE D



#### NOTES:

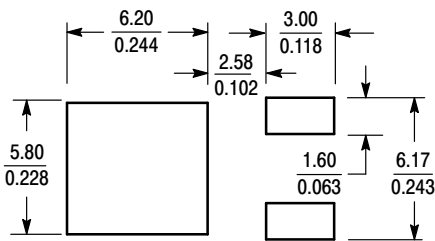
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

#### STYLE 2:

- PIN 1. GATE
- DRAIN
- SOURCE
- DRAIN

### SOLDERING FOOTPRINT\*



SCALE 3:1 (mm/inches)

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

HDPlus is a trademark of Semiconductor Components Industries, LLC (SCILLC).

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)

**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative