

NCP392D

Adjustable Front End Overvoltage Protection Controller with Protected Vbus Output

The NCP392D is an overvoltage front end protection controller and is able to disconnect the systems from its output pin in case wrong input operating conditions are detected, up to +28 V. Thanks to this device using internal NMOS, no external device is necessary, reducing the system cost and the PCB area of the application board.

Internal OVLO threshold is available, or can be adjusted if an external resistor bridge is used.

At power up ($\overline{\text{EN}}$ pin = low level), the Vout turns on tstart time after internal timer elapsed.

The NCP392D features an $\overline{\text{ACOK}}$ pin that indicates faulty condition.

Features

- Over-voltage Protection Up to + 28 V
- On-chip Low $R_{\text{DS(on)}}$ NMOS Transistors: Typical 34 m Ω
- Over-voltage Lockout (OVLO)
- Externally Adjustable OVLO
- Internal 15 ms Startup Delay
- Shutdown $\overline{\text{EN}}$ Input
- $\overline{\text{ACOK}}$ Status Pin
- + 100 V Surge Capability, in Compliance with IEC61000-4-5 Standard
- Compliance to IEC61000-4-2 (Level 4) Standard
 - 8 kV (Contact)
 - 15 kV (Air)
- ESD Ratings:
 - Machine Model = B (200 V)
 - Human Body Model = 2 (2 kV)
- CSP-12 Package 1.3 x 2.0 mm, 0.4 mm Pitch
- This is a Pb-Free Device

Typical Applications

- Cell Phones
- Tablets
- Camera Phones
- Digital Still Cameras
- Personal Digital Applications



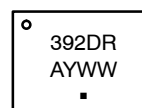
ON Semiconductor®

www.onsemi.com



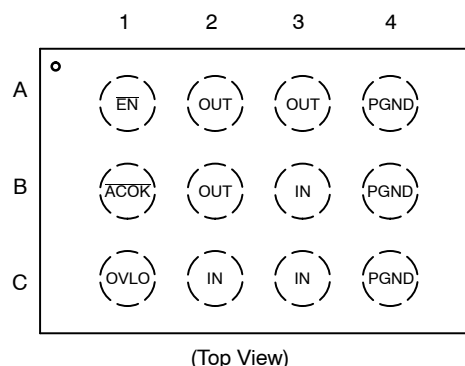
WLCSP 12
FCC SUFFIX
CASE 567JM

MARKING DIAGRAM



392DR = Specific Device Number
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

PIN CONNECTION



ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 9 of this data sheet.

NCP392D

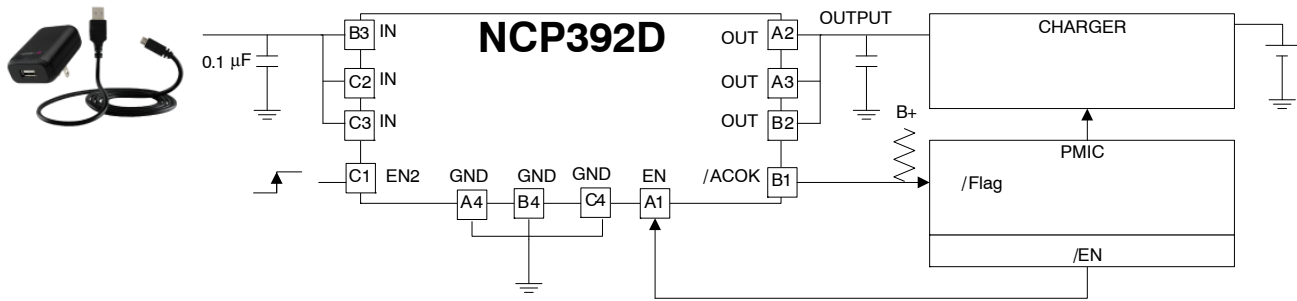


Figure 1. Typical Application Circuit

FUNCTIONAL BLOCK DIAGRAM

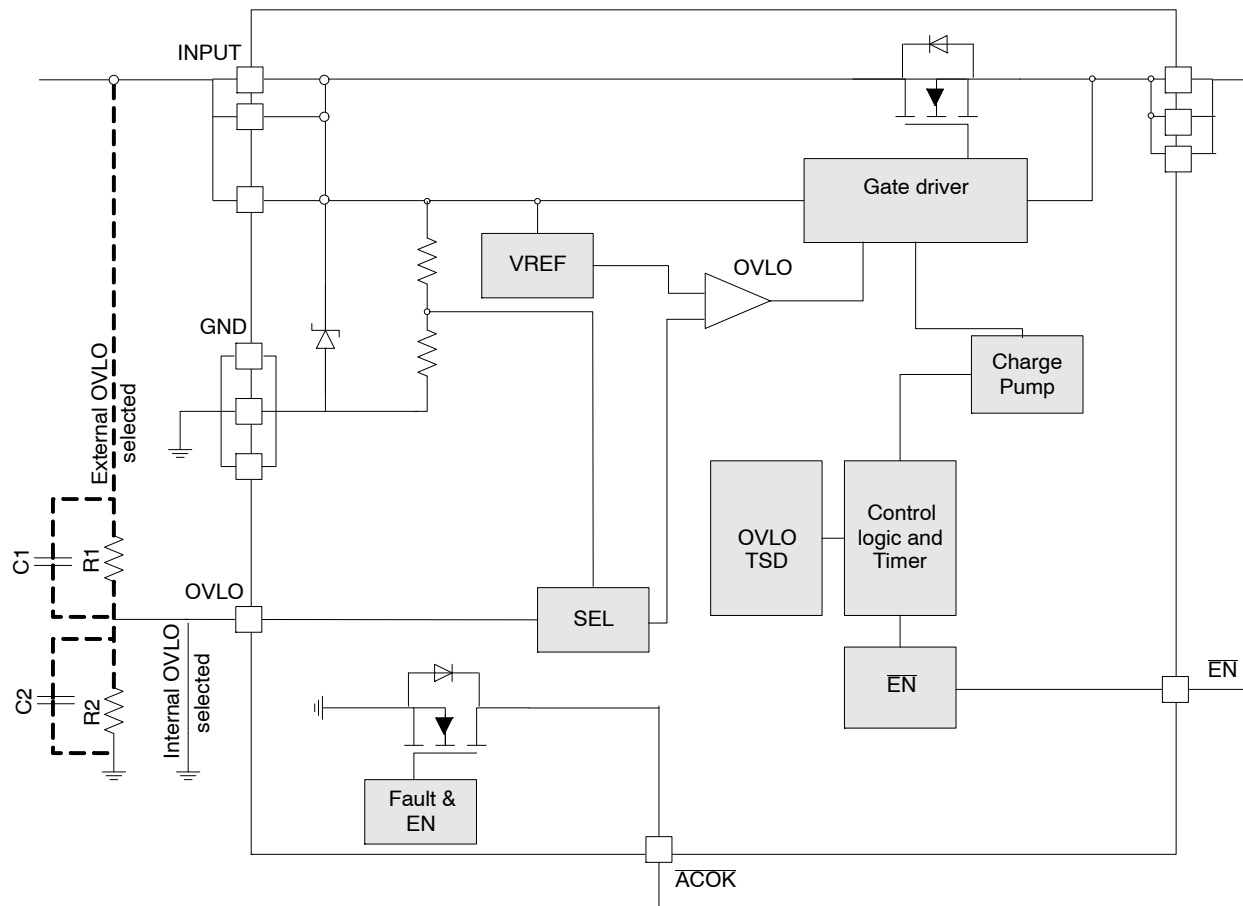


Figure 2. Functional Block Diagram

NCP392D

PIN FUNCTION DESCRIPTION

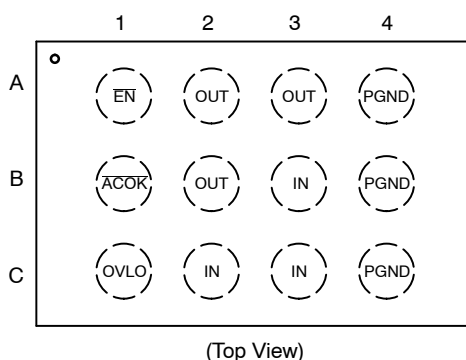


Figure 3. Pinout

Table 1. NCP392 PIN DESCRIPTION

Pin	Pin Name	Type	Description		
A1	EN	I/O	Enable pin bar. The device enters in shutdown mode when this pin is tied to a high level. In this case the output is disconnected from the input. To allow normal functionality, the EN pin is tied low with internal pull down.		
A2, A3, B2	OUT	OUTPUT	Output voltage pins. These pins follow IN pins, with debounce time, when “no fault” are detected. The outputs are disconnected from the Vin power supply when the input voltage is below UVLO, above OVLO threshold or internal thermal protection is exceeded. The three OUT pins must be hardwired together and used for power dissipation.		
A4, B4, C4	PGND	POWER	Ground. The three GND pins must be hardwired together and connect to the system GND.		
B1	ACOK	OUTPUT	ACOK pin: fault indication pin. Open drain. This pin is tied low if Vin is within UVLO and OVLO range.	1	$V_{IN} < V_{UVLO}$ or $V_{IN} \geq V_{OVLO}$
				0	Voltage stable
B3, C2, C3	IN	POWER	Input voltage pins. These pins are connected to the power supply. The three IN pins must be hardwired together.		
C1	OVLO	INPUT	External OVLO Adjustment. Connect external resistor bridge to OVLO pin to select a different OVLO threshold. Connect OVLO pin to GND if not used. In this case internal OVLO will be selected.		

Table 2. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Minimum Voltage (IN, OVLO to GND)	V _{minIN}	–0.3	V
Minimum Voltage (All others to GND)	V _{min}	–0.3	V
Maximum Voltage (IN to GND)	V _{maxIN}	29	V
Maximum Voltage (OVLO to GND)	V _{maxOVLO}	14	V
Maximum Voltage (OUT to GND)	V _{maxOUT}	22	V
Maximum Voltage (All others to GND)	V _{max}	7	V
Maximum DC current	I _{max}	4.5	A
Peak input current	I _{peak}	8	A
Thermal Resistance, Junction–to–Air	R _{θJA}	70	°C/W
Operating Ambient Temperature Range	T _A	–40 to +85	°C
Storage Temperature Range	T _{stg}	–65 to +150	°C
Junction Operating temperature	T _J	+ 125	°C
ESD Withstand Voltage (IEC 61000–4–2) Human Body Model (HBM), model = 2 (Note 1) Machine Model (MM) model = B (Note 2)	V _{esd}	15 kV air, 8 kV contact 2000 V 200 V	kV V V
Moisture Sensitivity	MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Human Body Model, 100 pF discharged through a 1.5 kΩ resistor following specification JESD22/A114.
2. Machine Model, 200 pF discharged through all pins following specification JESD22/A115

NCP392D

Table 3. ELECTRICAL CHARACTERISTICS

Min / Max limits values ($-40^{\circ}\text{C} < T_A < +85^{\circ}\text{C}$) and $V_{IN} = +5\text{ V}$ (Unless otherwise noted). Typical values are $T_A = +25^{\circ}\text{C}$.

Characteristics	Symbols	Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{in}, V_{OVLO}		2.8		28	V
Under voltage Lockout	UVLO	V_{in} rising			2.8	V
Under voltage Lockout hysteresis	UVLO _{hyst}	V_{in} falling	–	60	–	mV
Internal Over voltage Lockout threshold	OVLO	V_{in} rising (Note 3) OVLO pin tied to GND – 25°C	6.6	6.8	7.0	V
Internal Over voltage Lockout hysteresis	OVLO _{hyst}	V_{in} falling (Note 3) OVLO pin tied to GND – 25°C	1.5		2.5	%
External OVLO Reference	OVLO_EXT	NCP392DR	1.18	1.221	1.26	V
External Adjustable OVLO			4		20	V
Over-Voltage Lockout Hysteresis	OVLO _{EXThyst}	V_{in} falling		2		%
External OVLO select threshold	OVLO _{SEL}		0.2		0.3	V
Vin versus Vout Resistance	R_{DSon}	$V_{in} = 5\text{ V}, \overline{EN} = \text{GND}, -40^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$		34	50	m Ω
Supply Quiescent Current	I_{DD}	No load, $\overline{EN} = 0.4\text{ V}$		58	100	μA
Standby Current	I_{STB}	No load, $\overline{EN} = 1.2\text{ V}$,			6	μA
OVLO Supply current	I_{IN_OVLO}	$V_{OVLO} = 3\text{ V}, V_{IN} = 5\text{ V}, V_{OUT} = 0\text{ V}$		60	100	μA
OVLO select leakage	I_{OVLO}				100	nA

LOGIC

EN Voltage High	V_{IH}		1.2			V
EN Voltage Low	V_{IL}				0.4	V
ACOK Output Low Voltage	V_{OL}	$I_{SINK} = 1\text{ mA}$		0.4		V

TIMINGS

Start up time	t_{START}	From $V_{in} > 2.8\text{ V}$ to 10% V_{out} , \overline{EN} low		15		ms
Enable time	t_{EN}	V_{in} present, From \overline{EN} high to low, 10% V_{out}		15		ms
Soft Start	t_{RISE}	From 10% to 90% of V_{out} , C load 100 μF , Rload, 100 Ω , \overline{EN} low		1		ms
ACOK Start up time	t_{START2}	From Vin Valid to ACOK tied low, \overline{EN} low or high		30		ms
Turn off time	t_{OFF}	Surge off time		100		ns
Disable time	t_{DIS}	From $\overline{EN} > 1.2\text{ V}$ to 90% V_{out} . No load		20		μs
OVLO Turn off time	t_{OVLO}	V_{in} rising 2 V/ μs		1.5		μs

TSD

Thermal shutdown	TSD			140		$^{\circ}\text{C}$
Thermal shutdown rearming	TSD rearm			115		$^{\circ}\text{C}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Please contact your ON Semiconductor representative for additional OVLO threshold.

Electrical parameters are guaranteed by correlation across the full range of temperature.

Operation

The NCP392D provides over-voltage protection for positive voltage surge, up to + 28 V. An additional clamp, between IN and GND, protects the part against surge test, in compliance with IEC 61000-4-5 standard.

A $\overline{\text{ACOK}}$ open drain fault indicator is provided. This signal indicates whether input voltage is within the valid range.

Under-voltage Lockout (UVLO)

To ensure proper operation under any conditions, the device has a built-in under-voltage lock out (UVLO) circuit. This circuit has a built-in hysteresis to provide noise immunity to transient conditions.

Over-voltage Lockout (OVLO)

To protect connected systems on Vout pin from over-voltage, the device has a built-in over-voltage lock out (OVLO) circuit. During over-voltage condition, the output remains disabled until the input voltage is above OVLO – hysteresis.

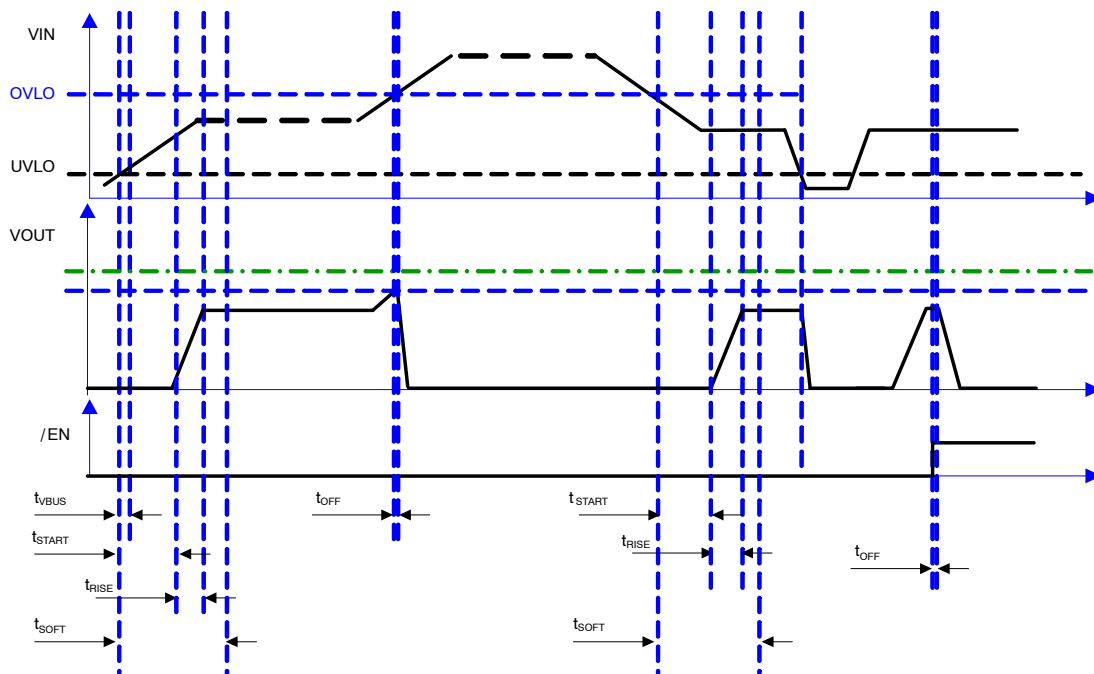


Figure 4. UVLO, OVLO and $\overline{\text{EN}}$ Functionality

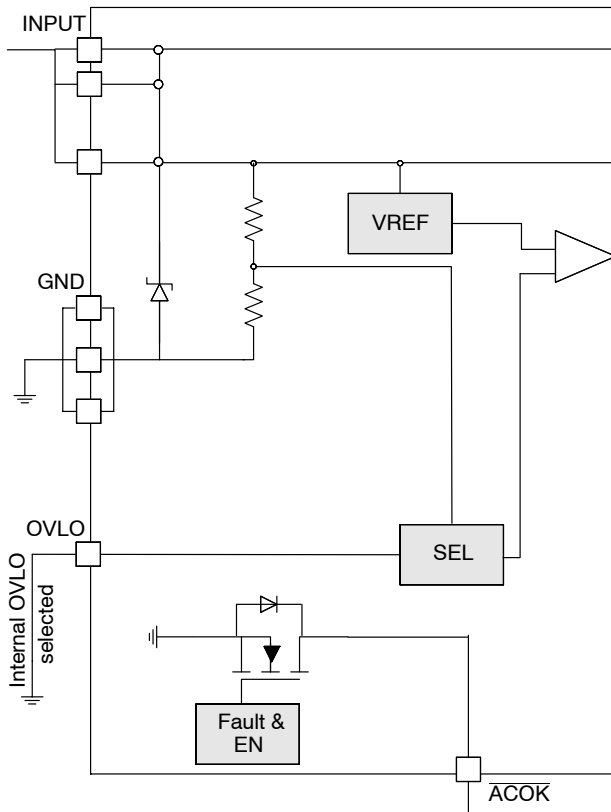


Figure 5. External Connection to GND of OVLO

If OVLO pin is not grounded, and by adding external bridge resistor on OVLO pin, between IN and GND, overvoltage protection can be adjusted as following:

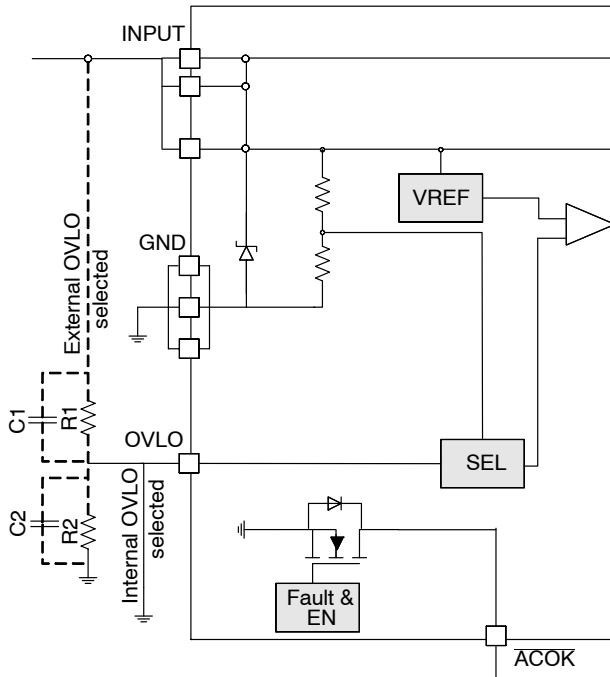


Figure 6. External Connection to Resistor Bridge of OVLO

$$NEW_OVLO_{TH} = \frac{OVLO_{EXT} \times (R_1 + R_2)}{R_2} \quad (\text{eq. 1})$$

With: $OVLO_{EXT} = 1.221 \text{ V}$ Typical (OVLO External Reference)

Example:

NEW_OVLO_{TH} target 12 V.

(eq. 2)

$$R_1 = R_2 \times \left(\frac{OVLO}{1.221} - 1 \right) = R_2 \times \left(\frac{12}{1.221} - 1 \right) = 8.828 \times R_2$$

Taking into account external input bridge doesn't have excessive current consumption, and 1% is recommended:

R_2 arbitrarily fixed at $1.05 \text{ M}\Omega$.

$R_1 = 9.269 \text{ M}\Omega$ ($9.31 \text{ M}\Omega$ standard value)

Obtained typical $OVLO = 12.04 \text{ V}$

C_1 and C_2 should be selected in such a way that the time constant $R_1 C_1 = R_2 C_2$.

EN Input

To enable normal operation, the \overline{EN} pin has to be at low level. Internal pull down is embedded in the part.

A high level on the pin, disconnects OUT pin from IN pin.

Table 4. CONTROL LOGIC MODES

OVP State NCP392D		OVLO EXT	
		Low	High
EN	Low	ON $T_{start} 15 \text{ ms}$	OFF
	High	OFF	OFF

NCP392D

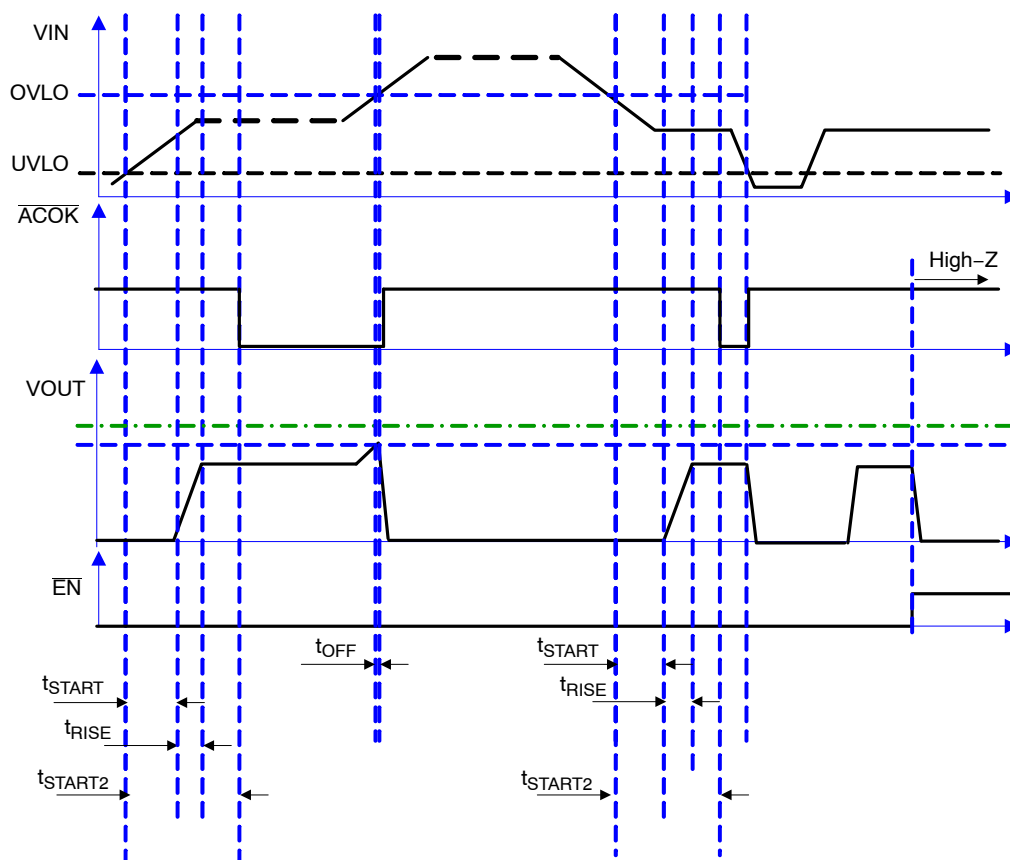


Figure 7. $\overline{\text{EN}}$ and $\overline{\text{ACOK}}$ Associated Timers

$\overline{\text{ACOK}}$ Pin

The NCP392D version integrates a $\overline{\text{ACOK}}$ status indicator. This is an open drain pin tied low when no fault is present (no TSD, no under voltage, no over voltage).

When disabled, the $\overline{\text{ACOK}}$ feature is disabled too and the output pin is in high impedance mode.

Thermal Shutdown Protection

In case of internal overheating, the integrated thermal shutdown (TSD) protection allows to open the internal MOSFET in order to instantaneously decrease the device temperature.

Embedded hysteresis allows to reengage the MOSFET when the junction temperature decreases.

If the fault event is still present, the temperature increases again and engages the thermal shutdown one more time until fault event disappeared.

PCB Recommendations

To limit internal power dissipation, PCB routing must be carefully done to improve current capability.

The NCP392D is declined in a CSP package. So power dissipation can be decreased on each pin connection but main thermal area must be as large as possible around IN and OUT pins. Taking into account and respectively, four IN and OUT pins must be hardwired together on the PCB.

Maximum power dissipation can be calculated with the following formula:

$$T_J - T_A = R_{\theta JA} \times P_d \quad (\text{eq. 3})$$

T_J : junction temperature

T_A : ambient temperature

$R_{\theta JA}$: thermal resistance of the junction to air through the case and board.

P_d : power dissipation = $R_{DS(on)} \times I^2$

ESD Tests

The NCP392D fully supports the IEC61000-4-2, level 4 (Input pin, 1 μF mounted on board).

That means, in Air condition, V_{in} has a ± 15 kV ESD protected input. In Contact condition, V_{in} has ± 8 kV ESD protected input.

Please refer to Figure 8 to see the IEC 61000-4-2 electrostatic discharge waveform.

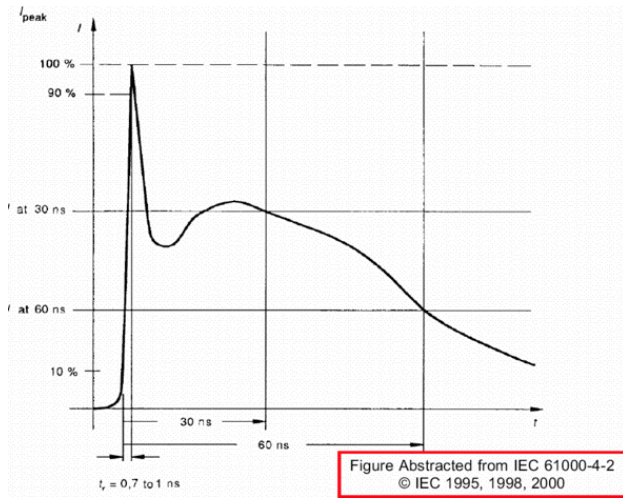


Figure 8. $I_{peak} = f(t)$ / IEC61000-4-2

USB OTG Support

When used in an application that has to supply voltage to an external accessory (i.e. USB OTG), the part is able to supply 1.8 A to the accessory. If $V_{IN} = 0$ V when +5.0 V OTG is applied to the OUT pin, current will flow through the MOSFET body diode and, as soon as the output voltage will be higher than the V_{UVLO} voltage (2.8 V) plus Body diode forward voltage, the part will turn fully ON and current will be supplied to the accessory with minimum drop.

In that case, the \overline{ACOK} pin will keep High-Z state.

ORDERING INFORMATION

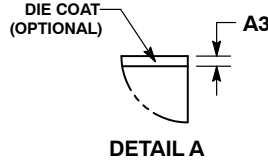
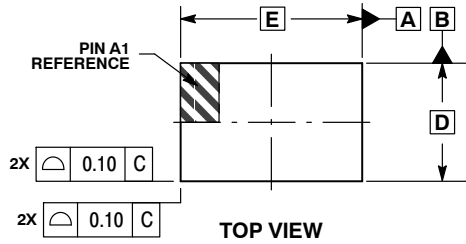
Device	Marking	Option	Package	Shipping [†]
NCP392DRFCCT1G	392DR	OVLO 6.8 V	WLCSP (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NCP392D

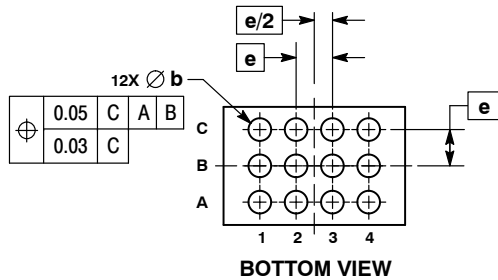
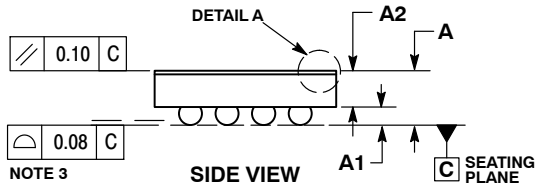
PACKAGE DIMENSIONS

WLCSP12, 1.3x2.0 CASE 567JM ISSUE A

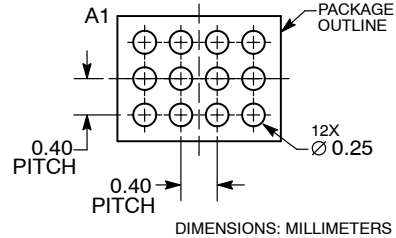


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.


DIM	MILLIMETERS	
	MIN	MAX
A	---	0.60
A1	0.17	0.23
A2	0.36 REF	
A3	0.04 REF	
b	0.24	0.30
D	1.26	1.31
E	2.01	2.04
e	0.40 BSC	



RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and the  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marketing.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative