

LC89091JAGEVK



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LC89091JA Digital Audio Interface Receiver Test Procedure

This document explains various evaluations of digital audio interface receiver LC89091JA.

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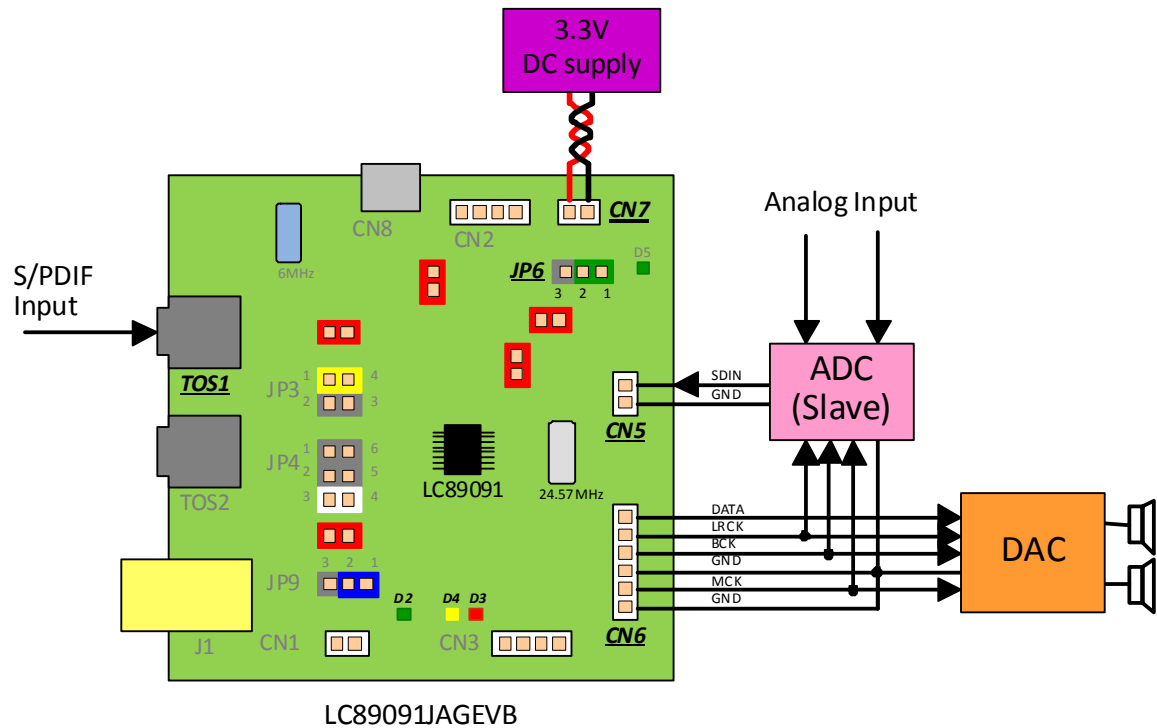
Modification History

Ver	Date	Description
0.00	2013.04.02	First edition

LC89091JAGEVK Test Procedure

1. Function Check (PC doesn't use)

- Basic operation of LC89091JA can be checked.



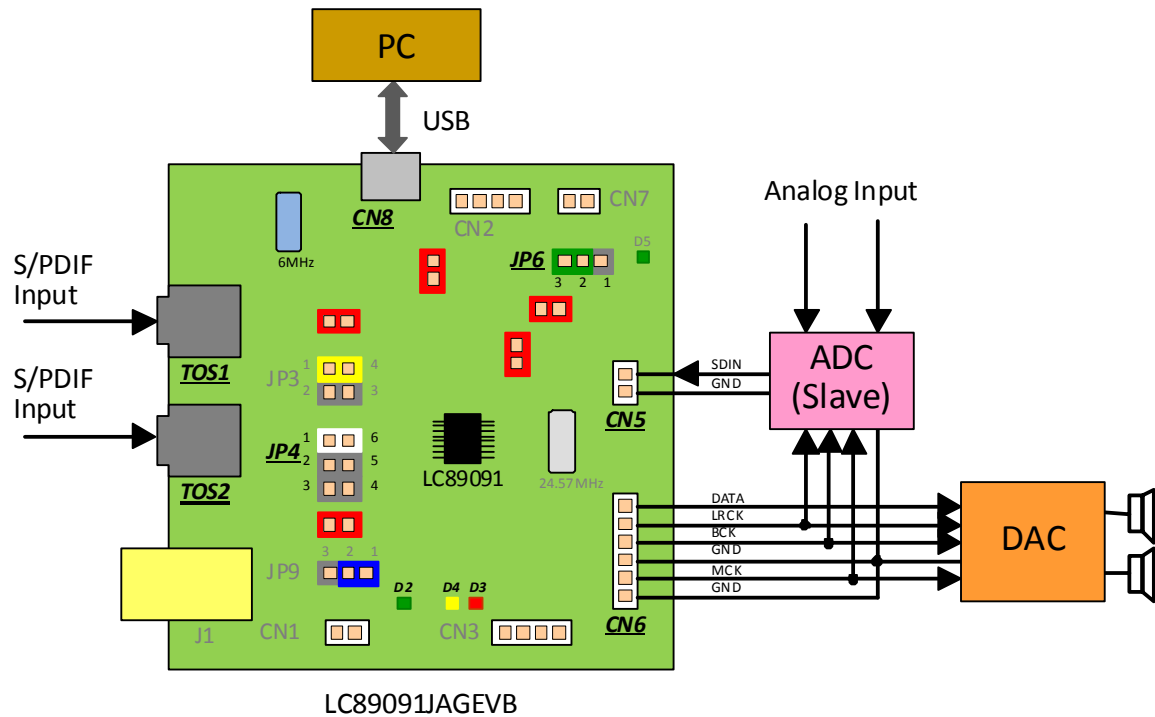
Power supply	USB	External DC	DSP connection	YES	NO
Register control	YES	NO	PLL error monitor	LED (D3)	PC
S/PDIF input	TOSLINK	COAXIAL	Non-PCM monitor	LED (D4)	PC
ADC connection	YES	NO	Emphasis monitor	LED (D2)	PC
DAC connection	YES	NO	Demodulation data	Oscilloscope	Audio output

S/PDIF		Emphasis input	LED indication			DAC output
Linear-PCM	Non-PCM		D2 Emphasis	D3 PLL error	D4 Non-PCM	
×	×	×	Off	Turn on	Off	ADC data
Input	×	No	Off	Off	Off	Demodulation data
Input	×	Yes	Turn on	Off	Off	Demodulation data
×	Input	×	Off	Off	Turn on	Demodulation data

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2. Function Check (PC uses)

- PC can be connected by USB and operation of LC89091JA can be checked by I2C control.



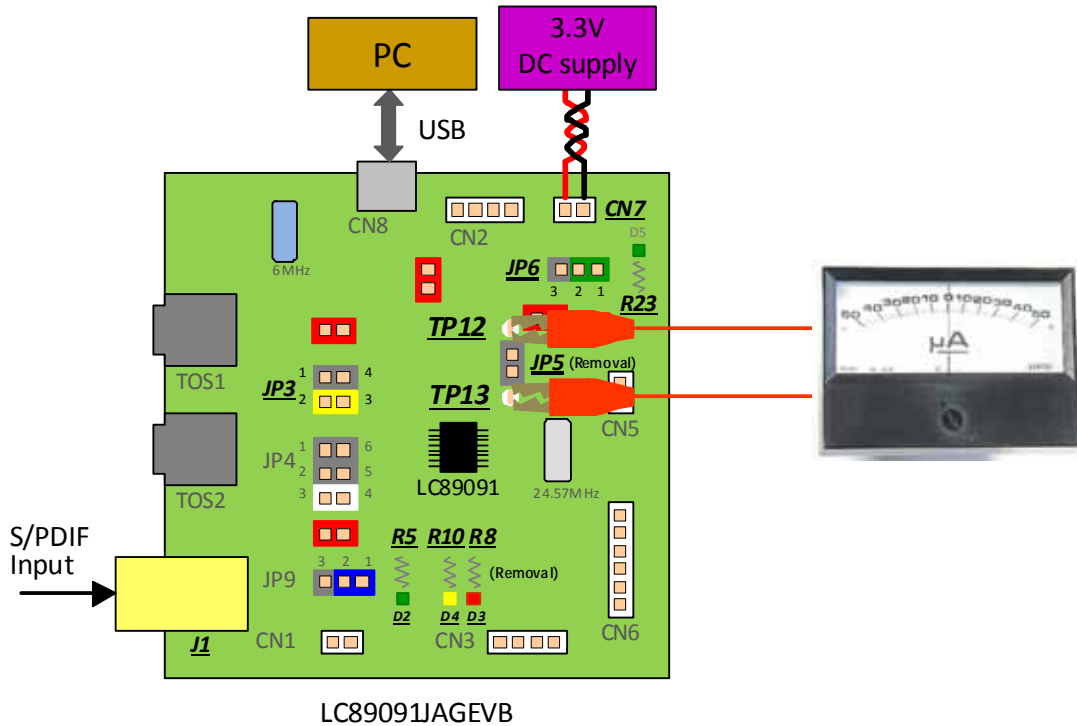
Power supply	USB	External DC	DSP connection	YES	NO
Register control	YES	NO	PLL error monitor	LED (D3)	PC
S/PDIF input	TOSLINK	COAXIAL	Non-PCM monitor	LED (D4)	PC
ADC connection	YES	NO	Emphasis monitor	LED (D2)	PC
DAC connection	YES	NO	Demodulation data	Oscilloscope	Audio output

Setting Item	R/W	Adr	D7	D6	D5	D4	D3	D2	D1	D0
System	R/W	00h	"0"	MPSEL	DATWT	ERRWT	ADMODE	AMPOPR	PDMODE	SYSRST
Clock	R/W	01h	"0"	"0"	XOUTCK	PRSEL1	PRSEL0	PLLDIV1	PLLDIV0	PLLACC
Data	R/W	02h	NPMODE	ERRSEL	GPOSEL1	GPOSEL0	DATMUT	THRSEL	DINSEL	DAFORM
Fs	R	03h	0	0	0	ERRFLG	FSC3	FSC2	FSC1	FSC0
Channel status	R	04h	CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0
	R	05h	CS15	CS14	CS13	CS12	CS11	CS10	CS9	CS8
	R	06h	CS23	CS22	CS21	CS20	CS19	CS18	CS17	CS16
	R	07h	CS31	CS30	CS29	CS28	CS27	CS26	CS25	CS24
	R	08h	CS39	CS38	CS37	CS36	CS35	CS34	CS33	CS32

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3. Consumption Current Measurement

- The consumption current of LC89091JA can be measured.
- JP5 socket remove and a current measurement machine insert in TP12 and TP13.
- Current limiting resistor (R5, R8, R10, R23) of LED remove.
- The current of various states can be measured by register control. (Current at the time of power down, etc.)



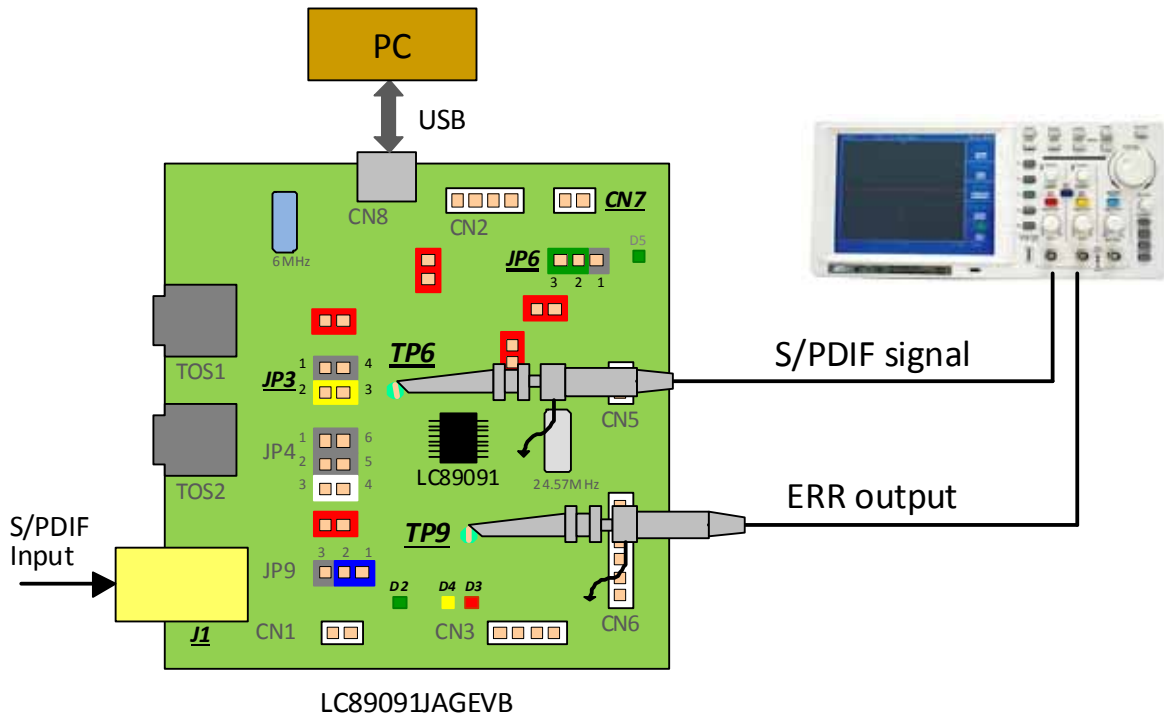
Power supply	USB	External DC	DSP connection	YES	NO
Register control	YES	NO	PLL error monitor	LED (D3)	PC
S/PDIF input	TOSLINK	COAXIAL	Non-PCM monitor	LED (D4)	PC
ADC connection	YES	NO	Emphasis monitor	LED (D2)	PC
DAC connection	YES	NO	Demodulation data	Oscilloscope	Audio output

Setting Item	R/W	Adr	D7	D6	D5	D4	D3	D2	D1	D0
System	R/W	00h	"0"	MPSEL	DATWT	ERRWT	ADMODE	AMPOPR	PDMODE	SYSRST
Clock	R/W	01h	"0"	"0"	XOUTCK	PRSEL1	PRSEL0	PLLDIV1	PLLDIV0	PLLACC
Data	R/W	02h	NPMODE	ERRSEL	GPOSEL1	GPOSEL0	DATMUT	THRSEL	DINSEL	DAFORM
Fs	R	03h	0	0	0	ERRFLG	FSC3	FSC2	FSC1	FSC0
Channel status	R	04h	CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0
	R	05h	CS15	CS14	CS13	CS12	CS11	CS10	CS9	CS8
	R	06h	CS23	CS22	CS21	CS20	CS19	CS18	CS17	CS16
	R	07h	CS31	CS30	CS29	CS28	CS27	CS26	CS25	CS24
	R	08h	CS39	CS38	CS37	CS36	CS35	CS34	CS33	CS32

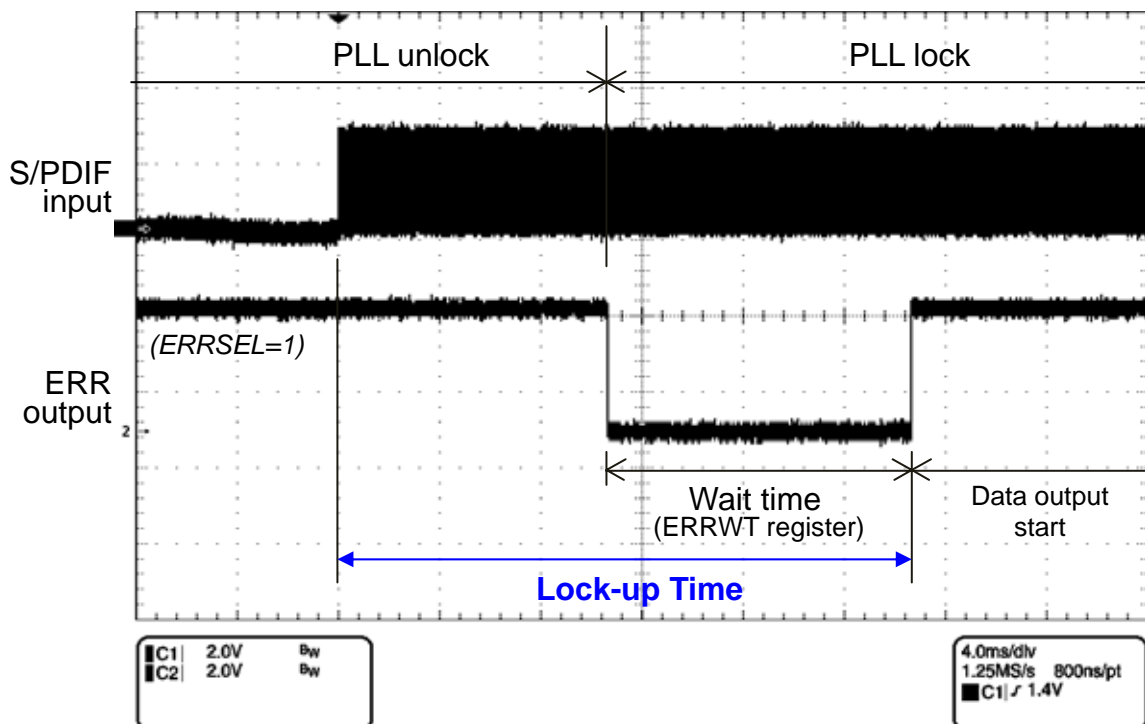
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4. Lock-up Time Measurement

- Time until an error flag is canceled is measured after S/PDIF input.
- It is set as register ERRSEL (address 02h, D6) =1.



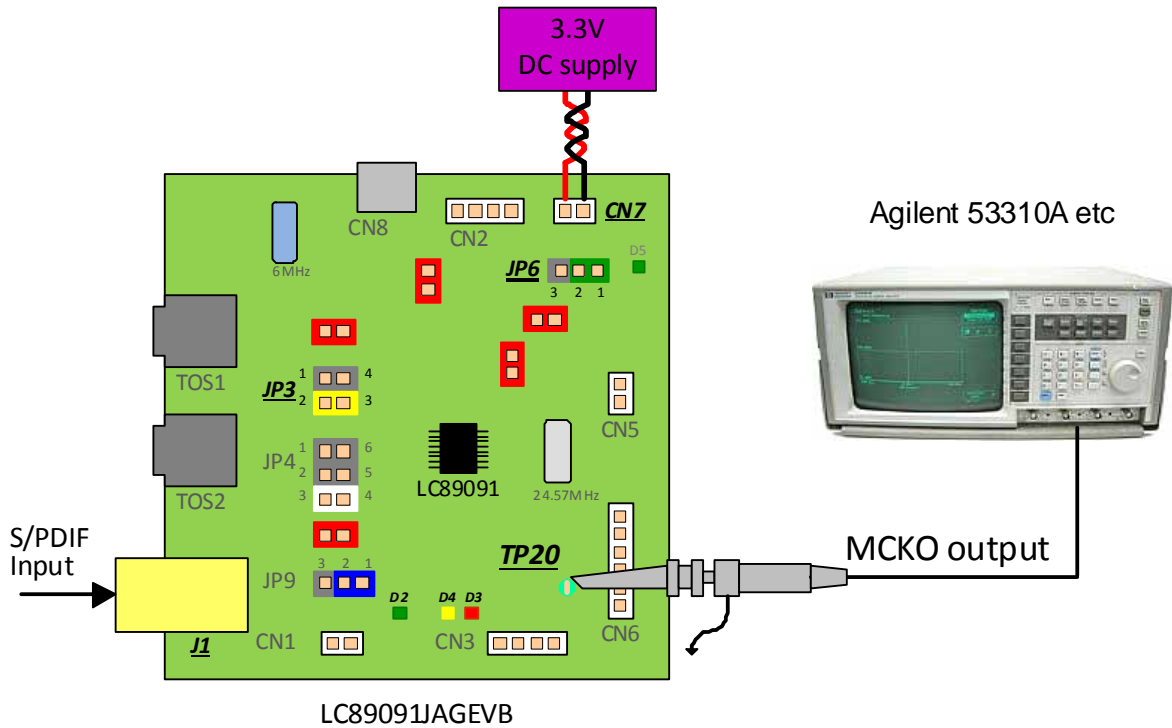
Power supply	USB	External DC	DSP connection	YES	NO
Register control	YES	NO	PLL error monitor	LED (D3)	PC
S/PDIF input	TOSLINK	COAXIAL	Non-PCM monitor	LED (D4)	PC
ADC connection	YES	NO	Emphasis monitor	LED (D2)	PC
DAC connection	YES	NO	Demodulation data	Oscilloscope	Audio output



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5. PLL Clock Jitter Measurement

- The clock jitter of master clock MCKO is measured with a dedicated device.
- S/PDIF's input recommends a coaxial with little influence of reflection.

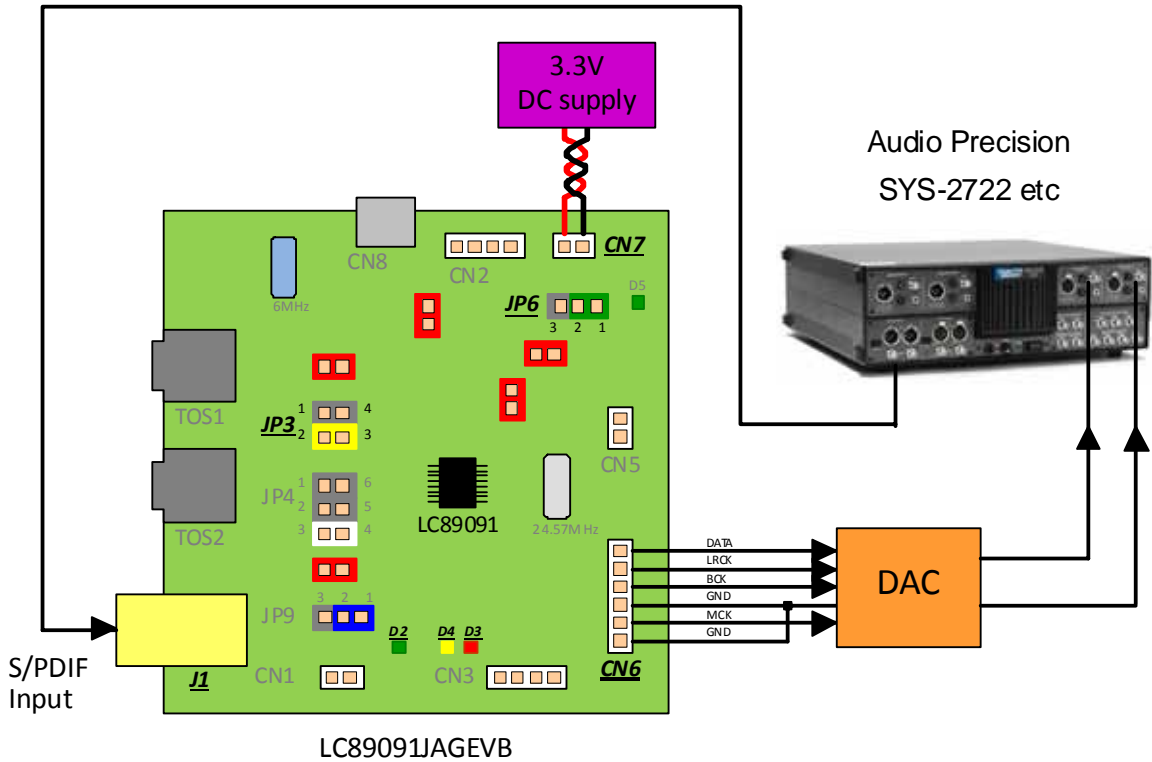


Power supply	USB	External DC	DSP connection	YES	NO
Register control	YES	NO	PLL error monitor	LED (D3)	PC
S/PDIF input	TOSLINK	COAXIAL	Non-PCM monitor	LED (D4)	PC
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DAC connection	YES	NO	Demodulation data	Oscilloscope	Audio output

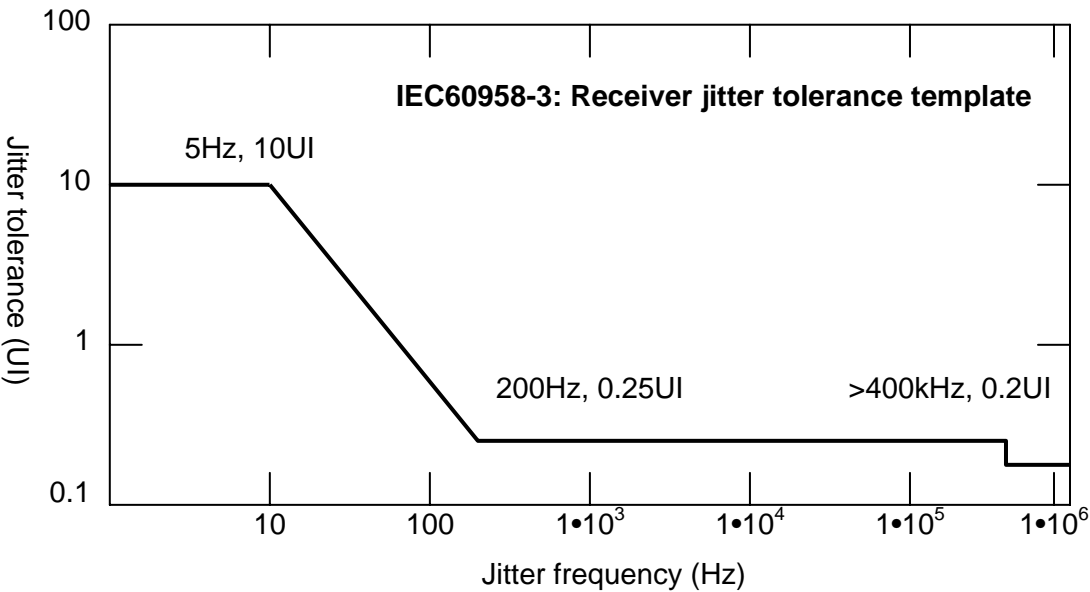
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6. S/PDIF Input Jitter Tolerance Measurement

- S/PDIF including jitter inputs to LC89091 and checks whether data is correctly receivable.
- The frequency and amplitude of impressing jitter are based on IEC60958-3.
- Please refer to the equipment manual for a measuring method.

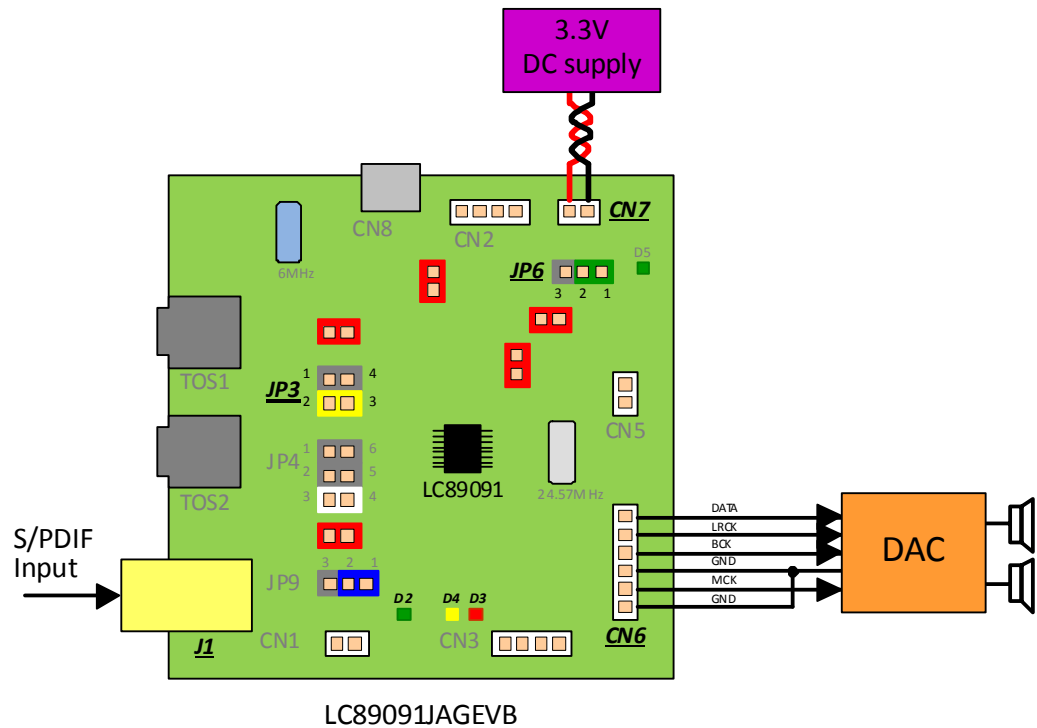


Power supply	USB	External DC	DSP connection	YES	NO
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S/PDIF input	TOSLINK	COAXIAL	Non-PCM monitor	LED (D4)	PC
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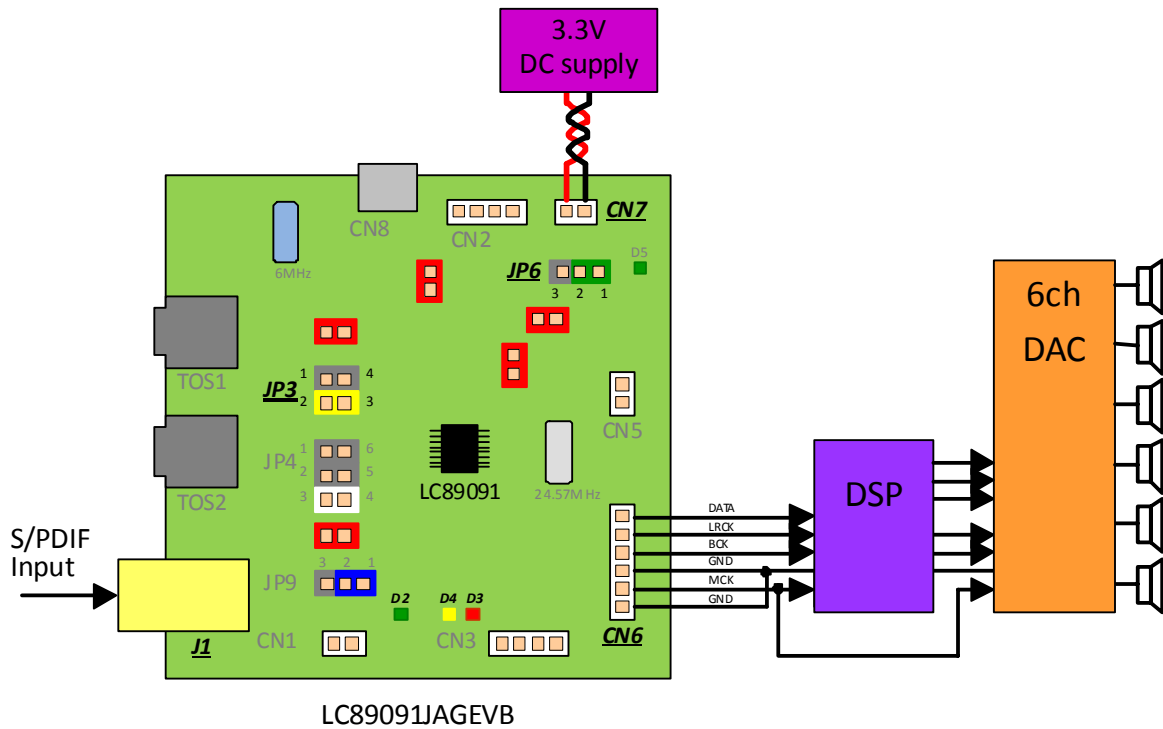
7. Example of Sound Quality Evaluation Circuit Configuration (2 channel stereo audio)



Power supply	USB	External DC	DSP connection	YES	NO
Register control	YES	NO	PLL error monitor	LED (D3)	PC
S/PDIF input	TOSLINK	COAXIAL	Non-PCM monitor	LED (D4)	PC
ADC connection	YES	NO	Emphasis monitor	LED (D2)	PC
DAC connection	YES	NO	Demodulation data	Oscilloscope	Audio output

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8. Example of Sound Quality Evaluation Circuit Configuration (5.1 channel multi-channel audio)



Power supply	USB	External DC	DSP connection	YES	NO
Register control	YES	NO	PLL error monitor	LED (D3)	PC
S/PDIF input	TOSLINK	COAXIAL	Non-PCM monitor	LED (D4)	PC
ADC connection	YES	NO	Emphasis monitor	LED (D2)	PC
DAC connection	YES	NO	Demodulation data	Oscilloscope	Audio output

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