STK5Q4U3xxJ series

Application Note

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1. Product synopsis

This application handbook is intended to provide practical guidelines for the **STK5Q4U3xxJ series** use.

The **STK5Q4U3xxJ series** is Intelligent Power Module (IPM) for 3-phase motor drives which contain the main power circuitry and the supporting control circuitry. The key functions are outlined below:

- Highly integrated device containing all High Voltage (HV) control from HV-DC to 3-phase outputs in a single small DIP module.
- Output stage uses IGBT/FRD technology and implements Under Voltage Protection (UVP) and Over Current Protection (OCP) with a Fault Detection output flag. Internal Boost diodes are provided for high side gate boost drive.
- Option of a combined or individual shunt resistor per phase for OCP.
- Externally accessible embedded thermistor for substrate temperature measurement.
- All control inputs and status outputs are at low voltage levels directly compatible with microcontrollers.
- Single control power supply due to internal bootstrap circuit for high side pre-driver circuit.
- Mounting points are available on DIP package.

A simplified block diagram of a motor control system is shown in Figure 1.

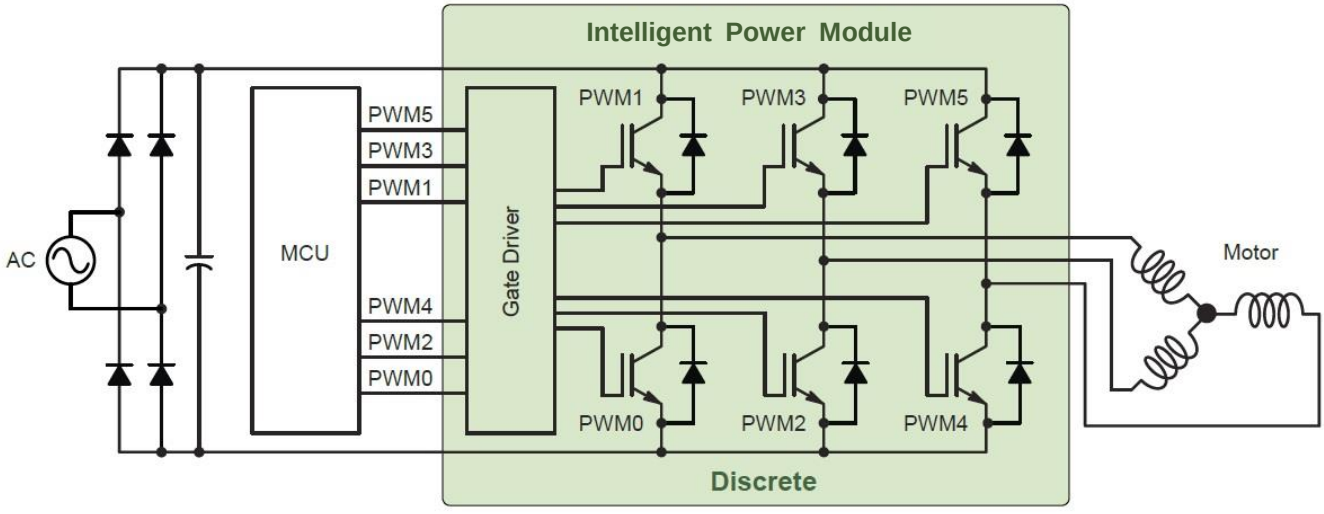


Figure 1. Motor Control System Block Diagram

2. Product description

Table1. gives an overview of the available devices. For a detailed description of the packages, please refer to Chapter 6.

Device	STK5Q4U340J-E *	STK5Q4U352J-E	STK5Q4U362J-E STK5Q4U363J-E *	STK5Q4U390J-E * STK5Q4U393J-E *
Feature	triple shunts			
Package	DIPS3			
Voltage (VCEmax.)	600V			
Current (Ic)	5A	8A	10A	15A
Peak current (Ic)	10A	16A	20A	30A
Isolation voltage	2000V			
Shunt resistance	external			

* Under development

Table 1. Device Overview

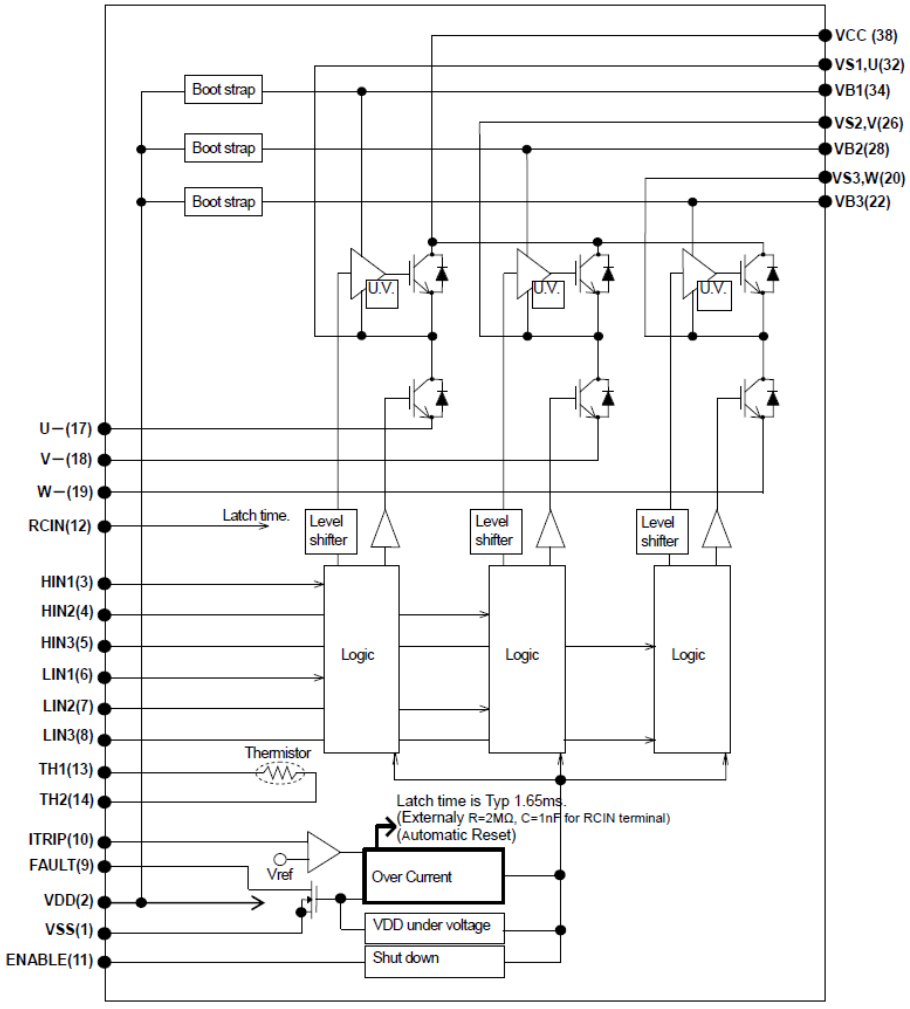


Figure 2. STK5Q4U3xxJ series equivalent circuits

The high side drive is used with a bootstrap circuit to generate the higher voltage needed for gate drive. The Boost diodes are internal to the part and sourced from VDD (15V). There is an internal level shift circuit for the high side drive signals allowing all control signals to be driven directly from Vss levels common with the control circuit such as the microcontroller without requiring external level shift such as opto isolators.

3. Performance test guidelines

The following Chapter gives performance test method shown in Figures 3 to 7.

3.1. Switching time definition and performance test method

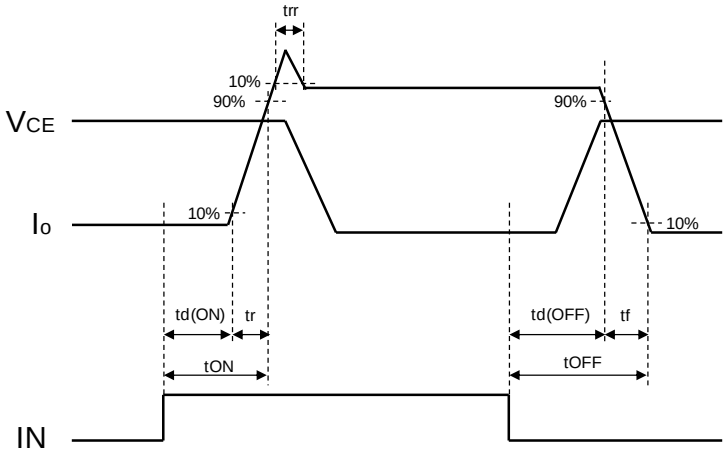


Figure 3. Switching time definition

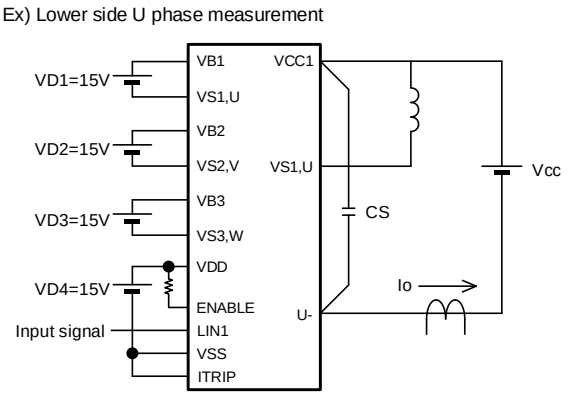


Figure 4. Evaluation circuit (Inductive load)

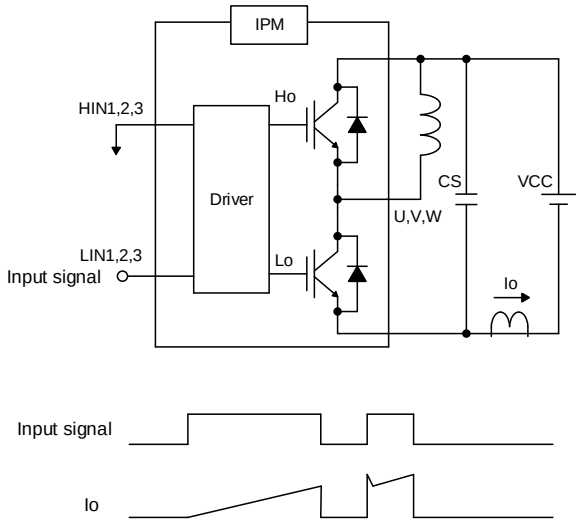


Figure 5. Switching loss circuit

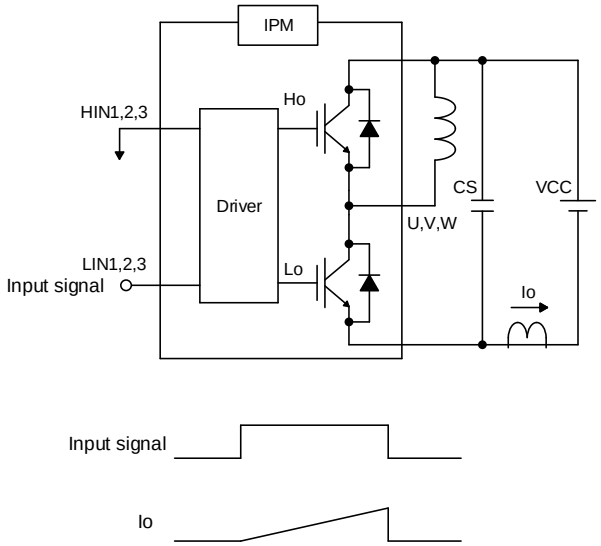


Figure 6. R.B.SOA circuit

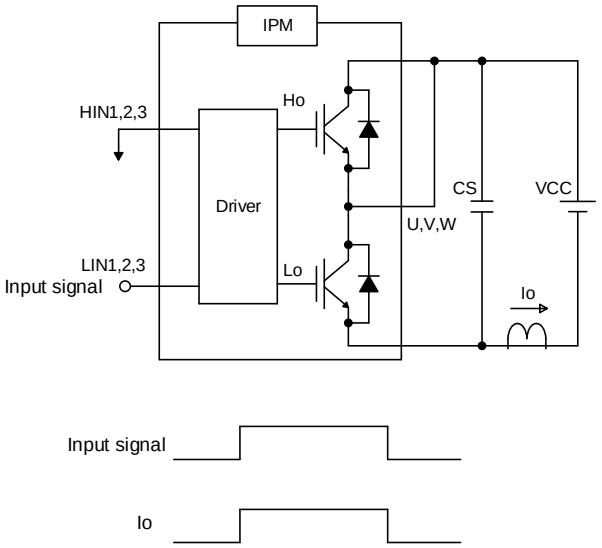


Figure 7. S.C.SOA circuit

3.2. Thermistor Characteristics

The thermistor is built-in between TH1 pin and TH2 pin. This is used to sense the temperature of the internal module. Its characteristic is outlined below.

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Resistance	R_{25}	Tc=25℃	99	100	101	kΩ
Resistance	R_{100}	Tc=100℃	5.18	5.38	5.60	kΩ
B-Constant(25-50℃)	B		4208	4250	4293	K
Temperature Range			-40		+125	℃

Table 2. NTC Thermistor value

R_{25} is the value of the built-in NTC thermistor at Tc=25℃. The resistance value is 100kΩ±1% and the value of the B-Constant (25-50℃) is 4250K±1%. The resistance value R(t) depended on the temperature is calculated by the following formula.

$$\mathbf{R(t) = R_{25} \times e^{B\left(\frac{1}{T}-\frac{1}{298}\right)}}$$

* The constant T is the absolute temperature value.

The result in the NTC values over temperatures

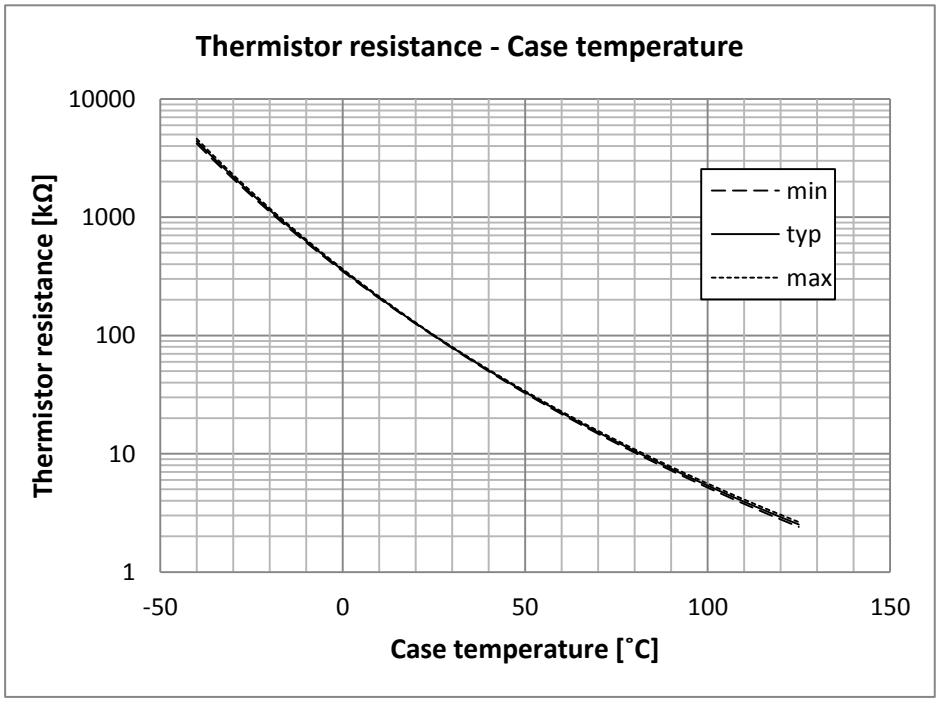


Figure 8. typical NTC value over temperature

4. Protective functions and Operation Sequence

This chapter describes the protection features.

- over current protection
- short circuit protection
- under Voltage Lockout (UVLO) protection
- cross conduction prevention

4.1. Over current protection

In difference to the internal single shunt series modules, the STK5Q4U3xxJ series module utilizes an external shunt resistor for the OCP functionality. As shown in Figure 9, the emitters of all three lower side IGBTs brought out to module pins. An external "over current protection circuitry" consisting of the shunt resistor and an RC filter network defines the trip level.

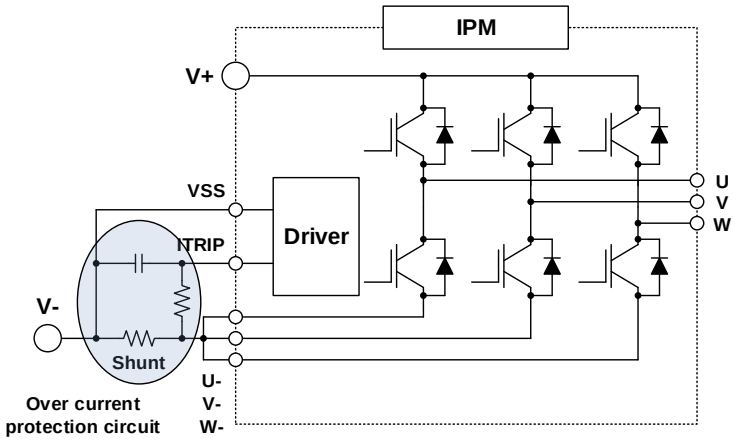


Figure 9. Over-current protection circuit setting

The OCP function is implemented by comparing the voltage on the Itrip input to an internal reference of 0.49V (typ). In case the voltage on this terminal i.e. across the shunt resistor exceeds the trip level an OCP fault is triggered.

Note: The current value of the OCP needs to be set by correctly sizing the external shunt resistor to less than 2x of the modules rated current.

In case of an OCP event all internal gate drive signal for the IGBTs of all three phases become inactive and the FLT/EN fault signal output is activated (low).

An RC filter is used on the Itrip input to prevent an erroneous OCP detection due to normal switching noise and/or recovery diode current. The time constant of that RC filter should be set to a value between 1.5µ to 2µs. In any case the time constant must be shorter than the IGBTs short current safe operating area (SCSOA). Please refer to Data Sheet for SCSOA. The resulting OCP level due to the filter time constant is shown in Figure 10.

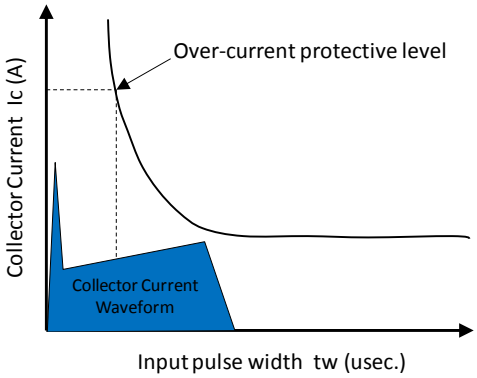


Figure 10. filter time constant

For optimal performance all traces around the shunt resistor need to be kept as short as possible.

Figure 11. shows the sequence of events in case of an OCP event.

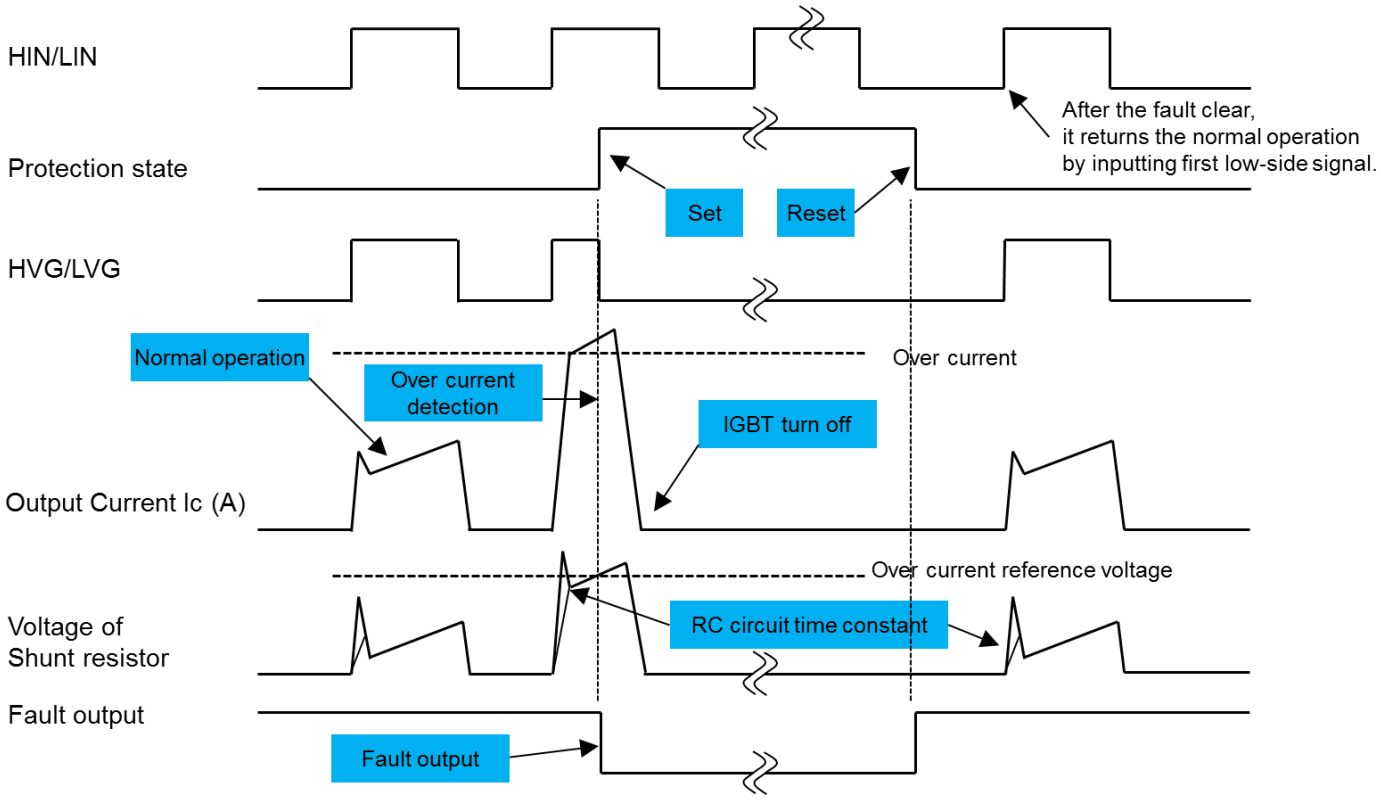


Figure 11. Over current protection Timing chart

4.2. Under Voltage Lockout Protection

The UVLO protection is designed to prevent unexpected operating behavior as described in Table 3. Both High-side and Low-side have UV protecting function. However the fault signal output only corresponds to the Low-side UVLO Protection. During the UVLO state the fault output is continuously driven (low).

VDD Voltage (typ. Value)	Operation behavior
< 12.5V	As the voltage is lower than the UVLO threshold the control circuit is not fully turned on. A perfect functionality cannot be guaranteed.
12.5 V – 13.5 V	IGBTs can work, however conduction and switching losses increase due to low voltage gate signal.
13.5 V – 16.5 V	Recommended conditions
16.5 V – 20.0 V	IGBTs can work. Switching speed is faster and saturation current higher, increasing short-circuit broken risk.
> 20.0 V	Control circuit is destroyed. Absolute max. rating is 20 V.

Table 3. *Module operation according to control supply voltage*

The sequence of events in case of a low side UVLO event (IGBTs turned off and active fault output) is shown in Figure 12. Figure 13 shows the same for a high side UVLO (IGBTs turned off and no fault output).

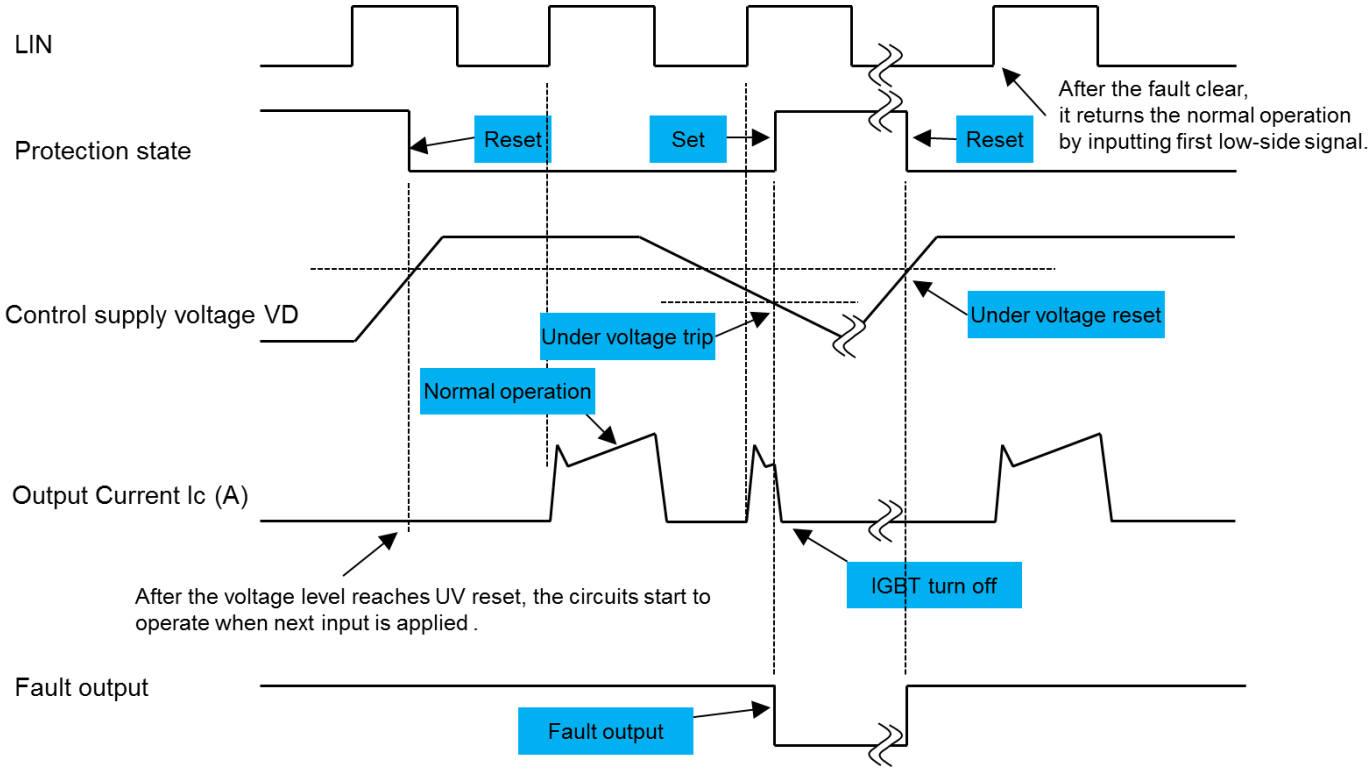


Figure 12. Low side UVLO timing chart

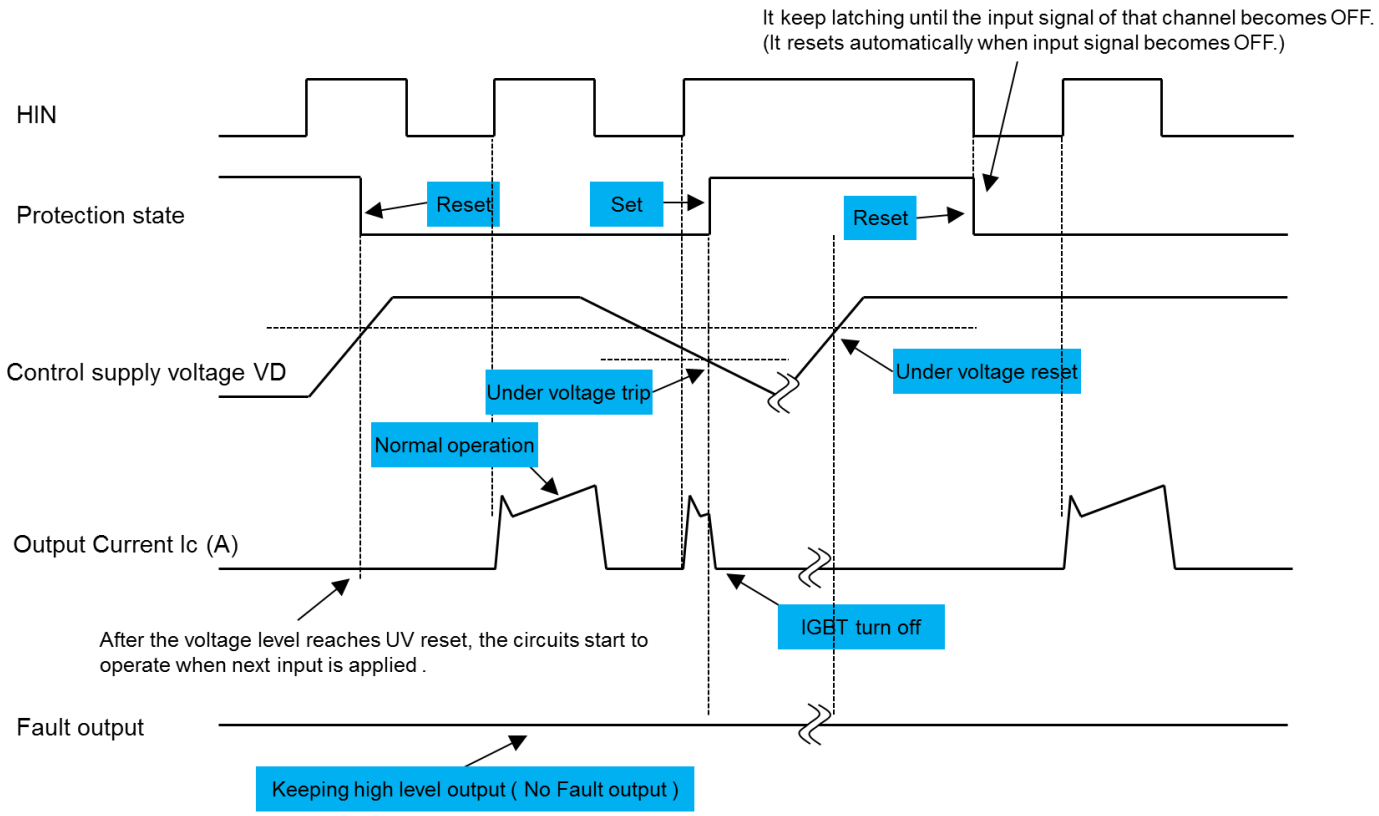


Figure 13. High side UVLO timing chart

4.3. Cross conduction prevention

The STK5Q4U3xxJ series module implement a cross conduction prevention logic at the pre-driver to avoid simultaneous drive of the low- and high-side IGBTs as shown in Figure 14.

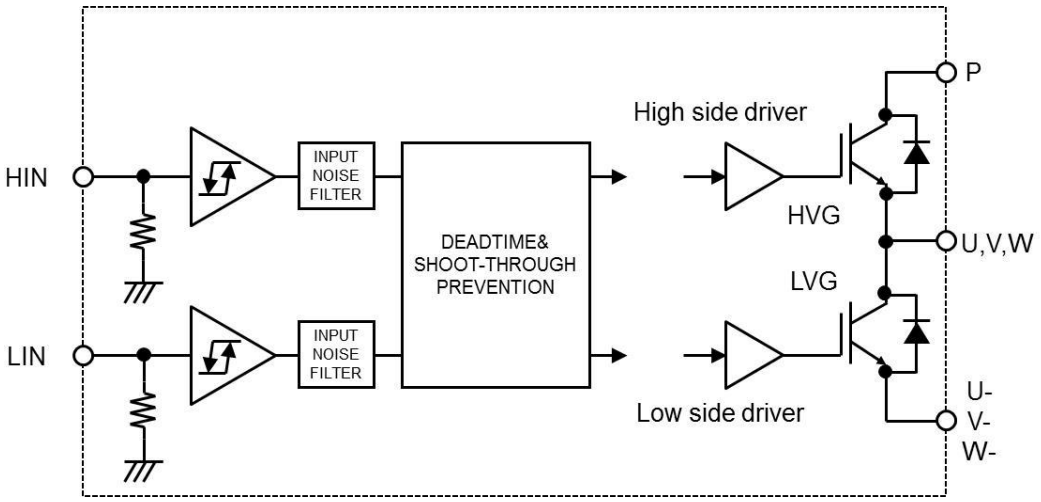


Figure 14. Cross Input Conduction Prevention

In case of both high and low side drive inputs are active (high) the logic prevents both gates from being driven – a corresponding timing diagram can be found in Figure 15 below.

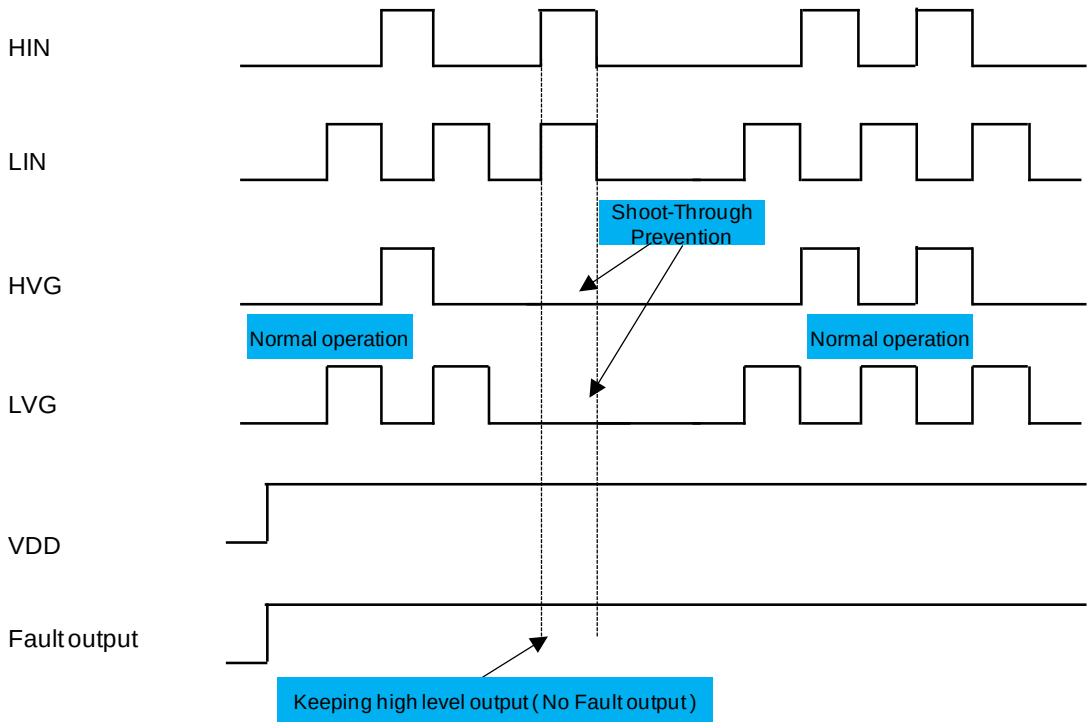


Figure 15. cross conduction prevention timing diagram

Even so cross conduction on the IGBTs due to incorrect external driving signals is prevented by the circuitry the driving signals (HIN and LIN) need to include a “dead time”. This period where both inputs are inactive between either one becoming active is required due to the internal delays within the IGBTs.

Figure 16 shows the delay from the HIN-input via the internal HVG to high side IGBT, the similar path for the low side and the resulting minimum dead time which is equal to the potential shoot through period:

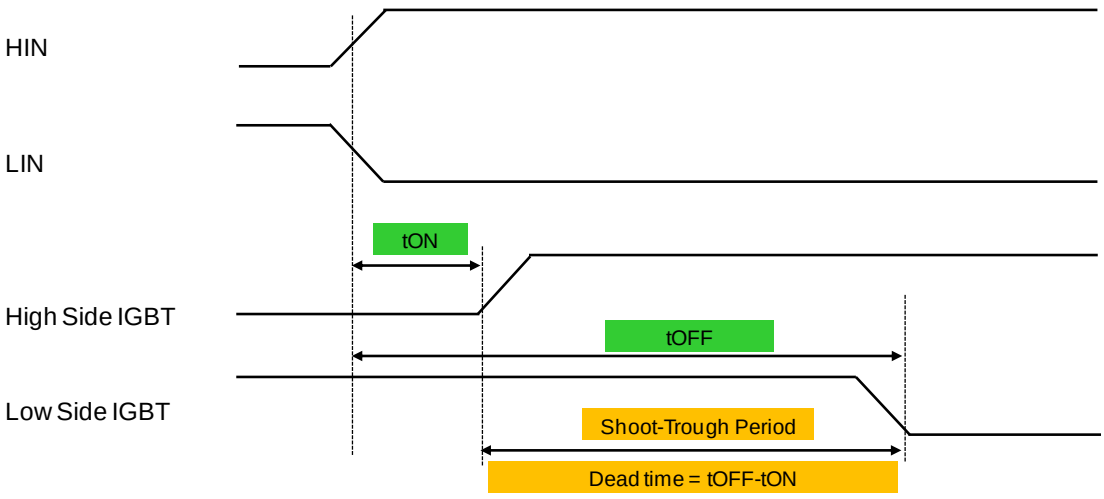


Figure 16. Shoot Trough Period

5. PCB design and mounting guidelines

This chapter provides guidelines for an optimized design and PCB layout as well as module mounting recommendations to appropriately handle and assemble the IPM.

5.1. Application (schematic) design

The following figure 17 gives an overview of the external circuitry's functionality when designing with the STK5Q4U3xxJ series module.

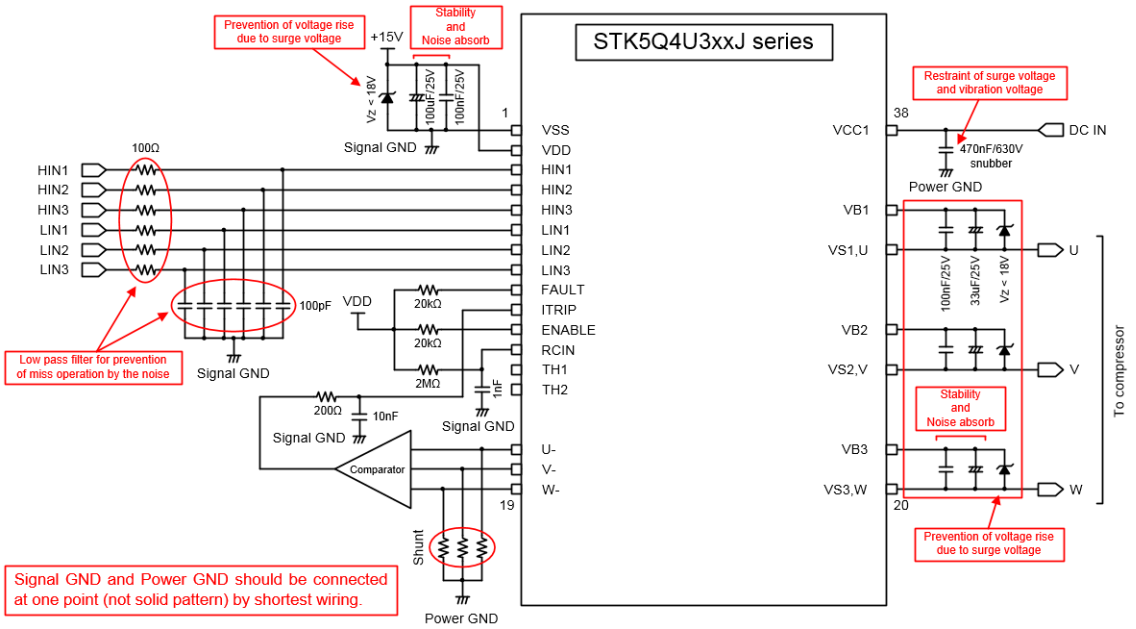


Figure 17. STK5Q4U3xxJ series application circuit

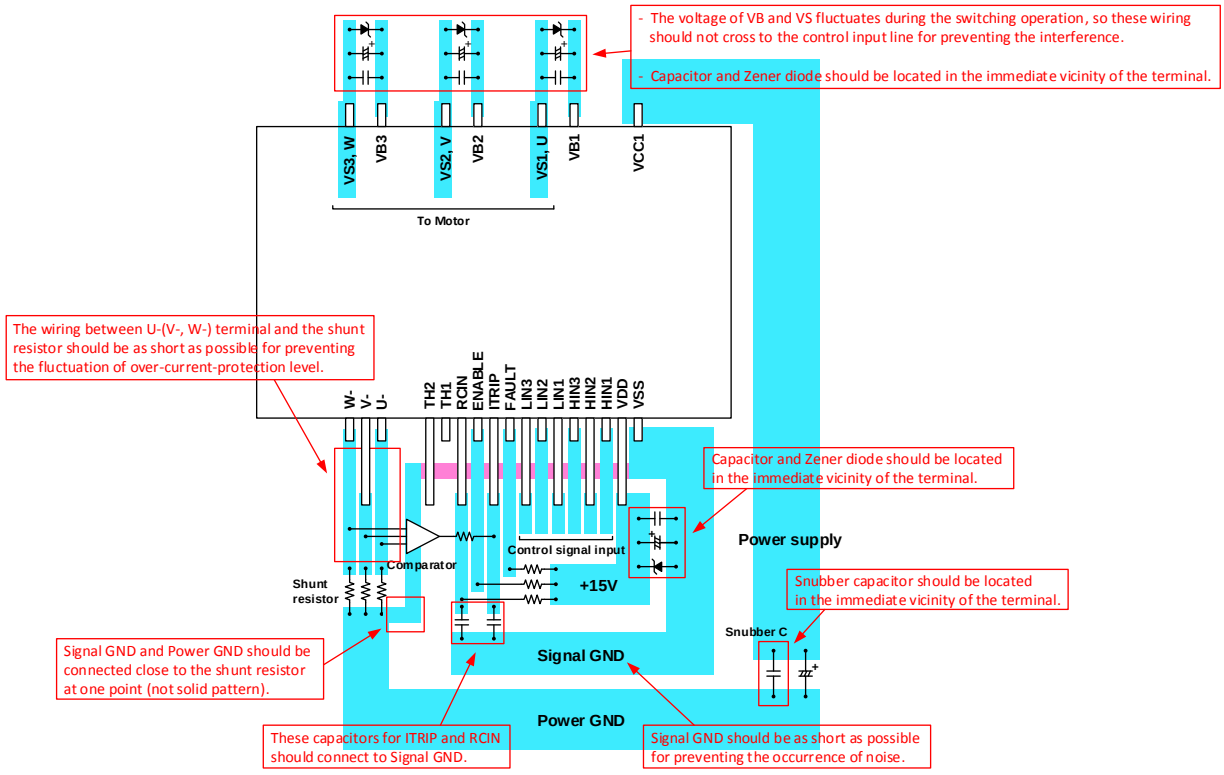


Figure 18. PCB design reference

5.2. Pin by pin design and usage notes

This section provides pin by pin PCB layout recommendations and usage notes. For a complete list of module pins refer to the datasheet or Chapter 6.

VCC1
U-, V-, W-

These pins are connected with the main DC power supply. The applied voltage is up to the Vcc level. Overvoltage on these pins could be generated by voltage spikes during switching at the floating inductance of the wiring. To avoid this behavior the wire traces need to be as short as possible to reduce the floating inductance. In addition a snubber capacitor needs to be placed as close as possible to these pins to stabilize the voltage and absorb voltage surges.

U, V, W

These terminals are the output pins for connecting the 3-phase motor. They share the same GND potential with each of the high side control power supplies. Therefore they are also used to connect the GND of the bootstrap capacitors. These bootstrap capacitors should be placed as close to the module as possible.

VDD, VSS

These pins connect with the circuitry of the internal protection and pre-drivers for the low -side power elements and also with the control power supply of the logic circuitry. Voltage to input these terminals is monitored by the under voltage protection circuit. The VSS terminal is the reference voltage for the control inputs signals.

VB1, VB2
VB3

The VBx pins are internally connected to the positive supply of the high-side drivers. The supply needs to be floating and electrically isolated. The boot-strap circuit shown in Figure 19 forms this power supply individually for every phase. Due to integrated boot FET only an external boot capacitor (CB) is required.

CB is charged when the following two conditions are met.

① Low-side signal is input

② Motor terminal voltage is low level

The capacitor is discharged while the high-side driver is activated.

Thus CB needs to be selected taking the maximum on time of the high side and the switching frequency into account.

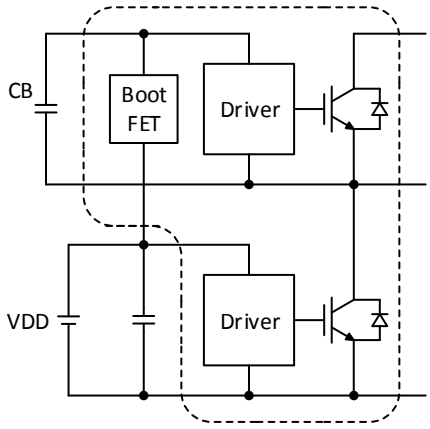


Figure 19. Boot Strap Circuit

The voltages on the high side drivers are individually monitored by the under voltage protection circuit. In case an UVP event is detected on a phase its operation is stopped.

Typically a CB value of less or equal 47uF (±20%) is used. In case the CB value needs to be higher, an external resistor (of apx. 20Ω or less) should be used in series with the capacitor to avoid high currents which can cause malfunction of the IPM.

HIN1, LIN1
HIN2, LIN2
HIN3, LIN3

These pins are the control inputs for the power stages. The inputs on HIN1/HIN2/HIN3 control the high-side transistors of U/V/W, the inputs on LIN1/LIN2/LIN3 control the low-side transistors of U/V/W respectively. The input are active high and the input thresholds VIH and VIL are 5V compatible to allow direct control with a microcontroller system.
Simultaneous activation of both low and high side is prevented internally to avoid shoot through at the power stage. However, due to IGBT switching delays the control signals must include a dead-time.

The equivalent input stage circuit is shown in Figure 20.

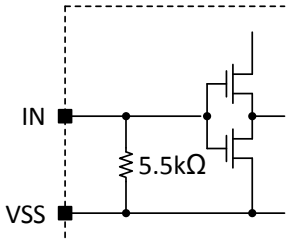


Figure 20. Internal Input Circuit

The output might not respond when the width of the input pulse is less than 1µs (both ON and OFF).

Note: After impressing VDD, it is necessary to input the low-side signal for starting the operation.

FAULT

The Fault pin is an active low output (open-drain output). It is used to indicate an internal fault condition of the module. The structure is shown in Figure 21.
The sink current of IoSD during an active fault is nominal 2mA @ 0.1V. Depending on the interface supply voltage, the external pull-up resistor (RP) needs to be selected to set the low voltage below the VIL trip level.

For the commonly used supplies VP:
VP = 15V -> RP >= 20kΩ
VP = 5V -> RP>= 6.8kΩ

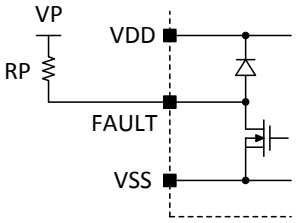


Figure 21. Fault Connection

For a detailed description of the fault operation refer to Chapter 4.

Note: The Fault signal does not permanently continue to latch. After the protection event ended, and the fault clear time(1.65ms) passed, the module's operation is re-started by inputting the low-side signal. Therefore the input needs to be driven low externally activated as soon as a fault is detected.

ITRIP 6 IGBTs are cut off by inputting the voltage exceeding threshold voltage (from 0.44V to 0.54V) to ITRIP pin from outside. The stop-mode is kept while the voltage of this pin exceeds the threshold voltage.

ENABLE Enable pin has shutdown function of the internal pre-driver. The pre-driver operates when the voltage of this pin is at 2.5V or more, and stops at 0.8V or less.
This pin can also be connected to the Fault pin directly.

TH1,TH2 An internal thermistor to sense the substrate temperature is connected between TH1 and TH2. By connecting an external pull-up resistor to either of TH1 and TH2, and shorting the other and VSS, the module temperature can be monitored. Please refer to heading 3.2 for details of the thermistor.

Note: This is the only means to monitor the substrate temperature indirectly.

RCIN This pin is used to set the fault clear time. By connecting the resistor RF versus VDD ,and the capasitor CF versus VSS, the fault clear time can be set. In condition that RF is 2MΩ and CF is 1nF, the fault clear time is 1.65ms.

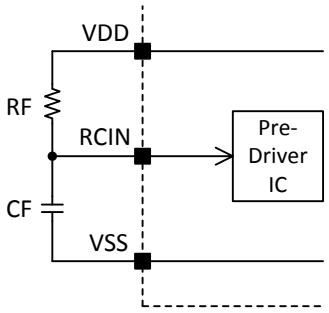


Figure 22. RCIN circuit

To shorten the fault clear time, reduce the value of RF or CF.

5.3. Heat sink mounting and torque

If a heat sink is used, insufficiently secure or inappropriate mounting can lead to a failure of the heat sink to dissipate heat adequately. This can lead to an inability of the device to provide its inherent performance, a serious reduction in reliability, or even destruction, burst and burn of the device due to overheating.

The following general points should be observed when mounting IPM on a heat sink:

1. Verify the following points related to the heat sink:
   - There must be no burrs on aluminum or copper heat sinks.
   - Screw holes must be countersunk.
   - There must be no unevenness in the heat sink surface that contacts IPM.
   - There must be no contamination on the heat sink surface that contacts IPM.

2. Highly thermal conductive silicone grease needs to be applied to the whole back (aluminum substrate side) uniformly, and mount IPM on a heat sink. Upon re-mounting apply silicone grease(50um to 100um) again uniformly.

3. For an intimate contact between the IPM and the heat sink, the mounting screws should be tightened gradually and sequentially while a left/right balance in pressure is maintained. Either a bind head screw or a truss head screw is recommended. Please do not use tapping screw. We recommend using a flat washer in order to prevent slack. The standard heat sink mounting condition of STK5Q4U3xxJ series is as follows.

Item	Recommended Condition
Pitch	26.0±0.1mm (Please refer to Package Outline Diagram)
Screw	diameter : M3 Bind machine screw, Truss machine screw, Pan machine screw
Washer	Plane washer *Don't use spring washer. The size is D:7mm, d:3.2mm and t:0.5mm (Fig.2) JIS B 1256
Heat sink	Material : copper or Aluminum Warpage (the surface that contacts IPM) : -50 ～ 50 µm Screw holes must be countersunk. No contamination on the heat sink surface that contacts IPM.
Torque	Final tightening : 0.4～ 0.6Nm Temporary tightening : 50 ～ 60 % of final tightening
Grease	Silicon grease Thickness : 50 ～ 100 µm Uniformly apply silicon grease to whole back. (Fig.3)

Table 4. heat sink mounting

Fig 1 : mount IPM on a Heat Sink

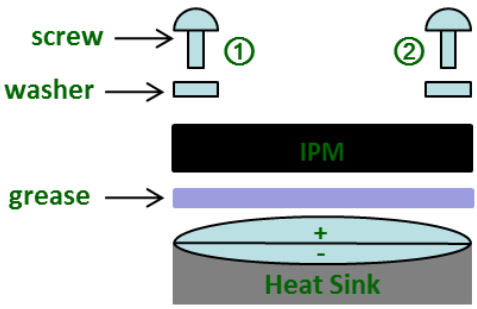


Fig 2 : size of washer

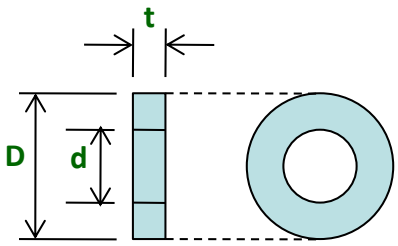
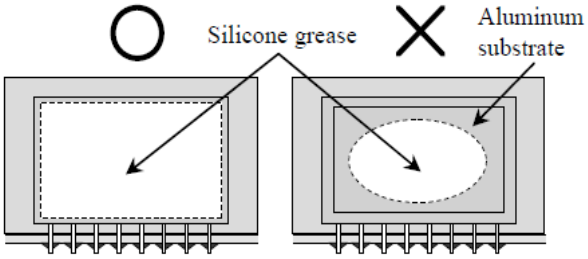


Fig 3 : About uniformly application



Steps to mount an IPM on a heat sink
1st: Temporarily tighten maintaining a left/right balance.
2nd : Finally tighten maintaining a left/right balance.

5.4. Mounting and PCB considerations

In designs in which the printed circuit board and the heat sink are mounted to the chassis independently, use a mechanical design which avoids a gap between IPM and the heat sink, or which avoids stress to the lead frame of IPM by an assembly that a moving IPM is forcibly fixed to the heat sink with a screw.

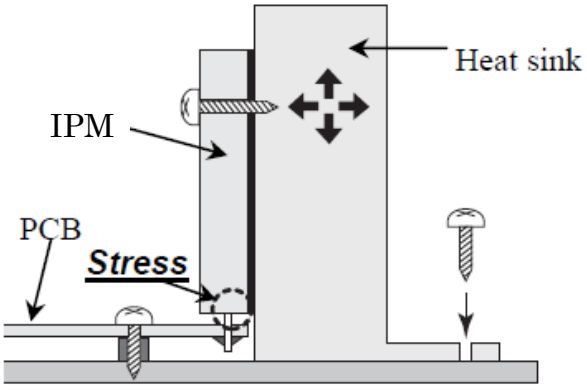
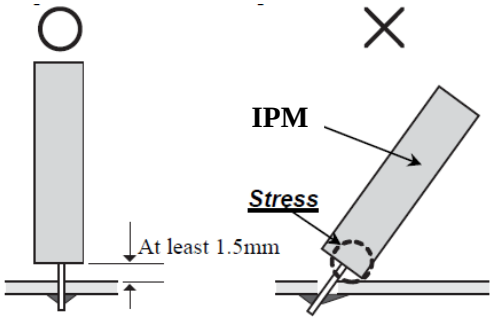


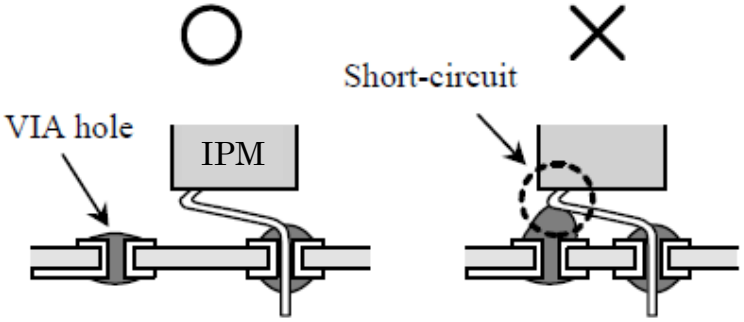
Figure 23. Fix to Heat Sink

Maintain a separation distance of at least 1.5 mm between the IPM case and the printed circuit board. In particular, avoid mounting techniques in which the IPM substrate or case directly contacts the printed circuit board.

Do not mount IPM with a tilted orientation. This can result in stress being applied to the lead frame and IPM substrate could short out tracks on the printed circuit board. Always mount the IPM vertically. If stress is given by compulsory correction of a lead frame after the mounting, a lead frame may drop out. Be careful of this point.



When designing the PCB layout take care that the bent part portion of the lead frame pins does not short-circuit to VIA holes or tracks on the PCB.



Since the use of sockets to mount IPM can result in poor contact with IPM leads, we strongly recommend making direct connections to PCB.
IPMs are flame retardant. However, under certain conditions, it may burn, and poisonous gas may be generated or it may explode. Therefore, the mounting structure of the IPM should also be flame retardant.

Mounting on a Printed Circuit Board

1. Align the lead frame with the holes in the printed circuit board and do not use excessive force when inserting the pins into the printed circuit board. To avoid bending the lead frames, do not try to force pins into the printed circuit board unreasonably.
2. Do not insert IPM into printed circuit board with an incorrect orientation, i.e. be sure to prevent reverse insertion. IPM may be destroyed, exploded, burned or suffer a reduction in their operating lifetime by this mistake.
3. Do not bend the lead frame.

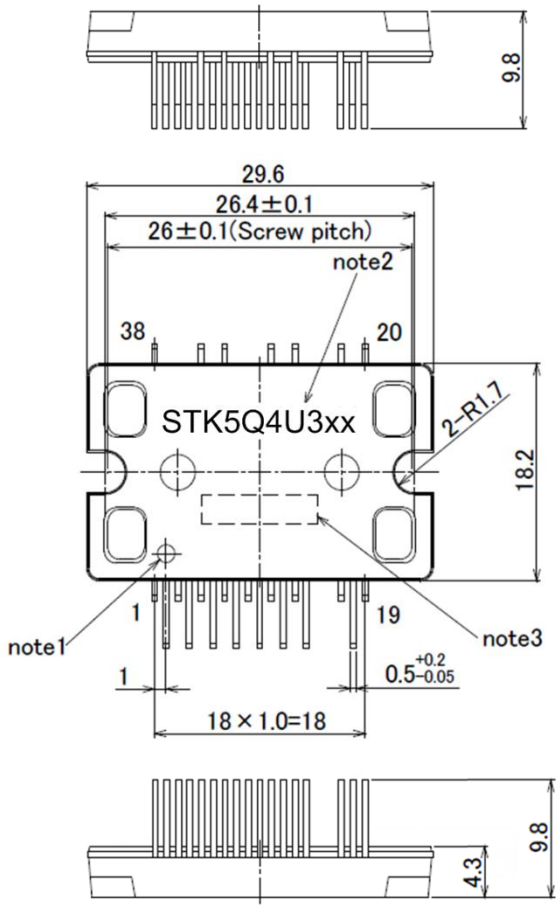
5.5. Cleaning

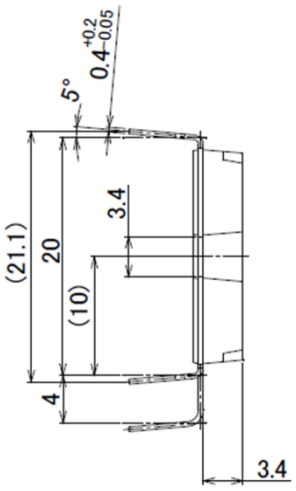
IPM has a structure that is unable to withstand cleaning. As a basic policy, do not clean independent IPM or printed circuit boards on which an IPM is mounted.

6. Package Outline

The package of STK5Q4U3xxJ series is DIPS3 (Dual-inline-package) shown in Figure 24.

6.1. Package outline and dimension





Unit: mm

missing pin: 15,16,21,23,24,25,27
29,30,31,33,35,36,37

note1: No.1 pin identification mark
note2: Model number
note3: Lot code

* The form of a character in this drawing differs from that of IPM.

Figure 24. Package Outline

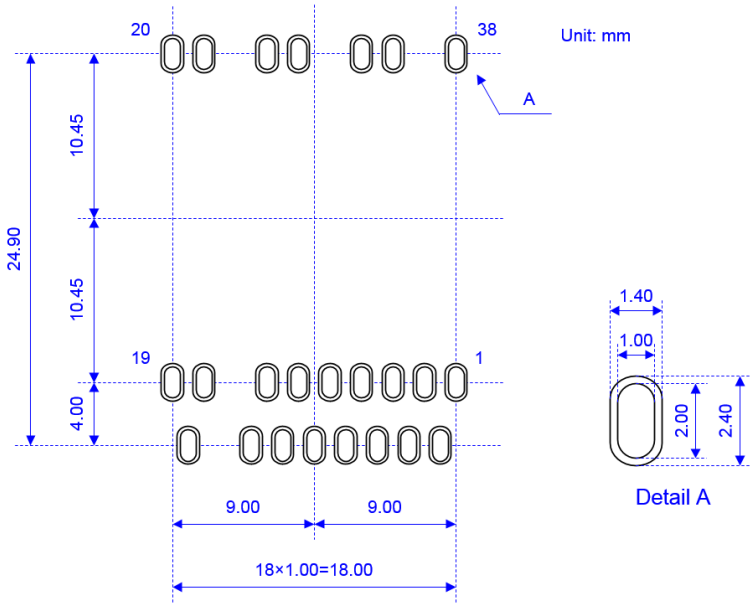


Figure 25. Recommended Land Pattern

6.2. Pin Out Description

Pin	Name	Description
1	VSS	Negative Main Power Supply
2	VDD	+15V Main Power Supply
3	HIN1	Logic Input High Side Gate Driver - Phase 1
4	HIN2	Logic Input High Side Gate Driver - Phase 2
5	HIN3	Logic Input High Side Gate Driver - Phase 3
6	LIN1	Logic Input Low Side Gate Driver - Phase 1
7	LIN2	Logic Input Low Side Gate Driver - Phase 2
8	LIN3	Logic Input Low Side Gate Driver - Phase 3
9	FAULT	Fault Output
10	ITRIP	Shut Down Input
11	ENABLE	Enable Input
12	RCIN	Fault Clear Time Setting
13	TH1	Thermistor
14	TH2	Thermistor
15		None
16		None
17	U-	Low Side Emitter Connection - Phase 1
18	V-	Low Side Emitter Connection - Phase 2
19	W-	Low Side Emitter Connection - Phase 3
20	VS3,W	Output 3 - High Side Floating Supply Offset Voltage
21		None
22	VB3	High Side Floating Supply Voltage 3
23		None
24		None
25		None
26	VS2,V	Output 2 - High Side Floating Supply Offset Voltage
27		None
28	VB2	High Side Floating Supply Voltage 2
29		None
30		None
31		None
32	VS1,U	Output 1 - High Side Floating Supply Offset Voltage
33		None
34	VB1	High Side Floating Supply Voltage 1
35		None
36		None
37		None
38	VCC1	Positive Bus Input Voltage

7. Demo Board

The demo board consists of the minimum required components such as snubber capacitor and bootstrap circuit elements of STK5Q4U3xxJ series.

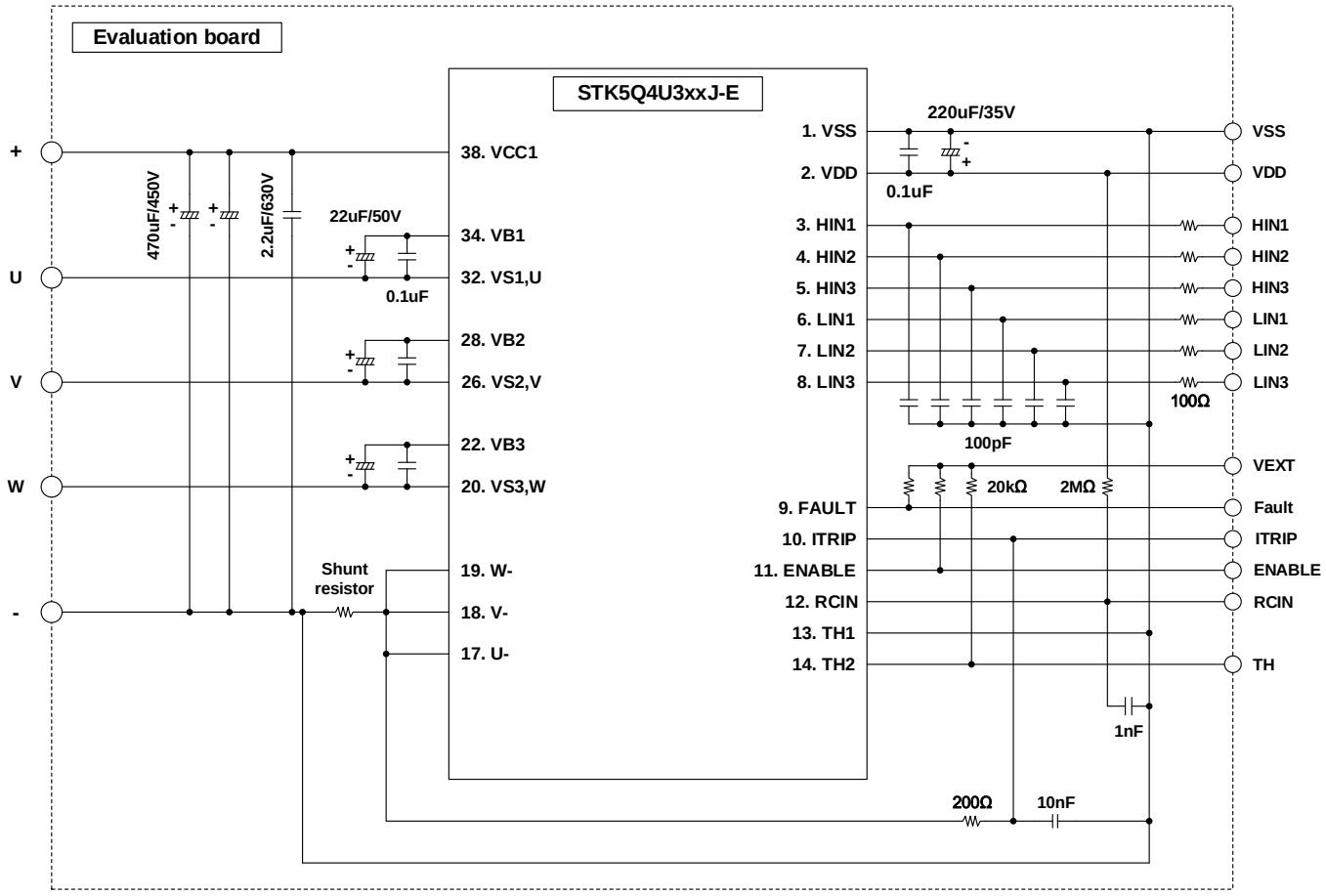
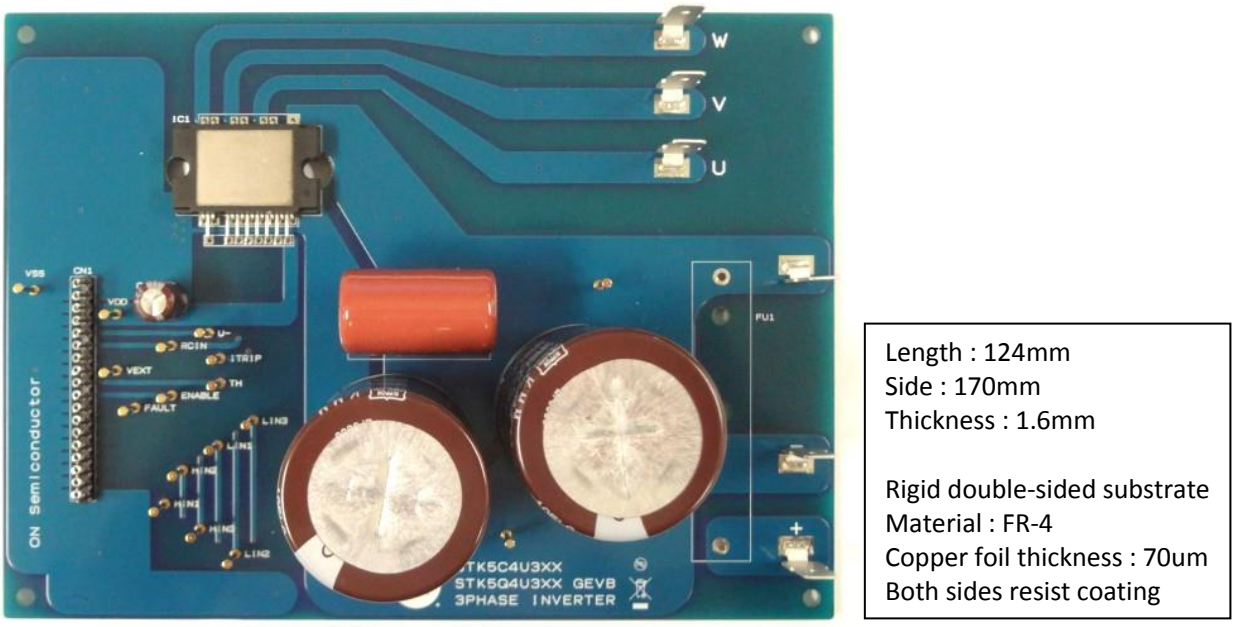


Figure 26. Evaluation board schematic



Length : 124mm
Side : 170mm
Thickness : 1.6mm

Rigid double-sided substrate
Material : FR-4
Copper foil thickness : 70um
Both sides resist coating

Figure 27. Appearance photo

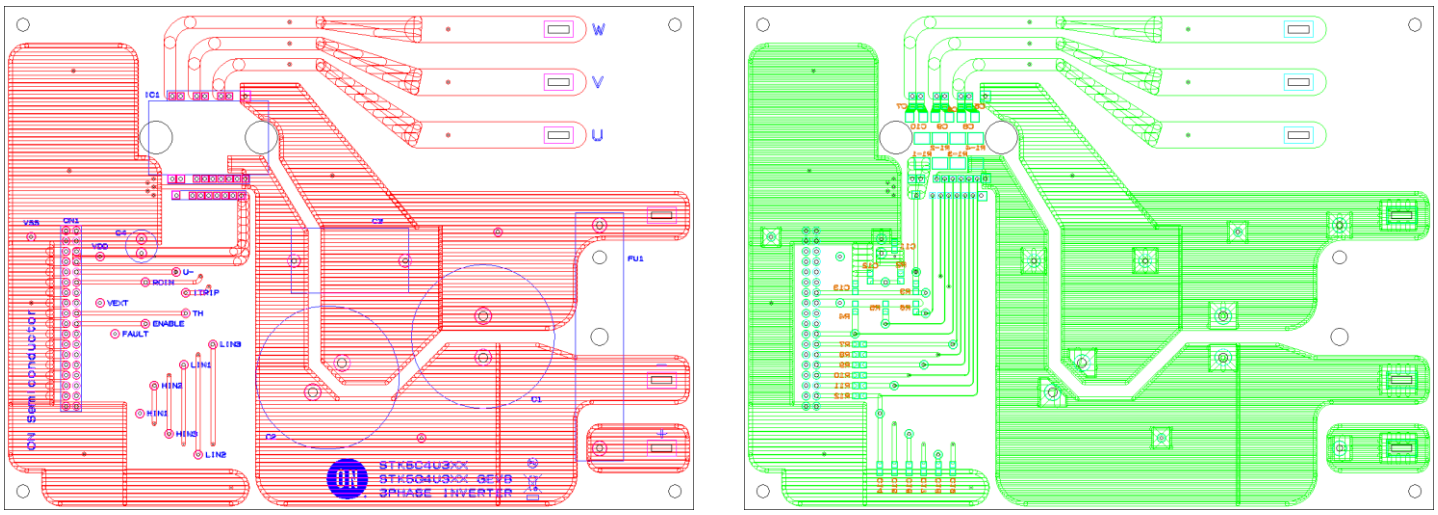


Figure 28. PCB layout (TOP view)

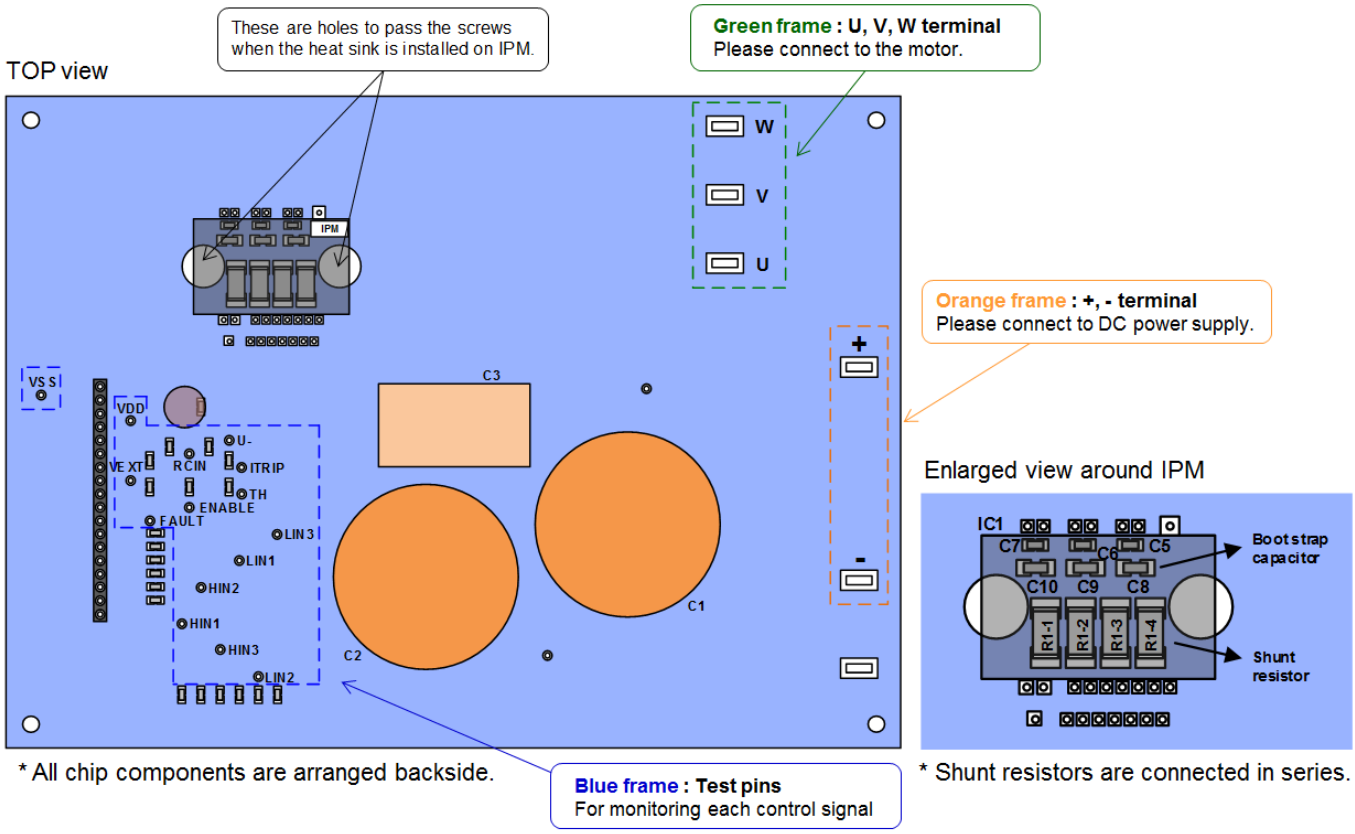


Figure 29. Description of each pin-1

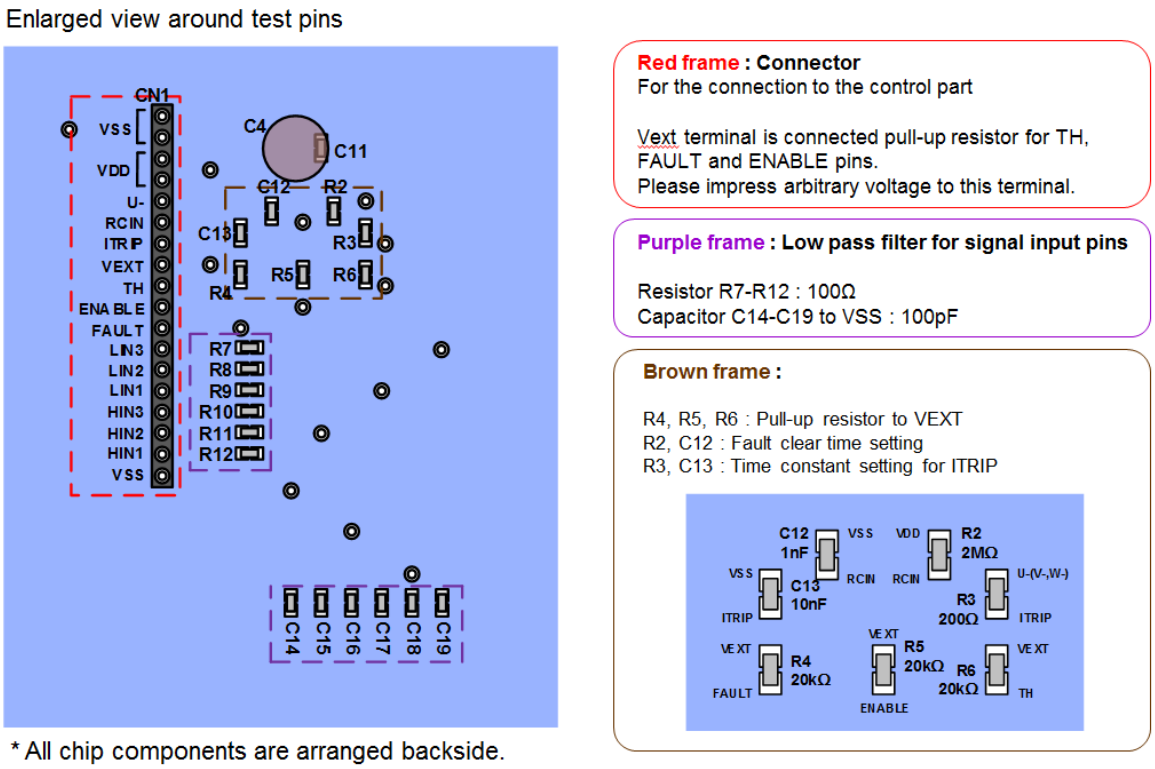


Figure 30. Description of each pin-2

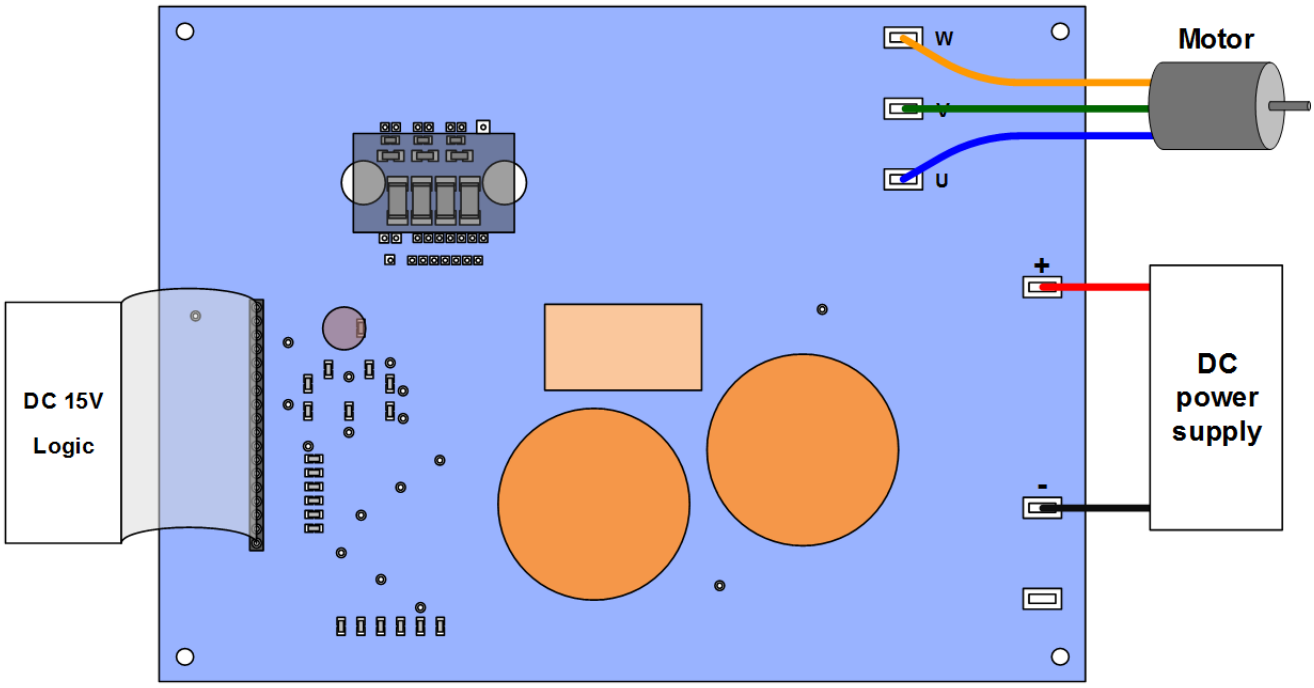


Figure 31. Connection example

Operation procedure

Step1: Please connect IPM, each power supply, logic parts and the motor to the evaluation board, and confirm that each power supply is OFF at this time.

Step2: Please impress the power supply of DC15V.

Step3: Please perform a voltage setup according to specifications, and impress the power supply between the "+" and the "-" terminal.

Step4: By inputting signal to the logic part, IPM control is started. (Therefore, please set electric charge to the boot-strap capacitor of upper side to turn on lower side IGBT before running.)

* When turning off the power supply part and the logic part, please carry out in the reverse order to above steps.