STK5F4U3E2D-E

Application Note

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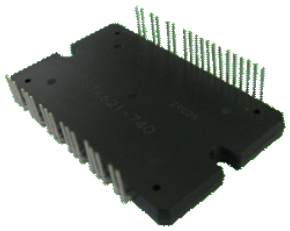
1. Product synopsis

This application handbook is intended to provide practical guidelines for the **STK5F4U3E2D-E** use.

The **STK5F4U3E2D-E** is hybrid IC based upon ONs Insulated Metal Substrate Technology (IMST) for 3-phase motor drives which contain the main power circuitry and the supporting control circuitry. The key functions are outlined below:

- Highly integrated device containing all High Voltage (HV) control from HV-DC to 3-phase outputs in a single small DIP module.
- Output stage uses IGBT/FRD technology and implements Under Voltage Protection (UVP) and Over Current Protection (OCP) with a Fault Detection output flag. Internal Boost diodes are provided for high side gate boost drive.
- Option of a combined or individual shunt resistor per phase for OCP.
- Externally accessible embedded thermistor for substrate temperature measurement.
- All control inputs and status outputs are at low voltage levels directly compatible with microcontrollers.
- Single control power supply due to internal bootstrap circuit for high side pre-driver circuit.
- Mounting points are available on DIP package

A simplified block diagram of a motor control system is shown if Figure 1.



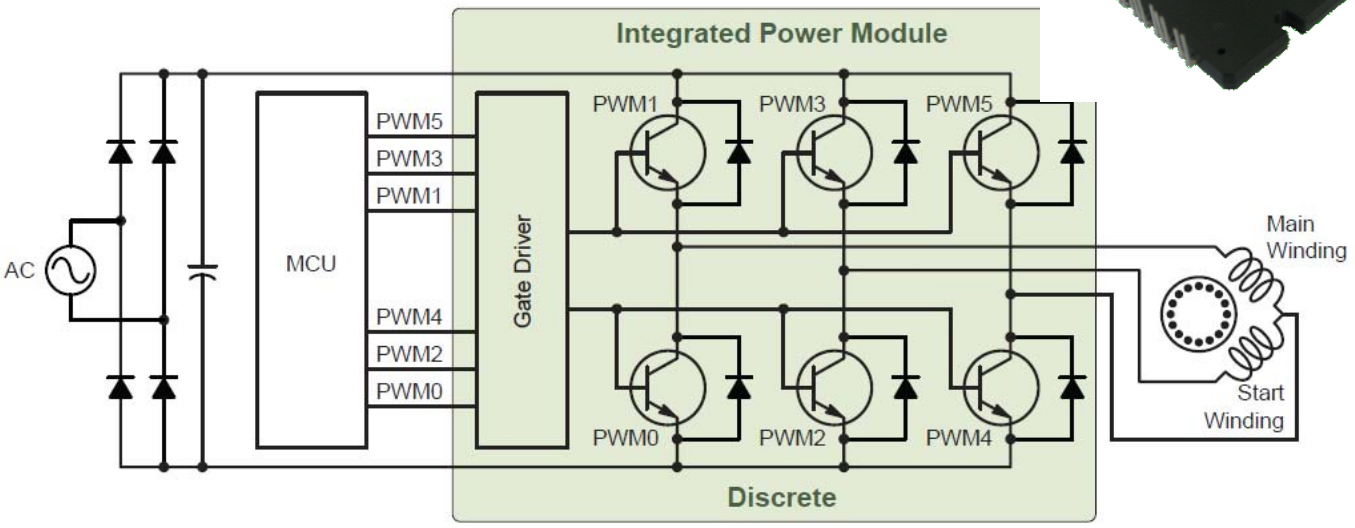


Figure 1. Motor Control System Block Diagram

2. Product description

Table1. gives an overview of the available devices, for a detailed description of the packages refer to Chapter 6.

Device	**STK5F4U3E2D-E**
Feature	Triple shunts
Package	DIP4
Voltage (VCEmax.)	600V
Current (Ic)	50A
Peak current (Ic)	100A
Isolation voltage	2000V
Shunt resistance	external

Table 1. Device Overview

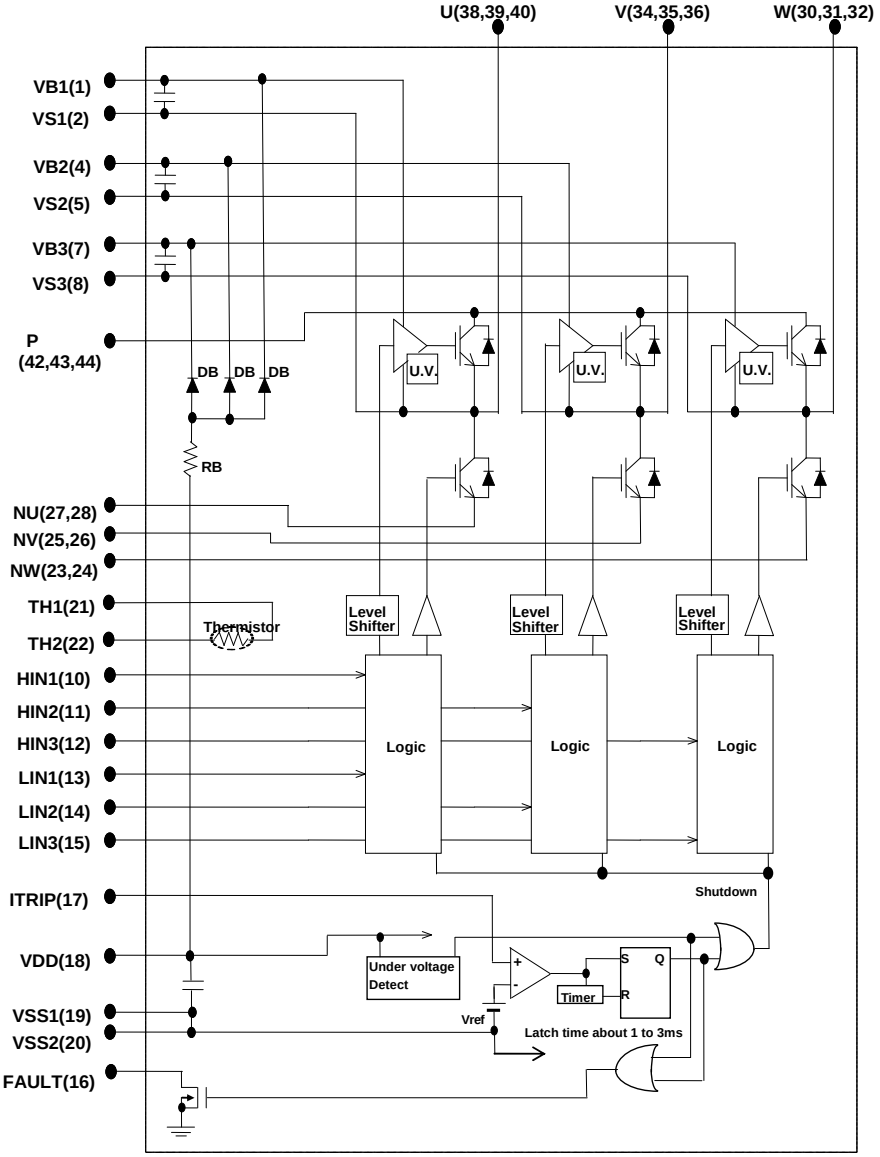


Figure 2. STK5F4U3E2D-E equivalent circuits

The high side drive is used with a bootstrap circuit to generate the higher voltage needed for gate drive. The Boost diodes are internal to the part and sourced from VDD (15V). There is an internal level shift circuit for the high side drive signals allowing all control signals to be driven directly from Vss levels common with the control circuit such as the microcontroller without requiring external level shift such as opto isolators.

3. Performance test guidelines

The following Chapter gives performance test method shown in Figures 3 to 7.

3.1. Switching time definition and performance test method

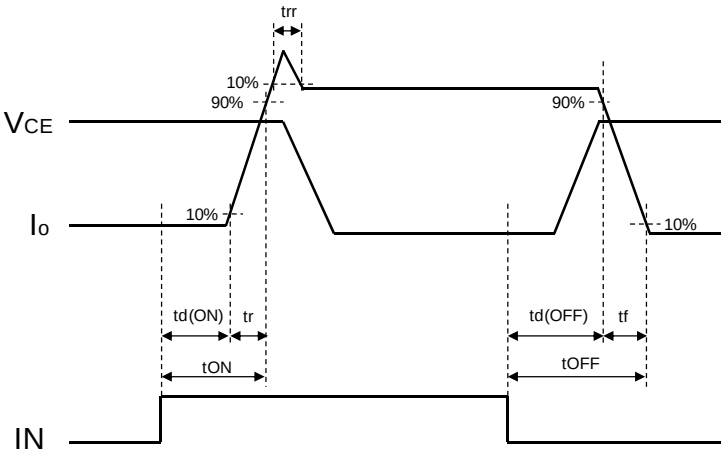


Figure 3. Switching time definition

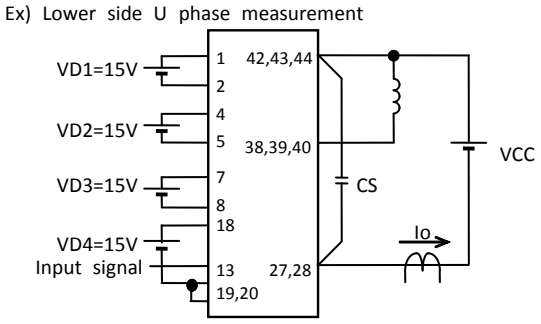


Figure 4. Evaluation circuit (Inductive load)

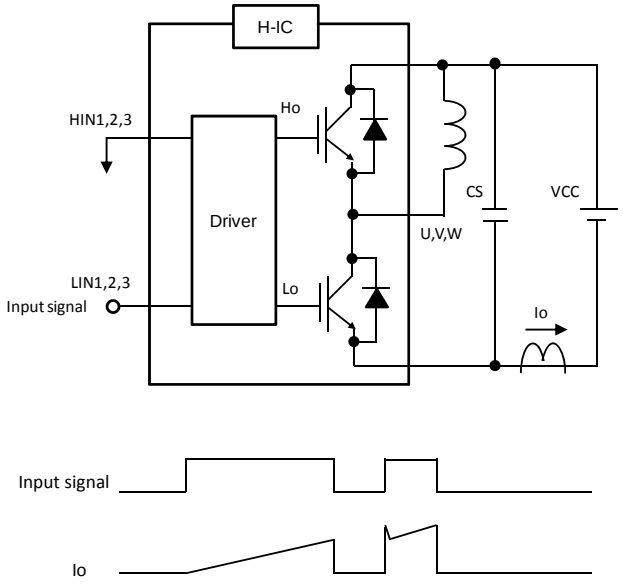


Figure 5. Switching loss circuit

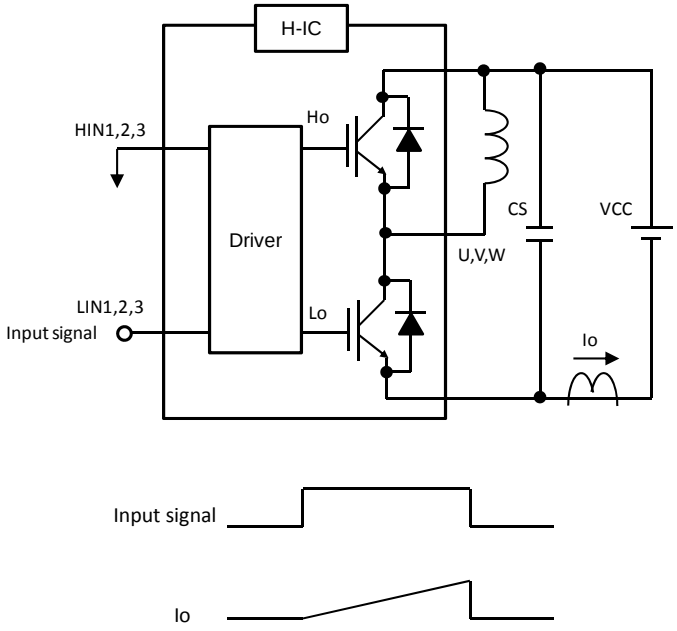


Figure 6. R.B.SOA circuit

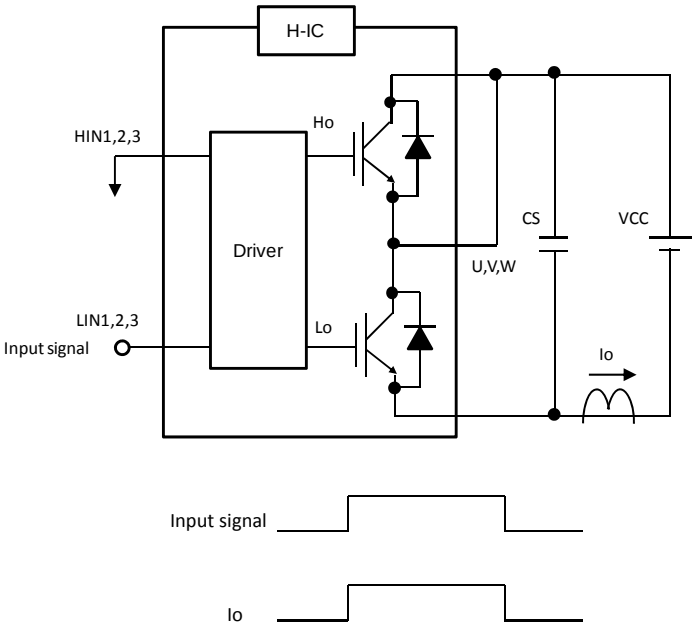


Figure 7. S.C.SOA circuit

3.2. Thermistor Characteristics

An integrated thermistor is used to sense the internal module temperature its electrical characteristic is outlined below.

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Resistance	R_{25}	Tc=25°C	97	100	103	kΩ
Resistance	R_{100}	Tc=100°C	4.93	5.38	5.88	kΩ
B-Constant(25-50°C)	B		4165	4250	4335	K
Temperature Range			-40		+125	°C

Table 2. NTC Thermistor value

Rt is the value of the integrated NTC thermistor at Tc=25°C. The resistance value is 100kΩ±3% and the value of the B-Constant (25-50°C) is 4250K±2%. The temperature depended value is calculated as shown in the formula.

$$R(t) = R_{25} \times e^{B\left(\frac{1}{T} - \frac{1}{298}\right)}$$

The resulting in the NTC values over temperatures

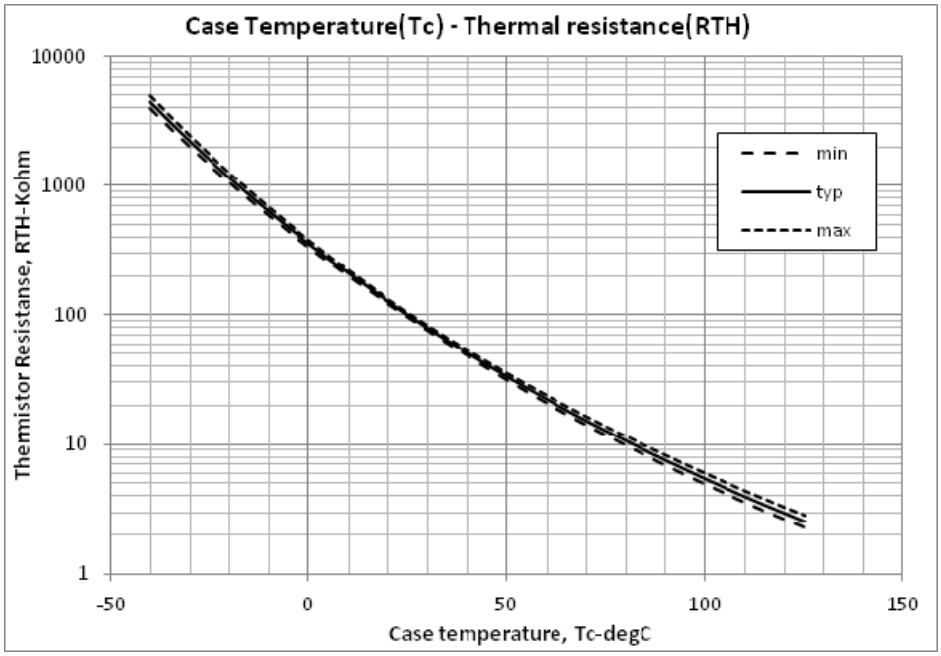


Figure 8. typical NTC value over temperature

4. Protective functions and Operation Sequence

This chapter describes the protection features.

- over current protection
- short circuit protection
- under Voltage Lockout (UVLO) protection
- cross conduction prevention

4.1. Over current protection

In difference to the internal single shunt series modules the STK5F4U3E2D-E module utilizes an external shunt resistor for the OCP functionality. As shown in Figure 9 the emitters of all three lower side IGBTs brought out to module pins. An external "over current protection circuitry" consisting of the shunt resistor and an RC filter network define the trip level.

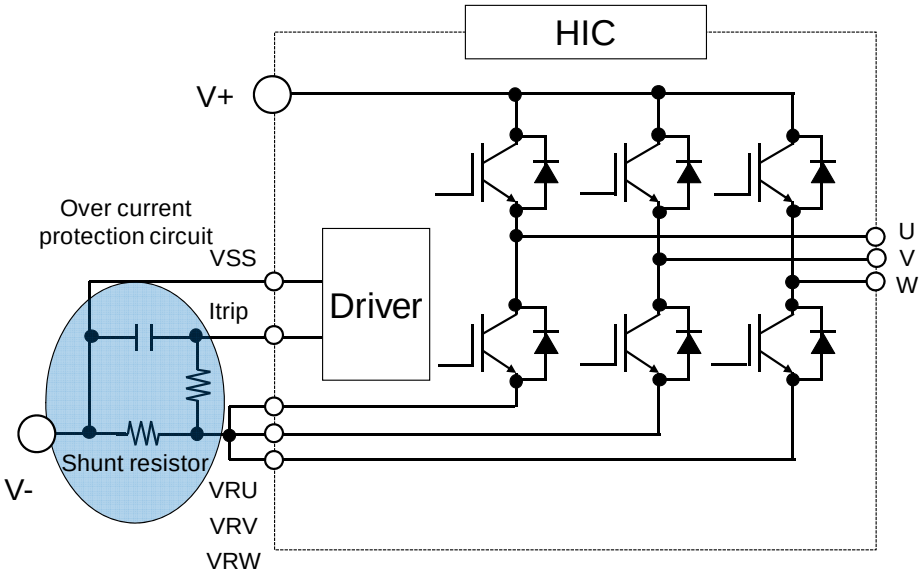


Figure 9. Over-current protection circuit setting

The OCP function is implemented by comparing the voltage on the Itrip input to an internal reference of 0.49V (typ). In case the voltage on this terminal i.e. across the shunt resistor exceeds the trip level an OCP fault is triggered.

Note: The current value of the OCP needs to be set by correctly sizing the external shunt resistor to less than 2x of the modules rated current.

In case of an OCP event all internal gate drive signal for the IGBTs of all three phases become inactive and the FLT/EN fault signal output is activated (low).

An RC filter is used on the Itrip input to prevent an erroneous OCP detection due to normal switching noise and/or recovery diode current. The time constant of that RC filter should be set to a value between 1.5µ to 2µs. In any case the time constant must be shorter than the IGBTs short current safe operating area (SCSOA) according to Figure 10. The resulting OCP level due to the filter time constant is shown in Figure 11.

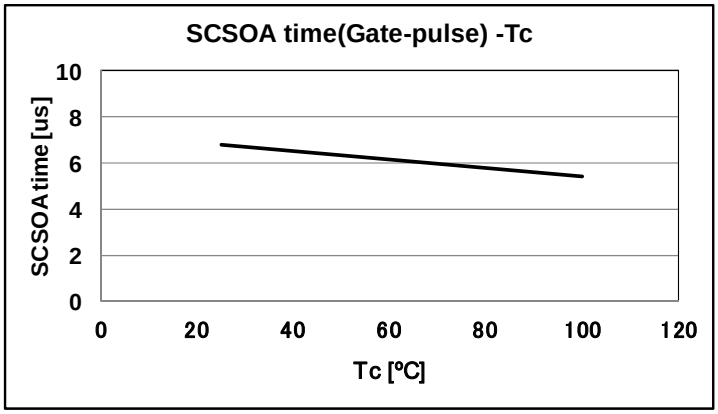


Figure 10. IGBT SCSOA

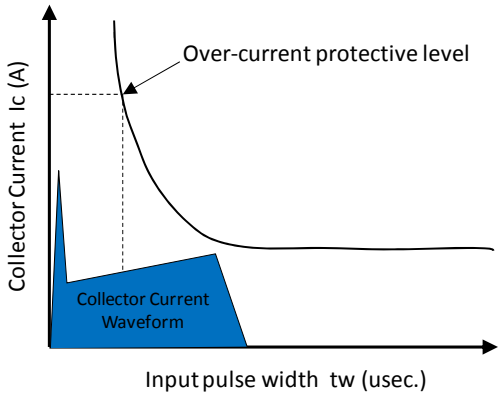


Figure 11. filter time constant

For optimal performance all traces around the shunt resistor need to be kept as short as possible

Figure 12. shows the sequence of events in case of an OCP event.

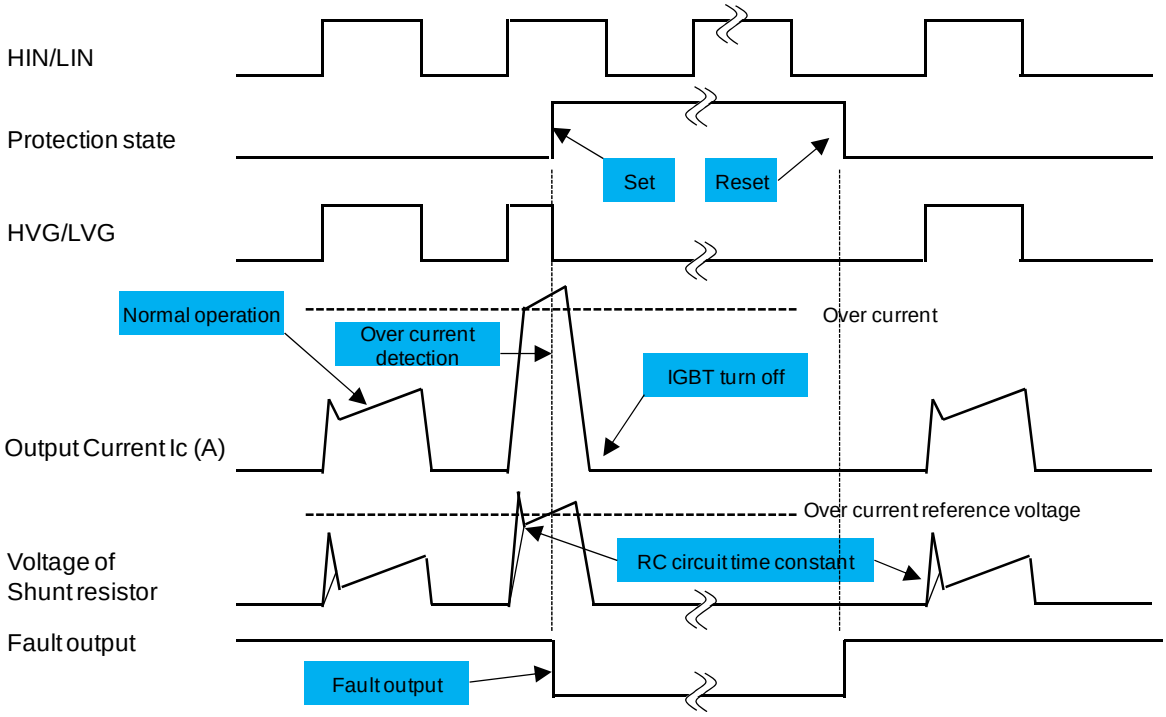


Figure 12. Over current protection Timing chart

4.2. Under Voltage Lockout Protection

The UVLO protection is designed to prevent unexpected operating behavior as described in Table 3. Both High-side and Low-side have UV protecting function. However the fault signal output only corresponds to the Low-side UVLO Protection. During the UVLO state the fault output is continuously driven (low).

VDD Voltage (typ. Value)	Operation behavior
< 12.5V	As the voltage is lower than the UVLO threshold the control circuit is not fully turned on. A perfect functionality cannot be guaranteed.
12.5 V – 13.5 V	IGBTs can work, however conduction and switching losses increase due to low voltage gate signal.
13.5 V – 16.5 V	Recommended conditions
16.5 V – 20.0 V	IGBTs can work. Switching speed is faster and saturation current higher, increasing short-circuit broken risk.
> 20.0 V	Control circuit is destroyed. Absolute max. rating is 20 V.

Table 3. *Module operation according to control supply voltage*

The sequence of events in case of a low side UVLO event (IGBTs turned off and active fault output) is shown in Figure 13. Figure 14 shows the same for a high side UVLO (IGBTs turned off and no fault output).

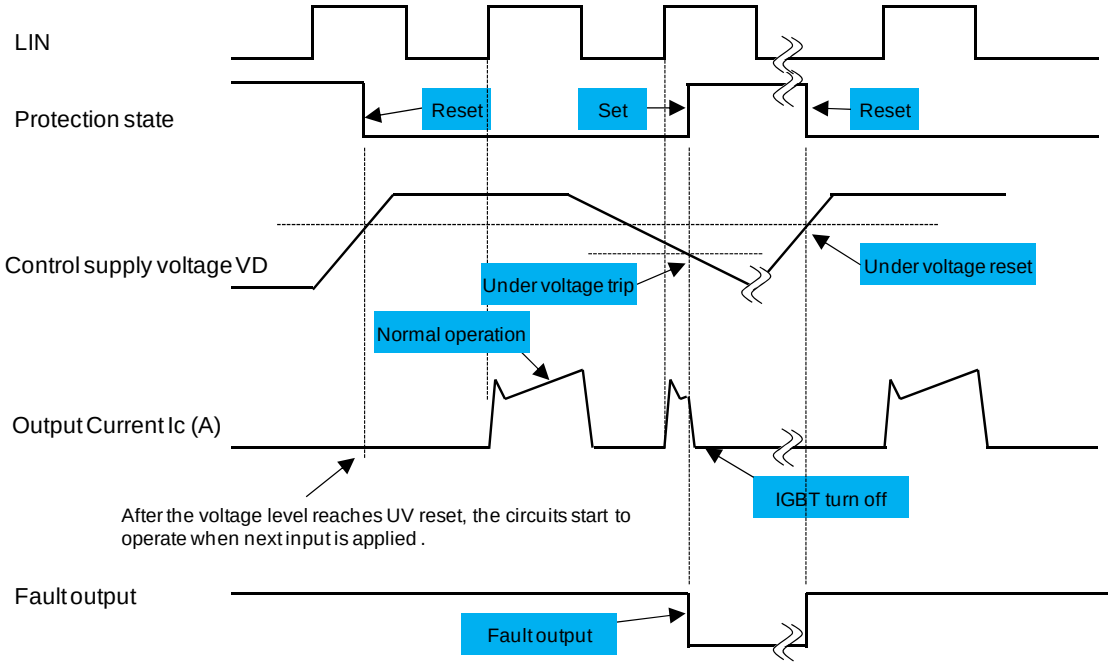


Figure 13. Low side UVLO timing chart

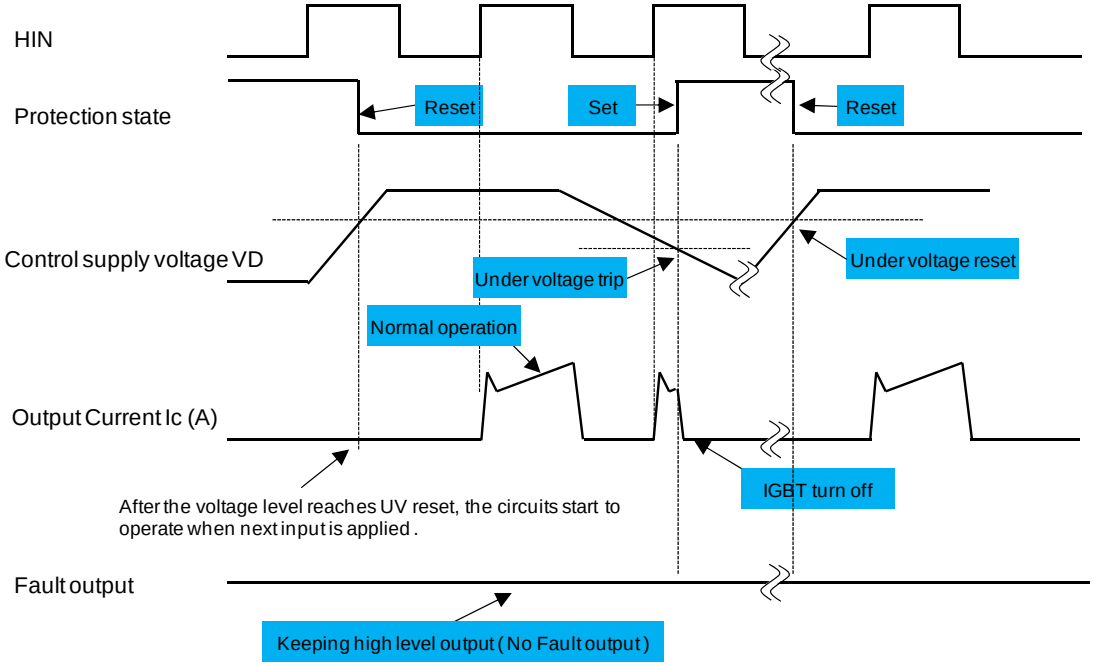


Figure 14. High side UVLO timing chart

4.3. Cross conduction prevention

The STK5F4U3E2D-E module implement a cross conduction prevention logic at the pre-driver to avoid simultaneous drive of the low- and high-side IGBTs as shown in Figure 15.

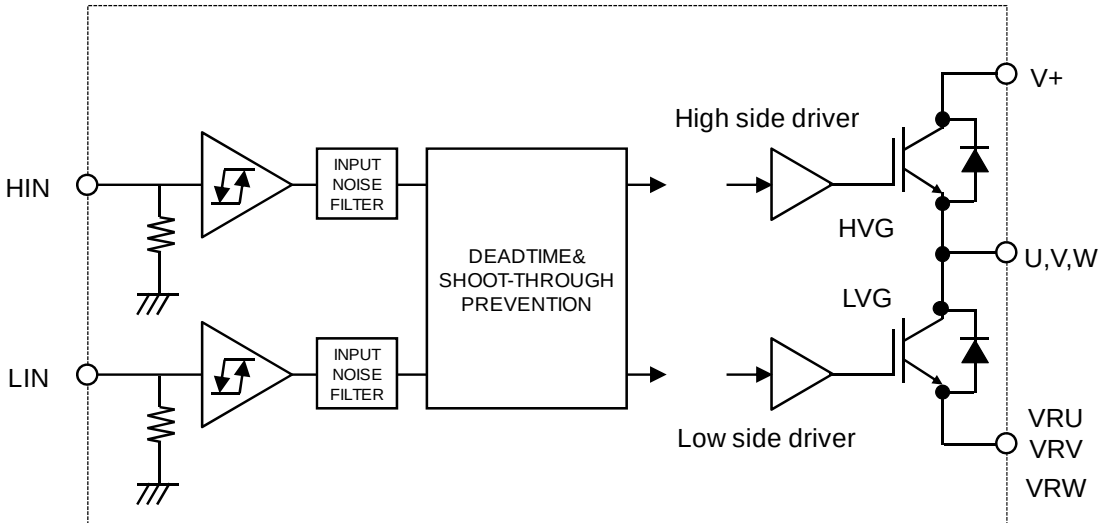


Figure 15. Cross Input Conduction Prevention

In case of both high and low side drive inputs are active (high) the logic prevents both gates from being driven – a corresponding timing diagram can be found in Figure 16 below.

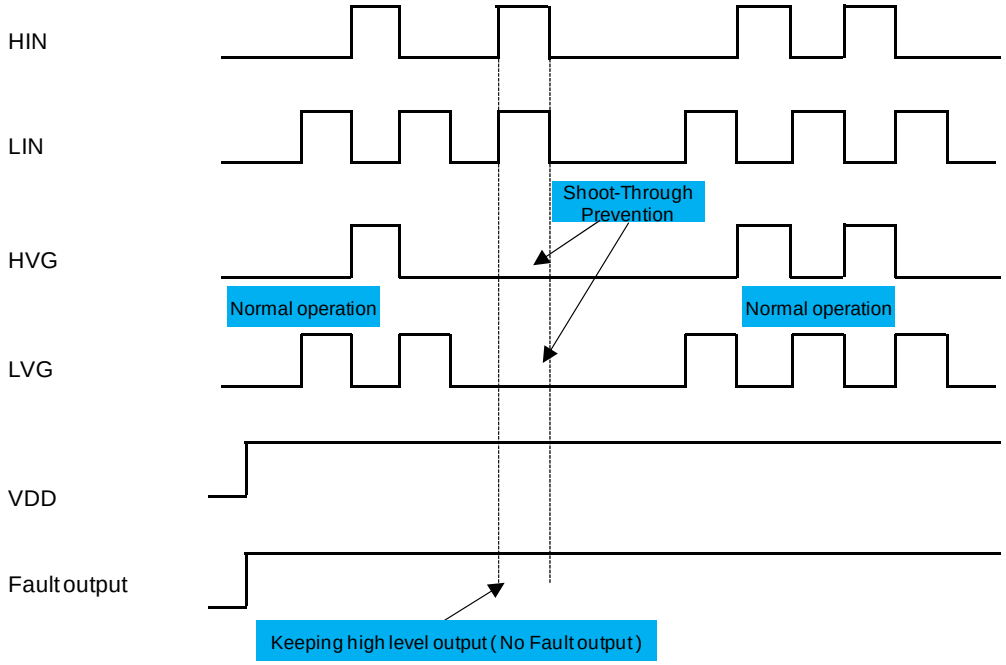


Figure 16. cross conduction prevention timing diagram

Even so cross conduction on the IGBTs due to incorrect external driving signals is prevented by the circuitry the driving signals (HIN and LIN) need to include a “dead time”. This period where both inputs are inactive between either one becoming active is required due to the internal delays within the IGBTs. Figure 17 shows the delay from the HIN-input via the internal HVG to high side IGBT, the similar path for the low side and the resulting minimum dead time which is equal to the potential shoot through period:

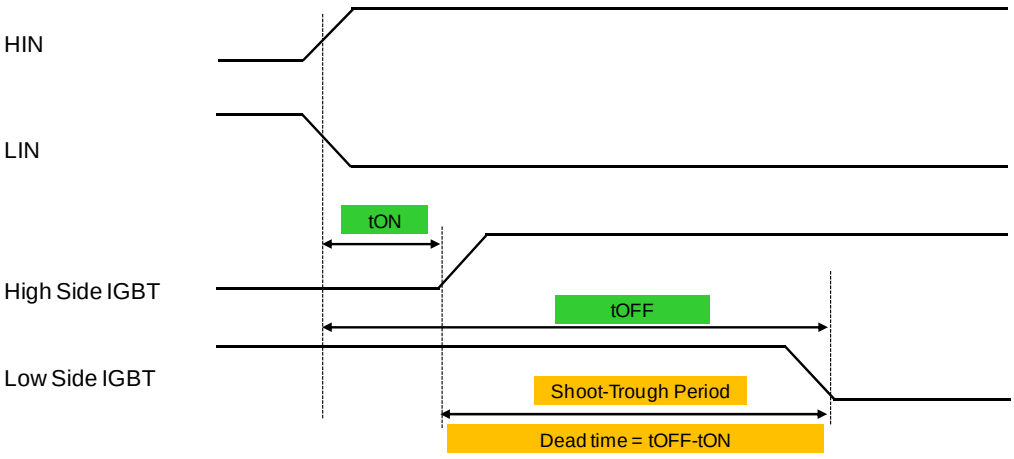


Figure 17. Shoot Trough Period

5. PCB design and mounting guidelines

This chapter provides guidelines for an optimized design and PCB layout as well as module mounting recommendations to appropriately handle and assemble the HIC module.

5.1. Application (schematic) design

The following two figures 18 gives an overview of the external circuitry's functionality when designing with the STK5F4U3E2D-E module.

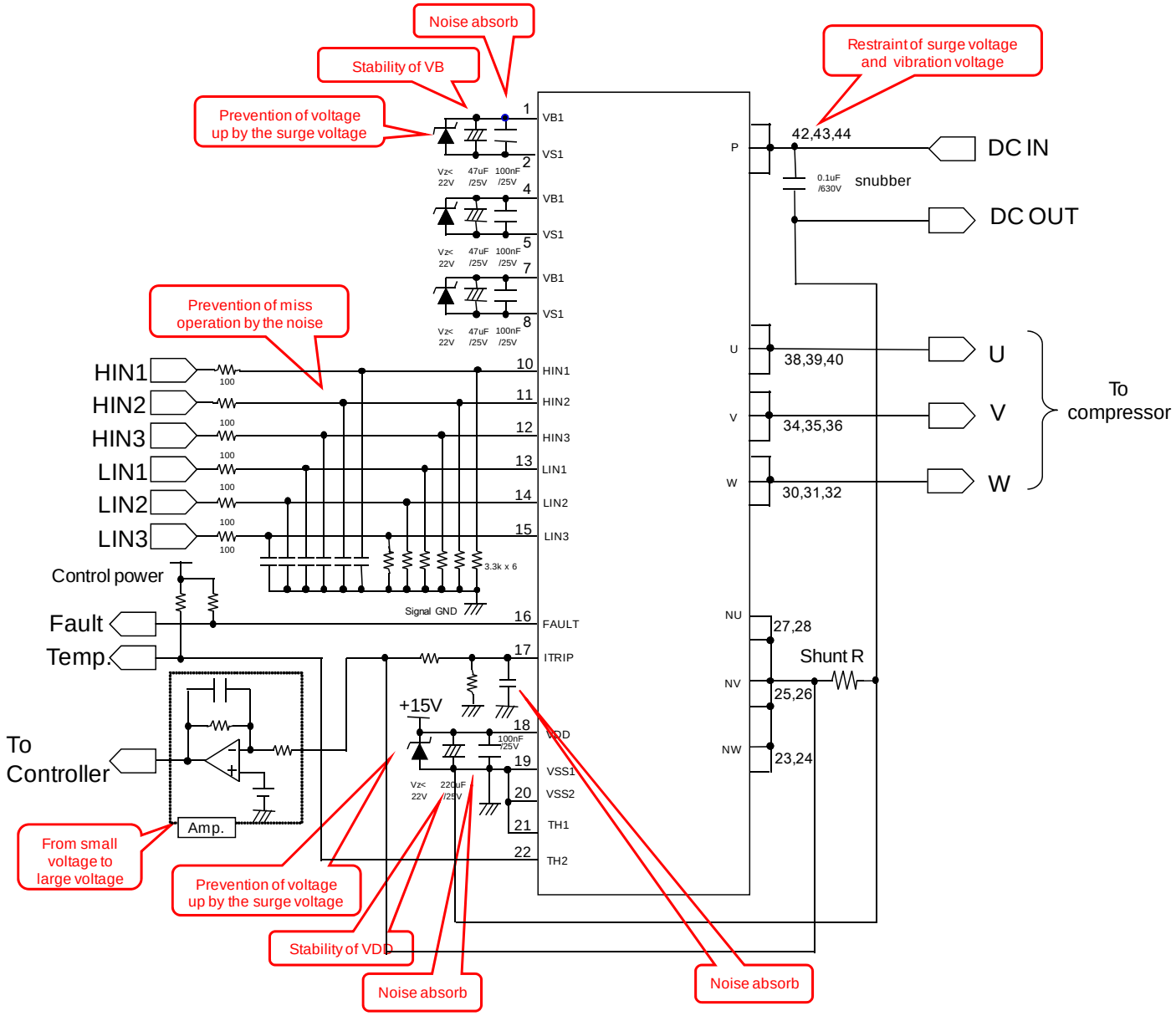


Figure 18. STK5F4U3E2D-E application circuit

5.2. Notes on PCB design

(1) External shunt resistor should be placed as close as possible to three phase output term inal (NU,NV,NW).
(2) Power side GND and control side GND must not be a solid common wiring.
Signal side GND is recommended to design the patterns in one point of connection to V ssterminal so that it does not flow to the power side the GND signal current.
(3) The power GND side and the control GND side a point of connection, GND wiring, pleas e be as short as possible.
(4) Snubber capacitor between the positive terminal and the negative terminal of the power, please place as close as possible to the hybrid IC.
(5) Capacitor and zener diode should be placed close to the terminal.
(6) C-R filter should be placed close to the terminal.
(7) Capacitor and zener diode should be placed close to the terminal.

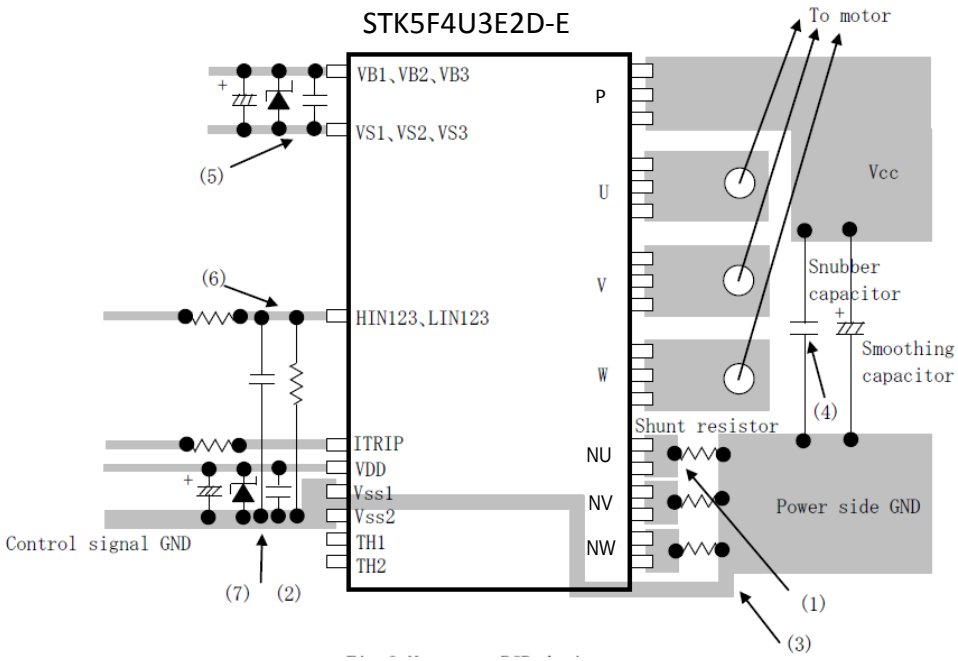


Figure 19. STK5F4U3E2D-E application circuit

5.3. Pin by pin design and usage notes

This section provides pin by pin PCB layout recommendations and usage notes. For a complete list of module pins refer to the datasheet or Chapter 6.

P & N These pins are connected with the main DC power supply. The applied voltage is up to the Vcc level. Overvoltage on these pins could be generated by voltage spikes during switching at the floating inductance of the wiring. To avoid this behavior the wire traces need to be as short as possible to reduce the floating inductance. In addition a snubber capacitor needs to be placed as close as possible to these pins to stabilize the voltage and absorb voltage surges.

U, V, W These terminals are the output pins for connecting the 3-phase motor. They share the same GND potential with each of the high side control power supplies. Therefore they are also used to connect the GND of the bootstrap capacitors. These bootstrap capacitors should be placed as close to the module as possible.

VDD, VSS

These pins connect with the circuitry of the internal protection and pre-drivers for the low -side power elements and also with the control power supply of the logic circuitry. Voltage to input these terminals is monitored by the under voltage protection circuit. The VSS terminal is the reference voltage for the control inputs signals as well as Fault and ISO. VSS is connected with the " N" terminal internally. The main circuit does typically not draw current from VSS.
When the "N" and "VSS" pins are connected externally care must be taken to select a single connection point as close as possible to the IC. In case of multiple connections to these pins and longer traces being used, the overcurrent protection level may become low. Therefor this should be avoided.

VB1, VB2, VB3

The VBx pins are internally connected to the positive supply of the high-side drivers. The supply needs to be floating and electrically isolated. The boot-strap circuit shown in Figure 20 forms this power supply individually for every phase. Due to integrated boot resistor and diode (RB & DB) only an external boot capacitor (CB) is required.

There are two current path to charge CB – depicted as ① and ②.

① when the low side power IGBT is ON

② when motor current is flows in CB

The capacitor is discharged while the high-side driver is activated.

Thus CB needs to be selected taking the maximum on time of the high side and the switching frequency into account.

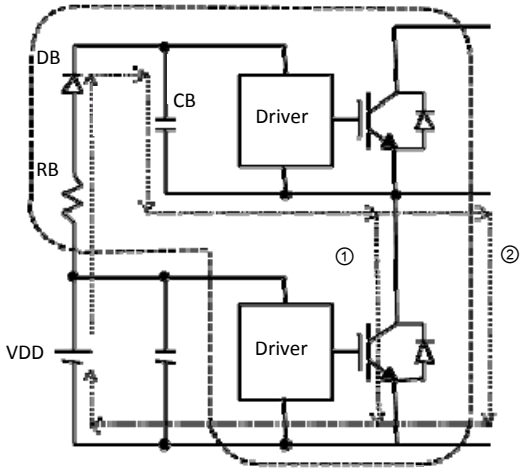


Figure 20. Boot Strap Circuit

To set an initial charge on CB a high ohmic resistor can be used between the motor and the "N" pins – considering the max voltage rating of the device.

The voltages on the high side drivers are individually monitored by the under voltage protection circuit. In case an UVP event is detected on a phase its operation is stopped.

Typically a CB value of less or equal 47uF (±20%) is used. In case the CB value needs to be higher an external resistor (of apx. 20Ω or less) should be used in series with the capacitor to avoid high currents which can cause malfunction of the hybrid IC.

HIN1, LIN1, HIN2, LIN2, HIN3, LIN3

These pins are the control inputs for the power stages. The inputs on HIN1/HIN2/HIN3 control the high-side transistors of U/V/W, and the inputs on LIN1/LIN2/LIN3 control the low-side transistors of U/V/W respectively. The input are active high and the input thresholds VIH and VIL are 5V compatible to allow direct control with a microcontroller system

Simultaneous activation of both low and high side is prevented internally to avoid shoot through at the power stage. However, due to IGBT switching delays the control signals must include a dead-time.

The equivalent input stage circuit is shown in Figure 21.

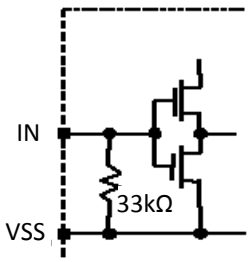


Figure 21. Internal Input Circuit

For fail safe operation the control inputs are internally tied to VSS via a 33kΩ (typ) resistor. To avoid switching captured by external wiring to influence the module behavior an additional external low-ohmic pull-down resistor with a value of 2.2kΩ-3.3kΩ should be used.

The output might not respond when the width of the input pulse is less than 1µs (both ON and OFF).

Fault or FLT/EN

The Fault pin is an active low input and open-drain output. It is used to indicate an internal fault condition of the module and also can be used to disable the module operation. The I/O structure is shown in Figure 22.

The internal sink current IoSD during an active fault is nominal 2mA @ 0.1V. Depending on the interface supply voltage the external pull-up resistor (RP) needs to be selected to set the low voltage below the VIL trip level.

For the commonly used supplies VP:

VP = 15V -> RP >= 20kΩ

VP = 5V -> RP>= 6.8kΩ

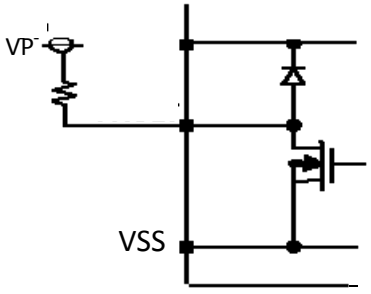


Figure 22. Fault Connection

For a detailed description of the fault operation refer to Chapter 4.
Note: The Fault signal does automatically re-started after the causing protection event end AND after the fault timeout of min. 18ms (STK5F1U3xx-E) respectively 2ms (STK5F4U3xx-E). Therefore the input needs to be driven low externally activated as soon as a fault is detected.

TH An internal thermistor to sense the substrate temperature is connected between VSS and the TH pins. In conjunction with an external pull-up resistor Rth a module temperature monitor can be build.

Note: with this mimic only the substrate temperature can be monitored.

5.4. Heat sink mounting and torque

If a heat sink is used, insufficiently secure or inappropriate mounting can lead to a failure of the heat sink to dissipate heat adequately. This can lead to an inability of the device to provide its inherent performance, a serious reduction in reliability, or even destruction, burst and burn of the device due to overheating.

The following general points should be observed when mounting H-IC on a heat sink:

1. Verify the following points related to the heat sink:
   - There must be no burrs on aluminum or copper heat sinks.
   - Screw holes must be countersunk.
   - There must be no unevenness in the heat sink surface that contacts H-IC.
   - There must be no contamination on the heat sink surface that contacts H-IC.

2. Highly thermal conductive silicone grease needs to be applied to the whole back (aluminum substrate side) uniformly, and mount H-IC on a heat sink. Upon re-mounting apply silicone grease (100um to 200um) again uniformly.

3. For an intimate contact between the H-IC and the heat sink, the mounting screws should be tightened gradually and sequentially while a left/right balance in pressure is maintained. Either a bind head screw or a truss head screw is recommended. Please do not use tapping screw. We recommend using a flat washer in order to prevent slack. The standard heat sink mounting condition of an STK5F4U3E2D-E is as follows.

Item	Recommended Condition
Pitch	68.0 ± 0.1mm (Please refer to Package Outline Diagram)
Screw	diameter : M4 Bind machine screw, Truss machine screw, Pan machine screw
Washer	Plane washer The size is D:9mm, d:4.8mm and t:0.8mm (Fig.2) JIS B 1256
Heat sink	Material : copper or Aluminum Warpage (the surface that contacts H-IC) : -50 to 100 µm Screw holes must be countersunk. No contamination on the heat sink surface that contacts H-IC.
Torque	Final tightening : 0.79 to 1.17Nm Temporary tightening : 20 to 30 % of final tightening
Grease	Silicon grease Thickness : 100 to 200 µm Uniformly apply silicon grease to whole back. (Fig.3)

Table 4. heat sink mounting

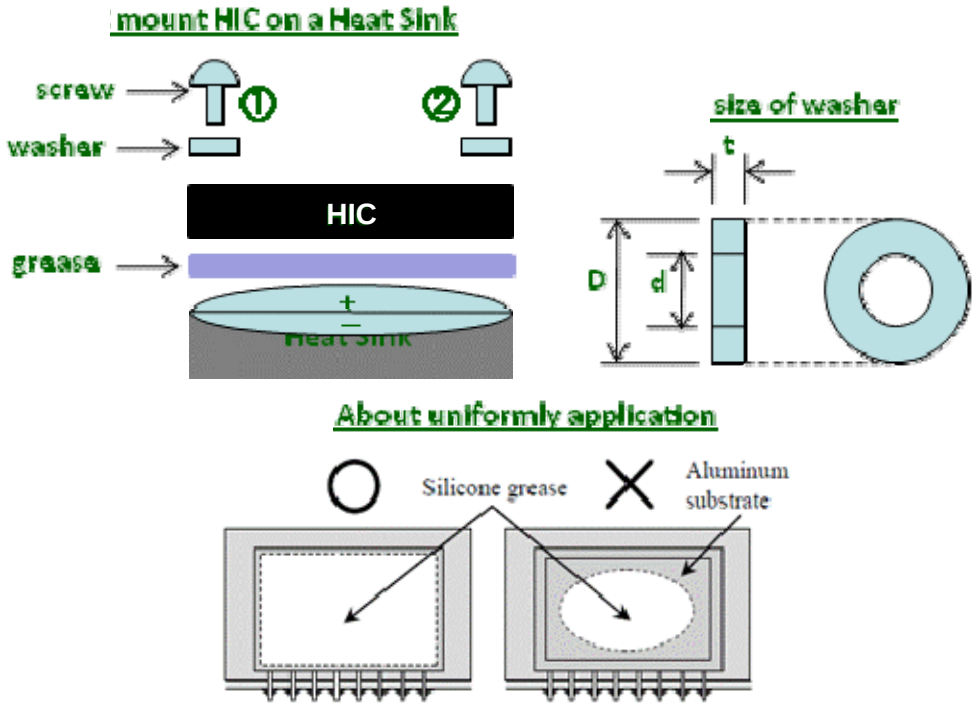


Figure 1. Mount on Heat Sink

steps to mount an HIC on a heat sink
1st: Temporarily tighten maintaining a left/right balance.
2nd : Finally tighten maintaining a left/right balance.

5.5. Mounting and PCB considerations (general information)

In designs in which the printed circuit board and the heat sink are mounted to the chassis independently, use a mechanical design which avoids a gap between H-IC and the heat sink, or which avoids stress to the lead frame of H-IC by an assembly that a moving H-IC is forcibly fixed to the heat sink with a screw.

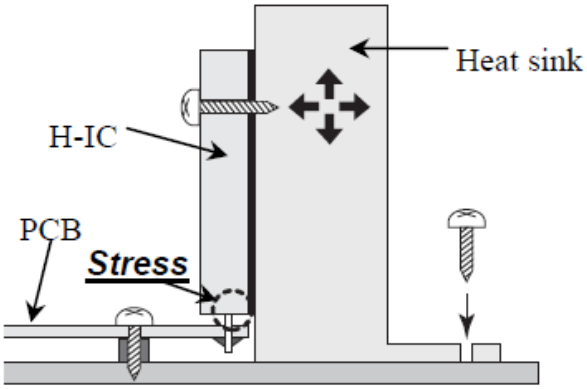


Figure 2. Fix to Heat Sink

Do not mount H-IC with a tilted orientation. This can result in stress being applied to the lead frame and H-IC substrate could short out tracks on the printed circuit board. Always mount the H-IC vertically. If stress is given by compulsory correction of a lead frame after the mounting, a lead frame may drop out. Be careful of this point.

When designing the PCB layout take care that the bent part portion of the lead frame pins does not short-circuit to VIA holes or tracks on the PCB.

Since the use of sockets to mount H-IC can result in poor contact with H-IC leads, we strongly recommend making direct connections to PCB.

H-IC modules are flame retardant. However, under certain conditions, it may burn, and poisonous gas may be generated or it may explode. Therefore, the mounting structure of the H-IC module should also be flame retardant.

Mounting on a Printed Circuit Board

1. Align the lead frame with the holes in the printed circuit board and do not use excessive force when inserting the pins into the printed circuit board. To avoid bending the lead frames, do not try to force pins into the printed circuit board unreasonably.
2. Do not insert H-IC into printed circuit board with an incorrect orientation, i.e. be sure to prevent reverse insertion. H-IC may be destroyed, exploded, burned or suffer a reduction in their operating lifetime by this mistake.
3. Do not bend the lead frame.

5.6. Cleaning

H-IC has a structure that is unable to withstand cleaning. As a basic policy, do not clean independent H-IC or printed circuit boards on which an H-IC is mounted.

6. Package Outline

STK5F4U3E2D-E is DIP4 package. (Dual-line-package)

6.1. Package outline and dimension

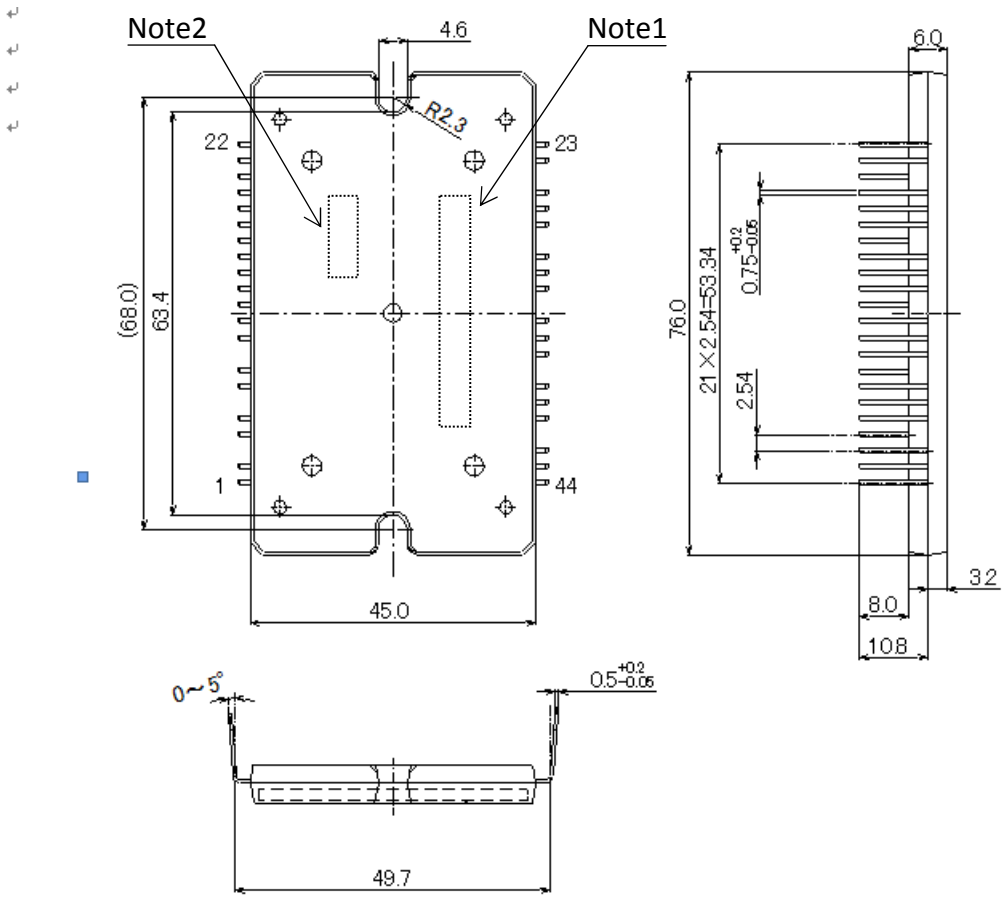


Figure 3. STK5F4U3E2D-E Package Outline

6.2. Laser Marking

Note 1: The labeling designates the model number – centered within a field of 4.5 mm width and 35 mm length

Note2 ： The labeling designates the order number – right justified within a field of 3.5 mm width and 14 mm length

*We examine the design except for the above.

6.3. Pin Out Description

Pin No.	Name	Description	Pin No.	Name	Description
1	VB1	High side floating supply voltage 1	44	P	Positive bus input voltage
2	VS1	High side floating supply offset voltage	43	P	Positive bus input voltage
3	-	Without pin	42	P	Positive bus input voltage
4	VB2	High side floating supply voltage 2	41	-	Without pin
5	VS2	High side floating supply offset voltage	40	U	U+ phase output
6	-	Without pin	39	U	U+ phase output
7	VB3	High side floating supply voltage 3	38	U	U+ phase output
8	VS3	High side floating supply offset voltage	37	-	Without pin
9	-	Without pin	36	V	V+ phase output
10	HIN1	Logic input high side driver-Phase1	35	V	V+ phase output
11	HIN2	Logic input high side driver-Phase2	34	V	V+ phase output
12	HIN3	Logic input high side driver-Phase3	33	-	Without pin
13	LIN1	Logic input low side driver-Phase1	32	W	W+ phase output
14	LIN2	Logic input low side driver-Phase2	31	W	W+ phase output
15	LIN3	Logic input low side driver-Phase3	30	W	W+ phase output
16	FAULT	Fault out	29	-	Without pin
17	ITRIP	Over-current protection level setting pin	28	NU	U- phase output
18	VDD	+15V main supply	27	NU	U- phase output
19	VSS1	Negative main supply	26	NV	V- phase output
20	VSS2	Negative main supply	25	NV	V- phase output
21	TH1	Thermistor out	24	NW	W- phase output
22	TH2	Thermistor out	23	NW	W- phase output

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