

# STK5F1U3xx series



ON Semiconductor®

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## Application Note

### 1. Product synopsis

This application handbook is intended to provide practical guidelines for the **STK5F1U3xx series** use.

The **STK5F1U3xx series** is hybrid ICs based upon ON's Insulated Metal Substrate Technology (IMST) for 3-phase motor drives which contain the main power circuitry and the supporting control circuitry. The key functions are outlined below:

- Highly integrated device containing all High Voltage (HV) control from HV-DC to 3-phase outputs in a single small DIP module.
- Output stage uses IGBT/FRD technology and implements Under Voltage Protection (UVP) and Over Current Protection (OCP) with a Fault Detection output flag. Internal Boost diodes are provided for high side gate boost drive.
- Option of a combined or individual shunt resistor per phase for OCP.
- Externally accessible embedded thermistor for substrate temperature measurement.
- All control inputs and status outputs are at low voltage levels directly compatible with microcontrollers.
- Single control power supply due to Internal bootstrap circuit for high side pre-driver circuit.
- Mounting points are available on DIP package

A simplified block diagram of a motor control system is shown in Figure 1.

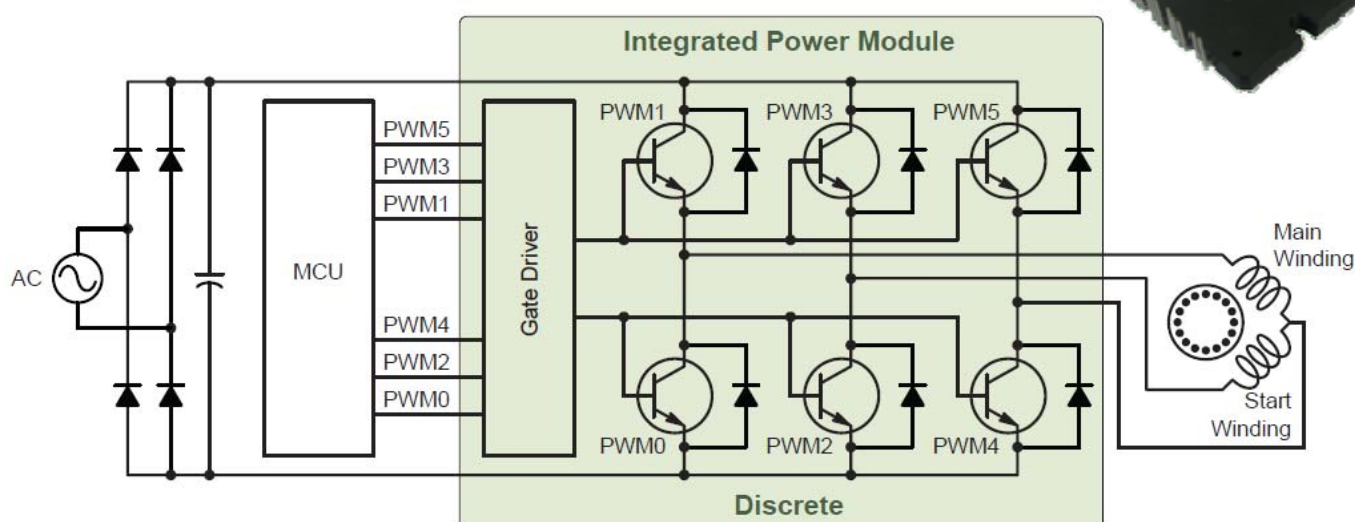


Figure 1. Motor Control System Block Diagram

## 2. Product description

Table1. gives an overview of the available devices, for a detailed description of the packages refer to Chapter 6.

Device	STK5F1U3C2D-E	STK5F1U3E2D-E
Feature	Single shunt	
Package	DIP4	
Voltage (VCEmax.)	600V	600V
Current (Ic)	30A	50A
Peak current (Ic)	49A	76A
Isolation voltage	2000V	2000V
Shunt resistance	13.5mΩ	9mΩ

Table 1. Device Overview

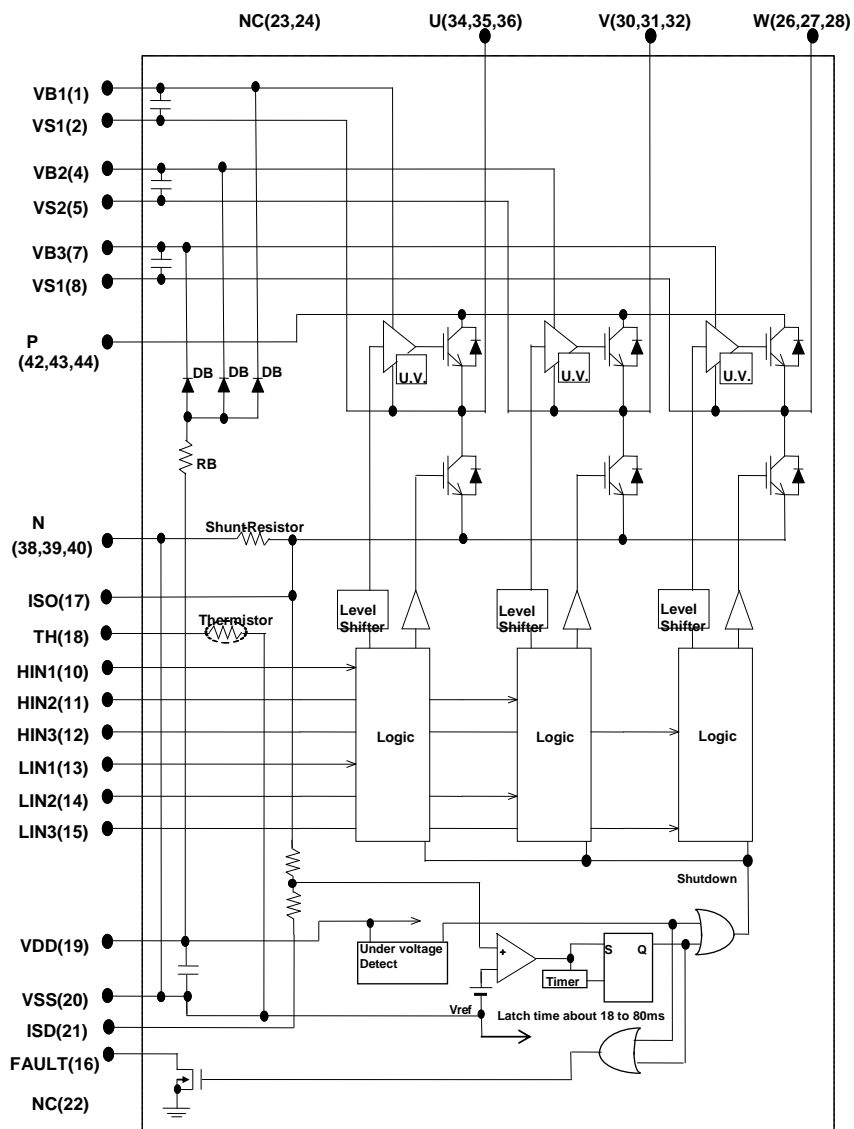


Figure 2. STK5F1U3xx series equivalent circuits

The high side drive is used with a bootstrap circuit to generate the higher voltage needed for gate drive. The Boost diodes are internal to the part and sourced from VDD (15V). There is an internal level shift circuit for the high side drive signals allowing all control signals to be driven directly from Vss levels common with the control circuit such as the microcontroller without requiring external level shift such as opto isolators.

## 3. Performance test guidelines

The following Chapter gives performance test method shown in Figures 3 to 7.

### 3.1. Switching time definition and performance test method

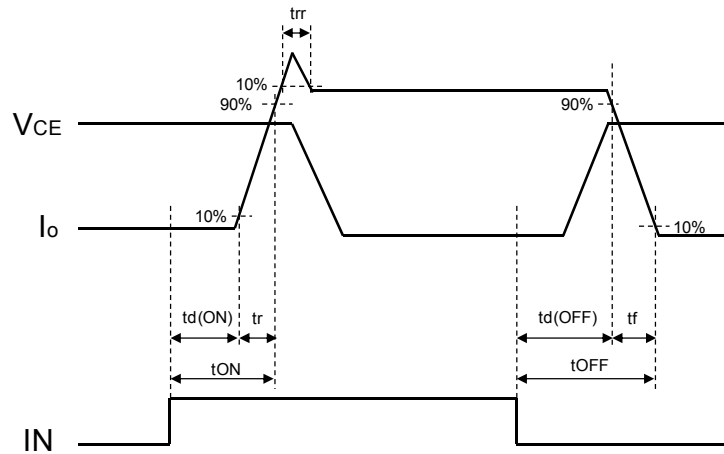


Figure 3. Switching time definition

Ex) Lower side U phase measurement

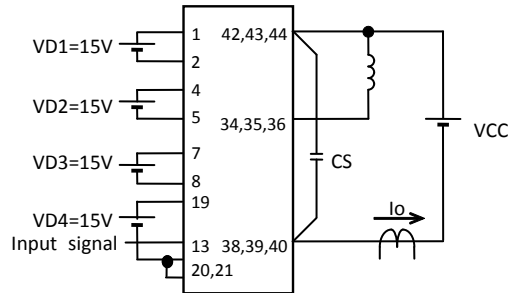


Figure 4. Evaluation circuit (Inductive load)

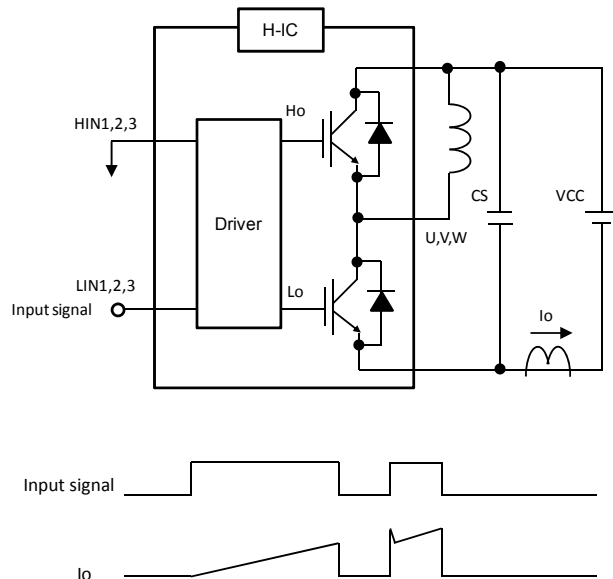


Figure 5. Switching loss circuit

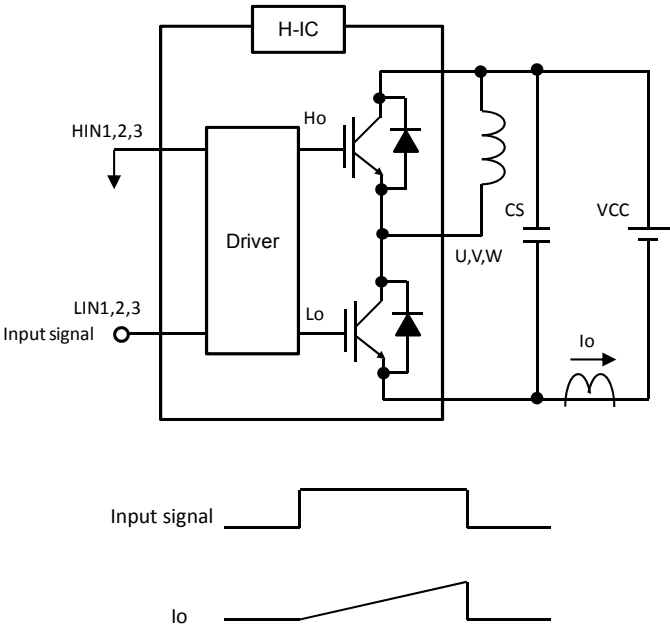


Figure 6. R.B.SOA circuit

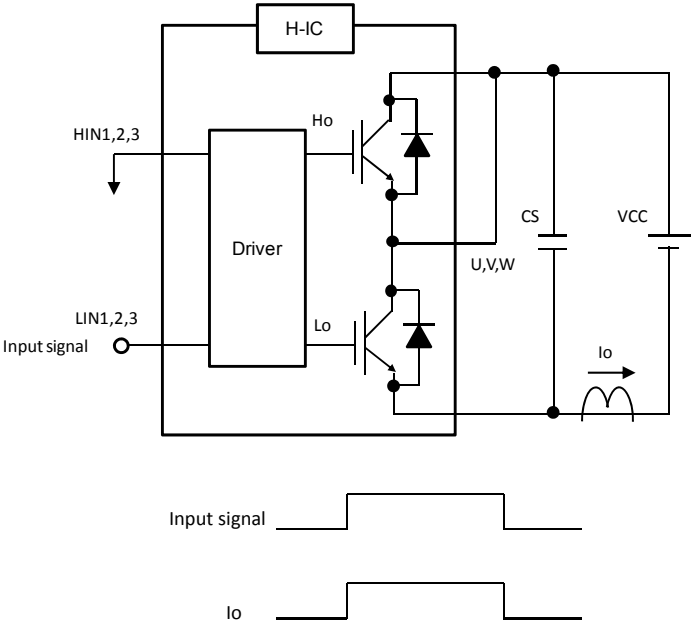


Figure 7. S.C.SOA circuit

## 3.2. Thermistor Characteristics

An integrated thermistor is used to sense the internal module temperature its electrical characteristic is outlined below.

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Resistance	R <sub>25</sub>	T <sub>c</sub> =25°C	97	100	103	kΩ
Resistance	R <sub>100</sub>	T <sub>c</sub> =100°C	4.93	5.38	5.88	kΩ
B-Constant(25-50°C)	B		4165	4250	4335	K
Temperature Range			-40		+125	°C

Table 2. NTC Thermistor value

R<sub>t</sub> is the value of the integrated NTC thermistor at T<sub>c</sub>=25°C. The resistance value is 100kΩ±3% and the value of the B-Constant (25-50°C) is 4250K±2%. The temperature depended value is calculated as shown in the formula.

$$R(t) = R_{25} \times e^{B \left( \frac{1}{T} - \frac{1}{298} \right)}$$

The resulting in the NTC values over temperatures

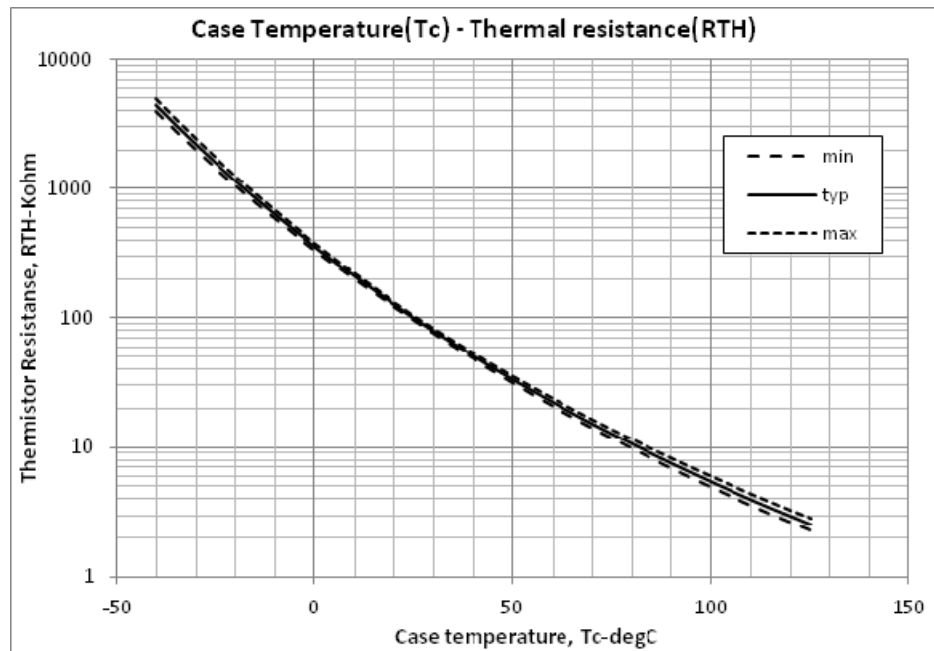


Figure 8. typical NTC value over temperature

## 4. Protective functions and Operation Sequence

This chapter describes the protection features.

- over current protection
- short circuit protection
- under Voltage Lockout (UVLO) protection
- cross conduction prevention

## 4.1. Over current protection

Over current protection is implemented by measuring the voltage across a shunt resistor to the negative supply terminal. In case of an OCP fault the gate drivers are shut down internally and the external Fault signal becomes active (low). The trip level of the over current protection current is programmable with an external resistance RSD between the ISD and VSS terminals as shown in over current protection Figure 9.

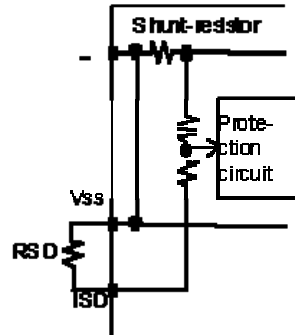


Figure 9. over current protection circuit

Once activated by a fault condition the FAULT signal output returns to inactive (and is pulled high by the external resistor) when the fault condition is over and the fault clear time (FLTCLR) has passed. This implies that the system microcontroller needs to disable all input signals to the module by driving them low upon detection of a fault condition.

The OCP trip level is programmed within the default or lower levels by an external resistor (RSD) between the ISD and VSD pins according to Figure 10. When the default level is used both terminals must be shorted e.g. by a 0Ω resistor.

Note 1: One should be aware that the “N” and the “VSS” pins are internally connected. Therefore an external short between these pins can cause the OCP level to be lower than desired.

Note 2: In order to prevent false OCP events due to switching noise and recovery current – a blanking time of some microseconds is implemented. This blanking time will also filter repetitive short high current pulses without tripping the OCP.

External Resistance (RSD) [kΩ]	Over Current Protection (ISD) [A]		
	min	typ	max
0	58.8	66.4	74.2
2	57.0	64.3	71.7
3.9	55.7	62.8	70.1
5.6	54.9	61.9	69.0
10	53.4	60.1	67.1
22	51.5	57.9	64.6
47	50.1	56.4	62.8
100	49.3	55.4	61.7
Open	48.4	54.4	60.6

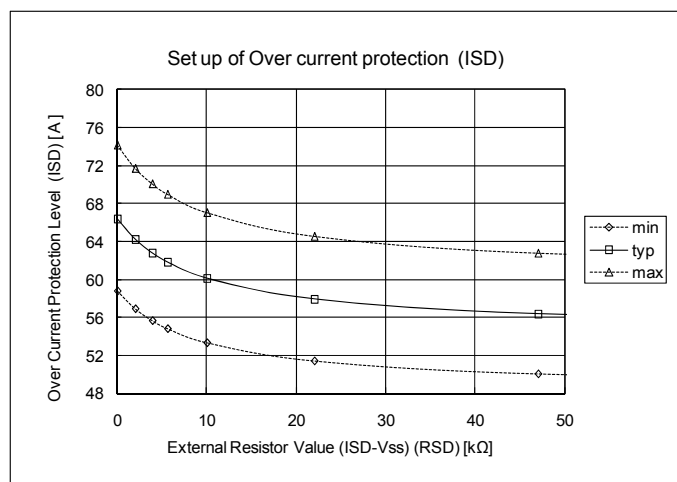


Figure 10. STK5F1U3E2D-E RSD values and resulting ISD curve

External Resistance (RSD) [kΩ]	Over Current Protection (ISD) [A]		
	min	typ	max
0	38.6	43.6	48.6
2	37.5	42.3	47.3
3.9	36.8	41.5	46.3
5.6	36.3	40.9	45.7
10	35.4	39.9	44.5
22	34.2	38.6	43.0
47	33.4	37.6	41.9
100	32.8	37.0	41.2
Open	32.3	36.3	40.4

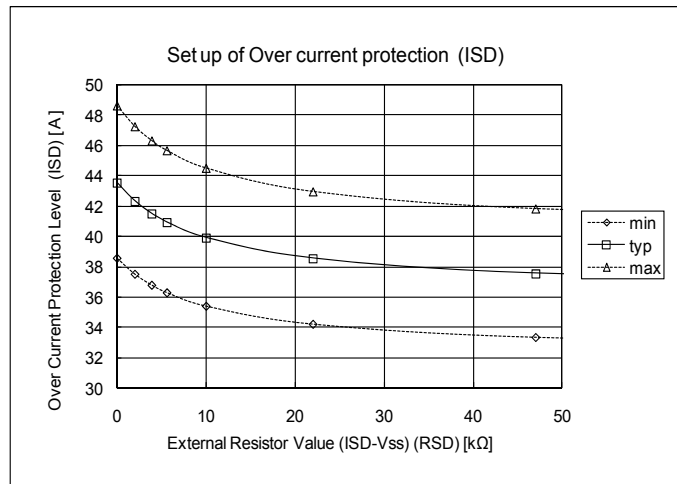


Figure 11. STK5F1U3C2A-E RSD values and resulting ISD curve

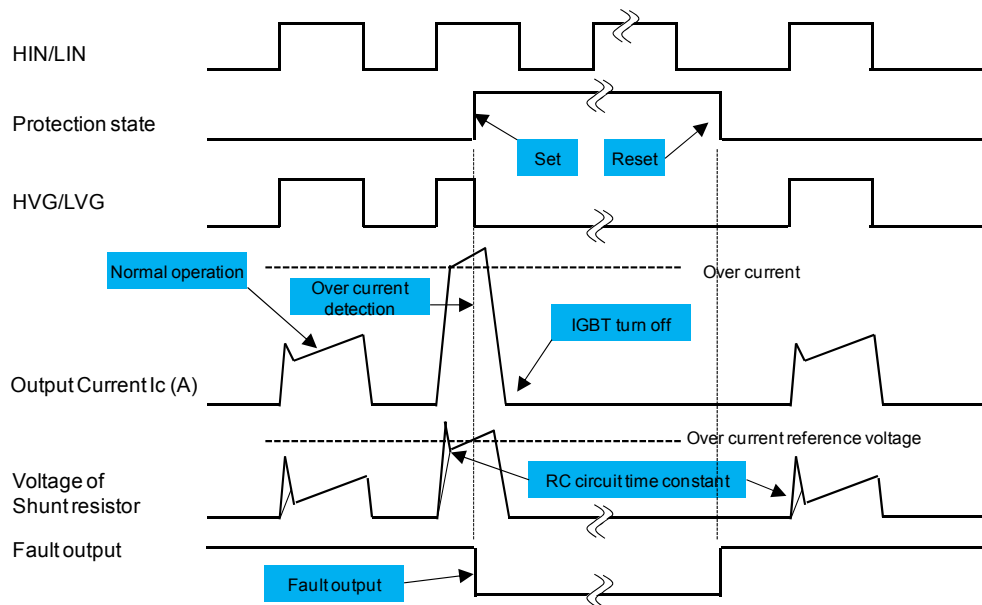


Figure 12. Over current protection Timing chart

## 4.2. Under Voltage Lockout Protection

The UVLO protection is designed to prevent unexpected operating behavior as described in Table 3. Both High-side and Low-side have UV protecting function. However the fault signal output only corresponds to the Low-side UVLO Protection. During the UVLO state the fault output is continuously driven (low).

VDD Voltage (typ. Value)	Operation behavior
< 12.5V	As the voltage is lower than the UVLO threshold the control circuit is not fully turned on. A perfect functionality cannot be guaranteed.
12.5 V – 13.5 V	IGBTs can work, however conduction and switching losses increase due to low voltage gate signal.
13.5 V – 16.5 V	Recommended conditions
16.5 V – 20.0 V	IGBTs can work. Switching speed is faster and saturation current higher, increasing short-circuit broken risk.
> 20.0 V	Control circuit is destroyed. Absolute max. rating is 20 V.

Table 3. Module operation according to control supply voltage

The sequence of events in case of a low side UVLO event (IGBTs turned off and active fault output) is shown in Figure 13. Figure 14 shows the same for a high side UVLO (IGBTs turned off and no fault output).

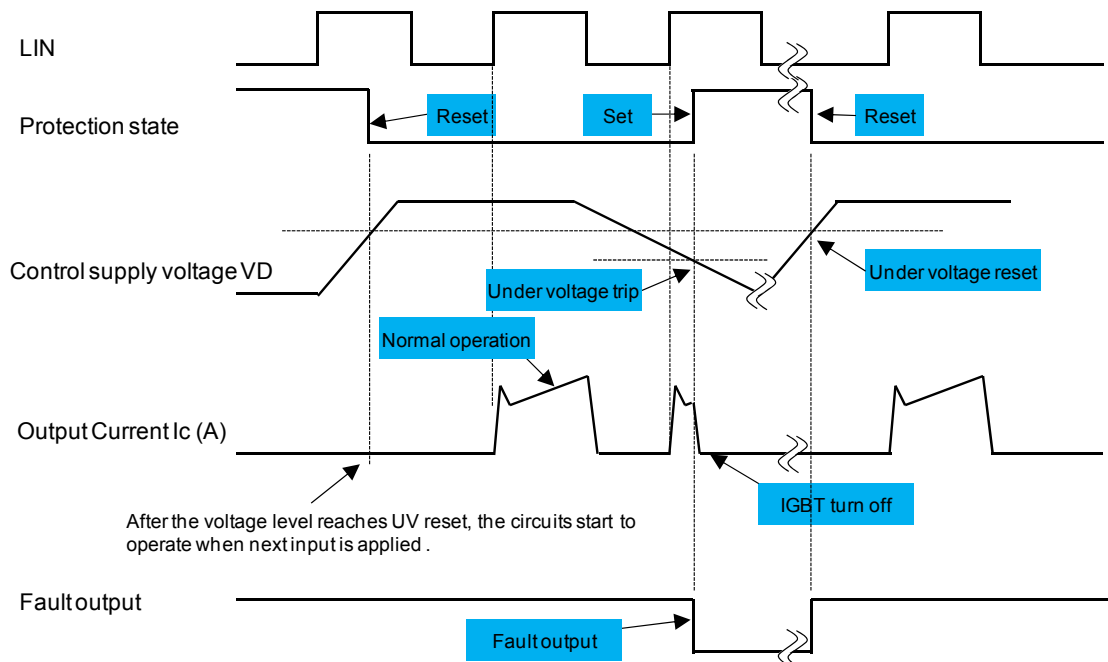


Figure 13. Low side UVLO timing chart

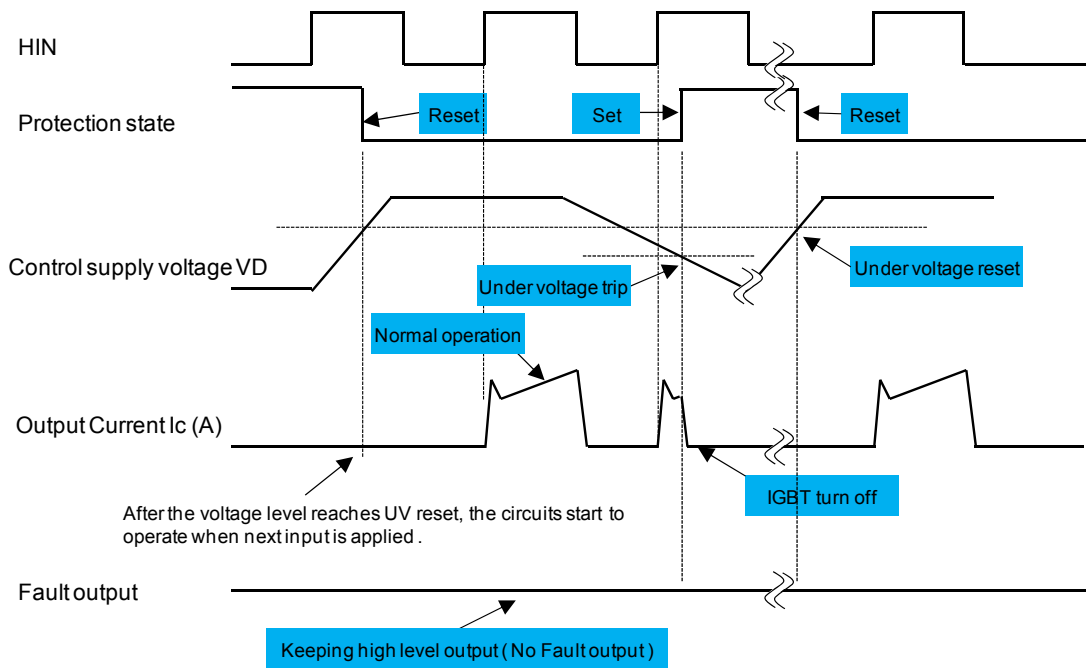


Figure 14. High side UVLO timing chart

## 4.3. Cross conduction prevention

The STK5F1U3xx series module implement a cross conduction prevention logic at the pre-driver to avoid simultaneous drive of the low- and high-side IGBTs as shown in Figure 15.

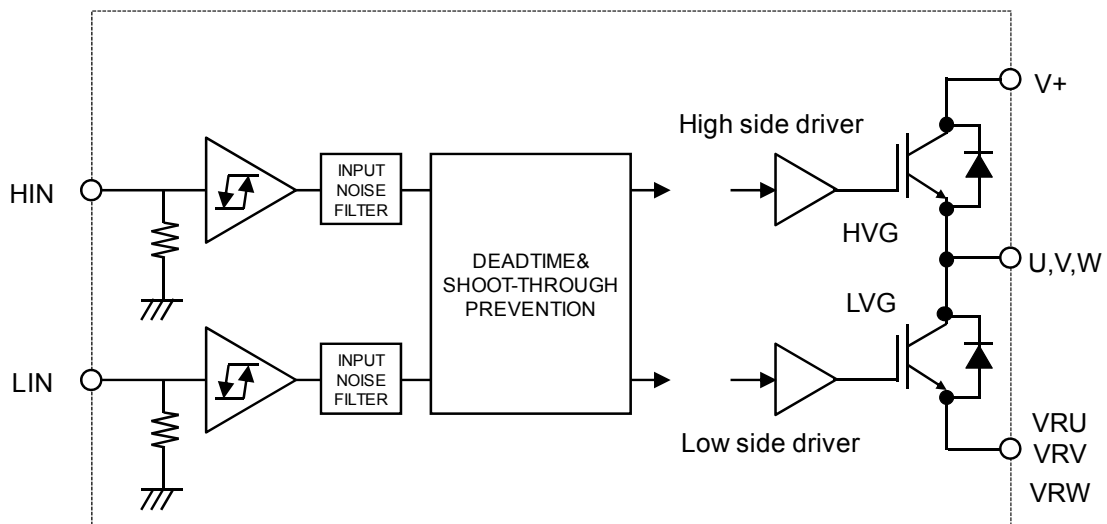


Figure 15. Cross Input Conduction Prevention

In case of both high and low side drive inputs are active (high) the logic prevents both gates from being driven – a corresponding timing diagram can be found in Figure 16 below.

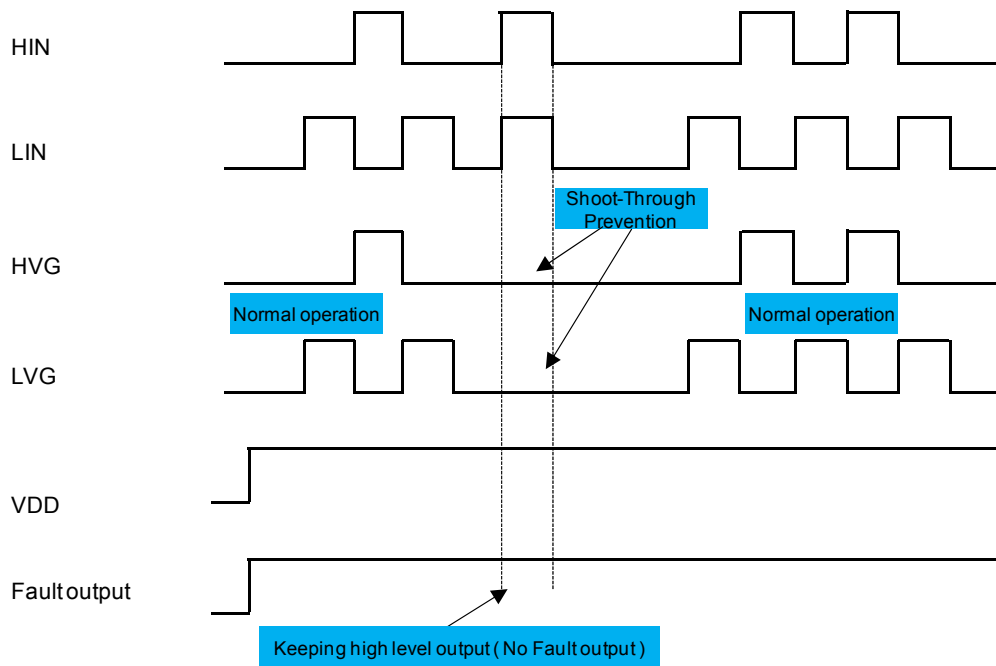


Figure 16. cross conduction prevention timing diagram

Even so cross conduction on the IGBTs due to incorrect external driving signals is prevented by the circuitry the driving signals (HIN and LIN) need to include a “dead time”. This period where both inputs are inactive between either one becoming active is required due to the internal delays within the IGBTs. Figure 17 shows the delay from the HIN-input via the internal HVG to high side IGBT, the similar path for the low side and the resulting minimum dead time which is equal to the potential shoot through period:

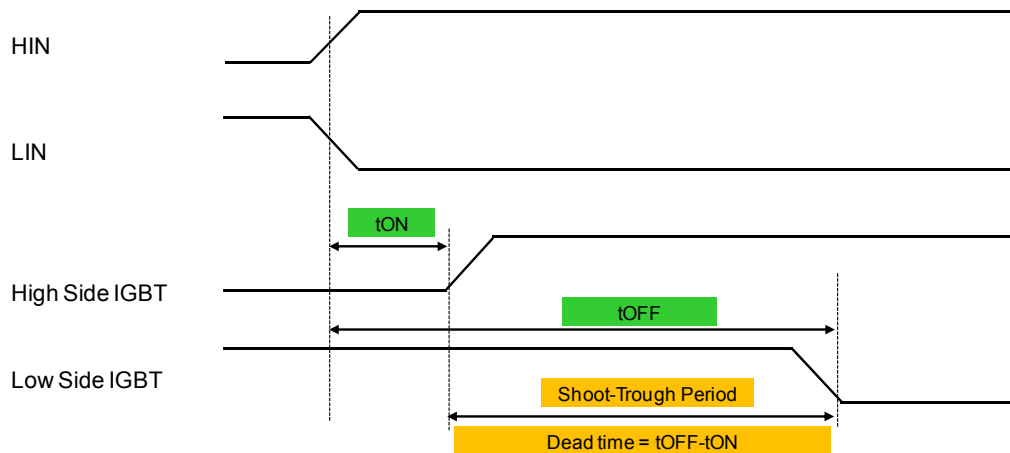


Figure 17. Shoot Trough Period

## 5. PCB design and mounting guidelines

This chapter provides guidelines for an optimized design and PCB layout as well as module mounting recommendations to appropriately handle and assemble the HIC module.

### 5.1. Application (schematic) design

The following two figures18 gives an overview of the external circuitry's functionality when designing with the STK5F1U3xx series module.

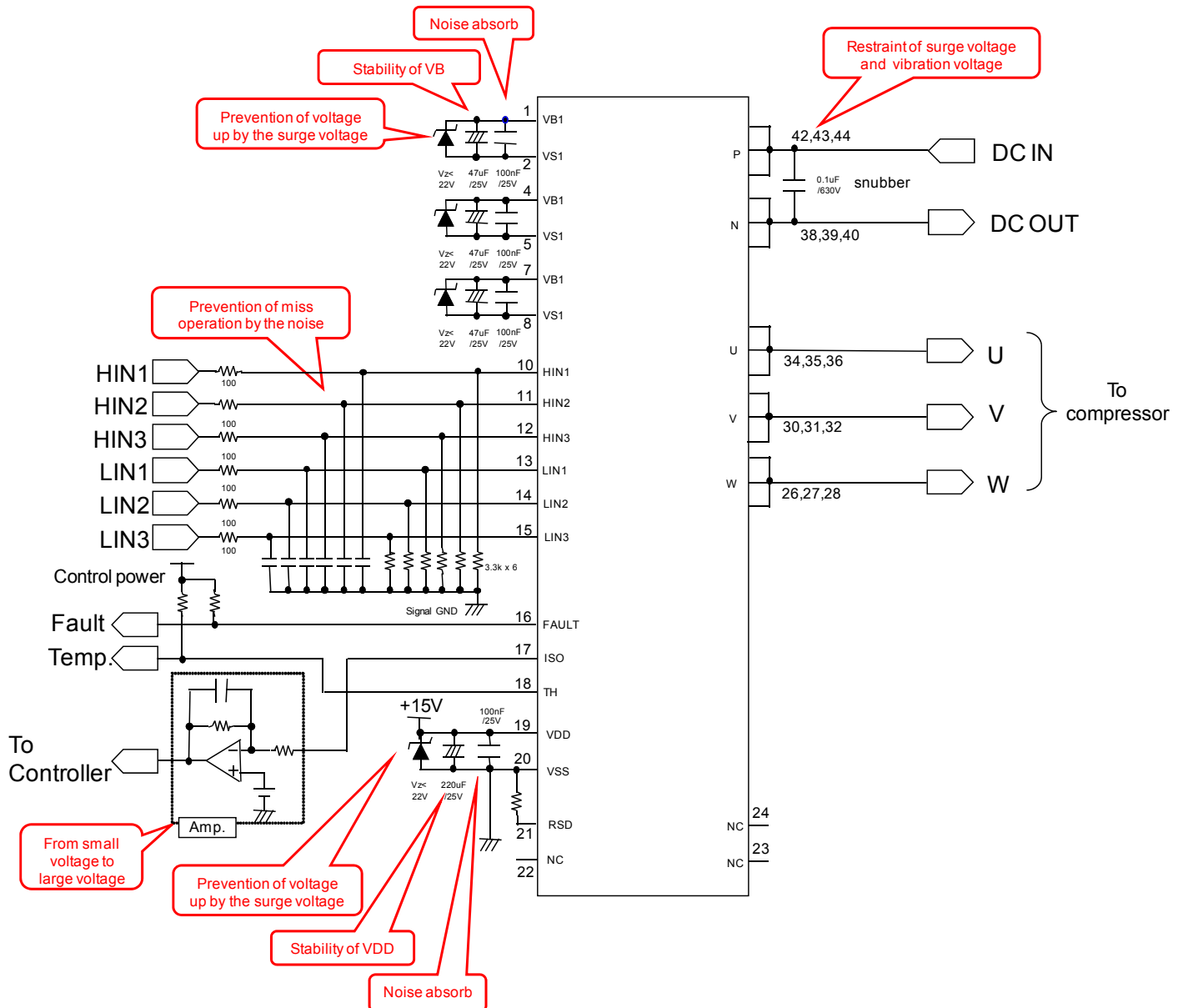


Figure 18. STK5F1U3xx series application circuit

## 5.2. Notes on PCB design

- (1) Snubber capacitor between the positive terminal and the negative terminal of the power, please place as close as possible to the hybrid IC.
- (2) Power side GND and control side GND must not be a solid common wiring. Signal side GND is recommended to design the patterns in one point of connection to Vss terminal so that it does not flow to the power side the GND signal current. The terminal Vss (control side GND) is connected to N terminal (power side GND) in the interior of the hybrid IC.
- (3) Capacitor and zener diode should be placed close to the terminal.
- (4) C-R filter should be placed close to the terminal.
- (5) Capacitor and zener diode should be placed close to the terminal.

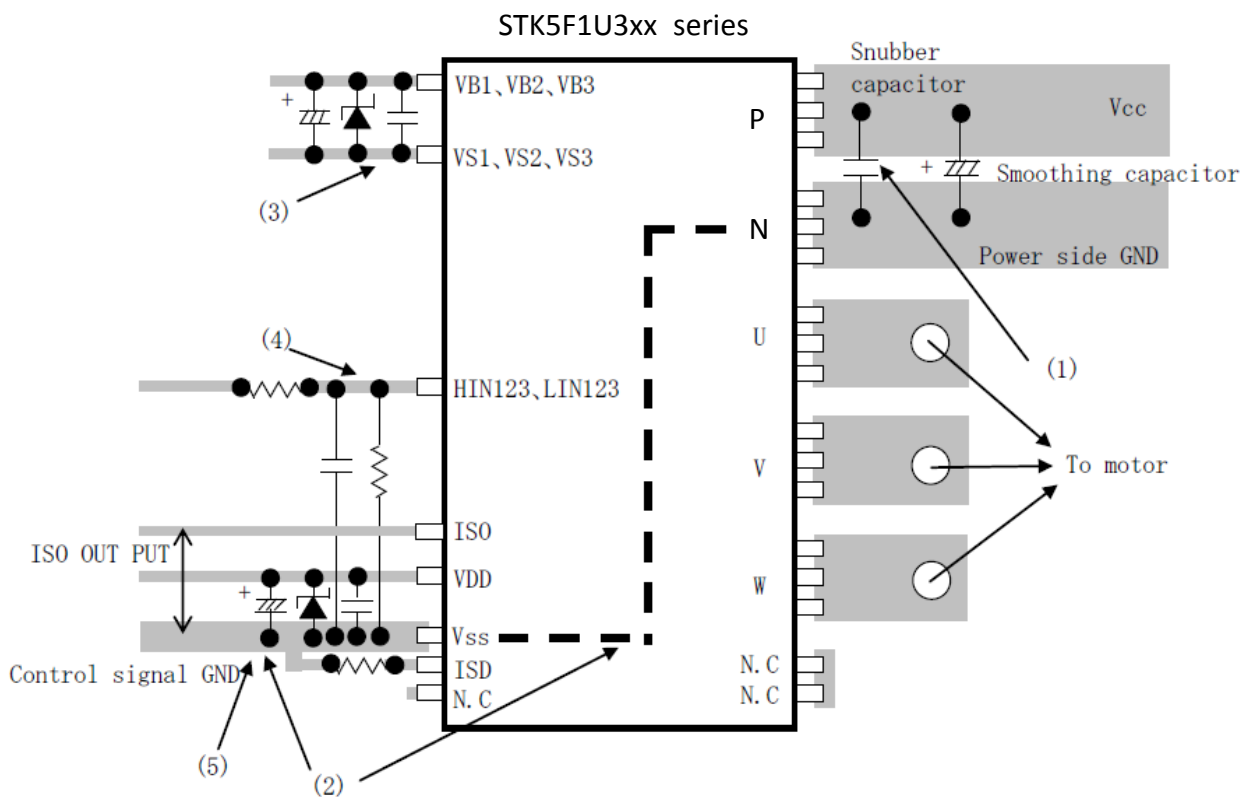


Figure 19. STK5F1U3xx series PCB design

## 5.3. Pin by pin design and usage notes

This section provides pin by pin PCB layout recommendations and usage notes. For a complete list of module pins refer to the datasheet or Chapter 6.

### P & N

These pins are connected with the main DC power supply. The applied voltage is up to the Vcc level. Overvoltage on these pins could be generated by voltage spikes during switching at the floating inductance of the wiring. To avoid this behavior the wire traces need to be as short as possible to reduce the floating inductance. In addition a snubber capacitor needs to be placed as close as possible to these pins to stabilize the voltage and absorb voltage surges.

### U, V, W

These terminals are the output pins for connecting the 3-phase motor. They share the same GND potential with each of the high side control power supplies. Therefore they are also used to connect the GND of the of the bootstrap capacitors. These bootstrap capacitors should be placed as close to the module as possible.

### VDD, VSS

These pins connect with the circuitry of the internal protection and pre-drivers for the low -side power elements and also with the control power supply of the logic circuitry. Voltage to input these terminals is monitored by the under voltage protection circuit. The VSS terminal is the reference voltage for the control inputs signals as well as Fault and ISO. VSS is connected with the “N” terminal internally. The main circuit does typically not draw current from VSS.

When the “N” and “VSS” pins are connected externally care must be taken to select a single connection point as close as possible to the IC. In case of multiple connections to these pins and longer traces being used, the overcurrent protection level may become low. Therefor this should be avoided.

### VB1, VB2, VB3

The VBx pins are internally connected to the positive supply of the high-side drivers. The supply needs to be floating and electrically isolated. The boot-strap circuit shown in Figure 20 forms this power supply individually for every phase. Due to integrated boot resistor and diode (RB & DB) only an external boot capacitor (CB) is required. There are two current path to charge CB – depicted as ① and ②.

① when the low side power IGBT is ON

② when motor current is flows in CB

The capacitor is discharged while the high-side driver is activated.

Thus CB needs to be selected taking the maximum on time of the high side and the switching frequency into account.

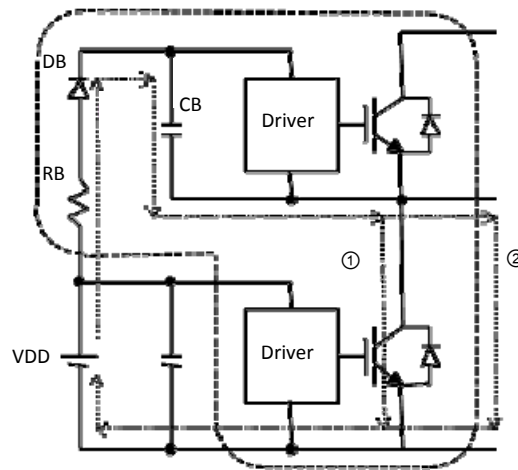


Figure 20. Boot Strap Circuit

To set an initial charge on CB a high ohmic resistor can be used between the motor and the “N” pins – considering the max voltage rating of the device.

The voltages on the high side drivers are individually monitored by the under voltage protection circuit. In case an UVP event is detected on a phase its operation is stopped.

Typically a CB value of less or equal 47uF ( $\pm 20\%$ ) is used. In case the CB value needs to be higher an external resistor (of apx. 20 $\Omega$  or less) should be used in series with the capacitor to avoid high currents which can cause malfunction of the hybrid IC.

### **HIN1, LIN1, HIN2, LIN2, HIN3, LIN3**

These pins are the control inputs for the power stages. The inputs on HIN1/HIN2/HIN3 control the high-side transistors of U/V/W, and the inputs on LIN1/LIN2/LIN3 control the low-side transistors of U/V/W respectively. The input are active high and the input thresholds  $V_{IH}$  and  $V_{IL}$  are 5V compatible to allow direct control with a microcontroller system

Simultaneous activation of both low and high side is prevented internally to avoid shoot through at the power stage. However, due to IGBT switching delays the control signals must include a dead-time.

The equivalent input stage circuit is shown in Figure 21.

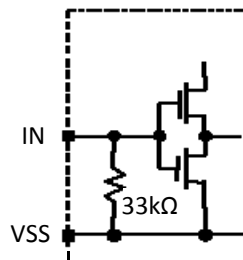


Figure 21. Internal Input Circuit

For fail safe operation the control inputs are internally tied to VSS via a 33k $\Omega$  (typ) resistor. To avoid switching captured by external wiring to influence the module behavior an additional external low-ohmic pull-down resistor with a value of 2.2k $\Omega$ -3.3k $\Omega$  should be used.

The output might not respond when the width of the input pulse is less than 1 $\mu$ s (both ON and OFF).

### **Fault**

The Fault pin is an active low input and open-drain output. It is used to indicate an internal fault condition of the module and also can be used to disable the module operation. The I/O structure is shown in Figure 22.

The internal sink current  $I_{oSD}$  during an active fault is nominal 2mA @ 0.1V. Depending on the interface supply voltage the external pull-up resistor ( $R_P$ ) needs to be selected to set the low voltage below the  $V_{IL}$  trip level.

*For the commonly used supplies  $V_P$ :*

$V_P = 15V \rightarrow R_P \geq 20k\Omega$

$V_P = 5V \rightarrow R_P \geq 6.8k\Omega$

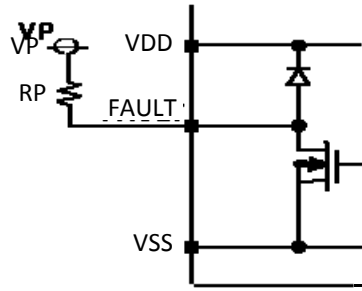


Figure 22. Fault Connection

For a detailed description of the fault operation refer to Chapter 4.

Note: The Fault signal does not latch permanently. The modules operation is automatically re-started after the causing protection event end and after the minimum of the fault timeout(18ms). Therefore the input needs to be driven low externally activated as soon as a fault is detected.

## ISO

The ISO pin allows monitoring the output voltage of the integrated current sense amplifier. This pin is usually left unconnected. Any external circuitry needs to have an impedance higher than 5.6kΩ.

Note: In case this pin is shorted to VSS – current sensing will not function.

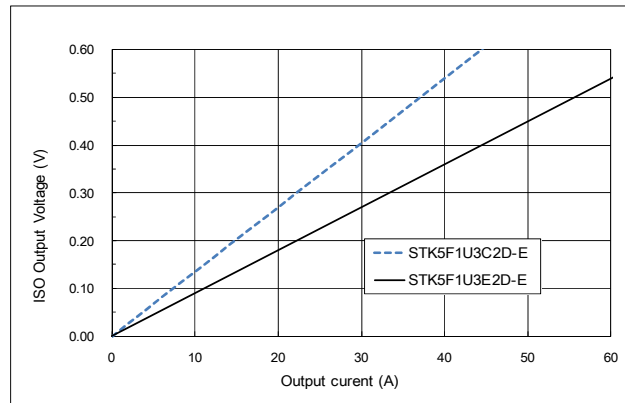


Figure 23. The output current ( $I_o$ ) vs ISO characteristics

## TH

An internal thermistor to sense the substrate temperature is connected between VSS and the TH pins. In conjunction with an external pull-up resistor  $R_{th}$  a module temperature monitor can be build.

Note: with this mimic only the substrate temperature can be monitored.

## RCIN

This pin is used to the set the fault clear time. It is recommended to leave this pin open to select the default fault clear time of 18 ms.

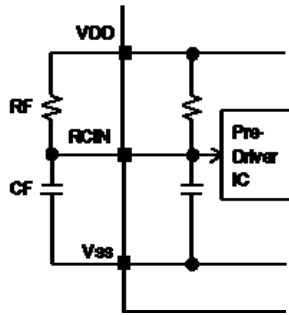


Figure 24. RCIN Circuit

To shorten the fault clear time connect an external resistor  $R_F$  between VDD and RCIN.  
To extend the fault clear time) connect an external capacitor  $C_F$  between RCIN and VSS.

### 5.4. Heat sink mounting and torque

If a heat sink is used, insufficiently secure or inappropriate mounting can lead to a failure of the heat sink to dissipate heat adequately. This can lead to an inability of the device to provide its inherent performance, a serious reduction in reliability, or even destruction, burst and burn of the device due to overheating.

The following general points should be observed when mounting H-IC on a heat sink:

1. Verify the following points related to the heat sink:
  - There must be no burrs on aluminum or copper heat sinks.
  - Screw holes must be countersunk.
  - There must be no unevenness in the heat sink surface that contacts H-IC.
  - There must be no contamination on the heat sink surface that contacts H-IC.
2. Highly thermal conductive silicone grease needs to be applied to the whole back (aluminum substrate side) uniformly, and mount H-IC on a heat sink. Upon re-mounting apply silicone grease(100um to 200um) again uniformly.
3. For an intimate contact between the H-IC and the heat sink, the mounting screws should be tightened gradually and sequentially while a left/right balance in pressure is maintained. Either a bind head screw or a truss head screw is recommended. Please do not use tapping screw. We recommend using a flat washer in order to prevent slack. The standard heat sink mounting condition of an STK5F1U3xx series is as follows.

Item	Recommended Condition
Pitch	$68.0 \pm 0.1\text{mm}$ (Please refer to Package Outline Diagram)
Screw	diameter : M4 Bind machine screw, Truss machine screw, Pan machine screw
Washer	Plane washer The size is D:9mm, d:4.8mm and t:0.8mm (Fig.2) JIS B 1256
Heat sink	Material : copper or Aluminum Warpage (the surface that contacts H-IC) : -50 to 100 $\mu\text{m}$ Screw holes must be countersunk. No contamination on the heat sink surface that contacts H-IC.
Torque	Final tightening : 0.79 to 1.17Nm Temporary tightening : 20 to 30 % of final tightening
Grease	Silicon grease Thickness : 100 to 200 $\mu\text{m}$ Uniformly apply silicon grease to whole back. (Fig.3)

Table 4. heat sink mounting

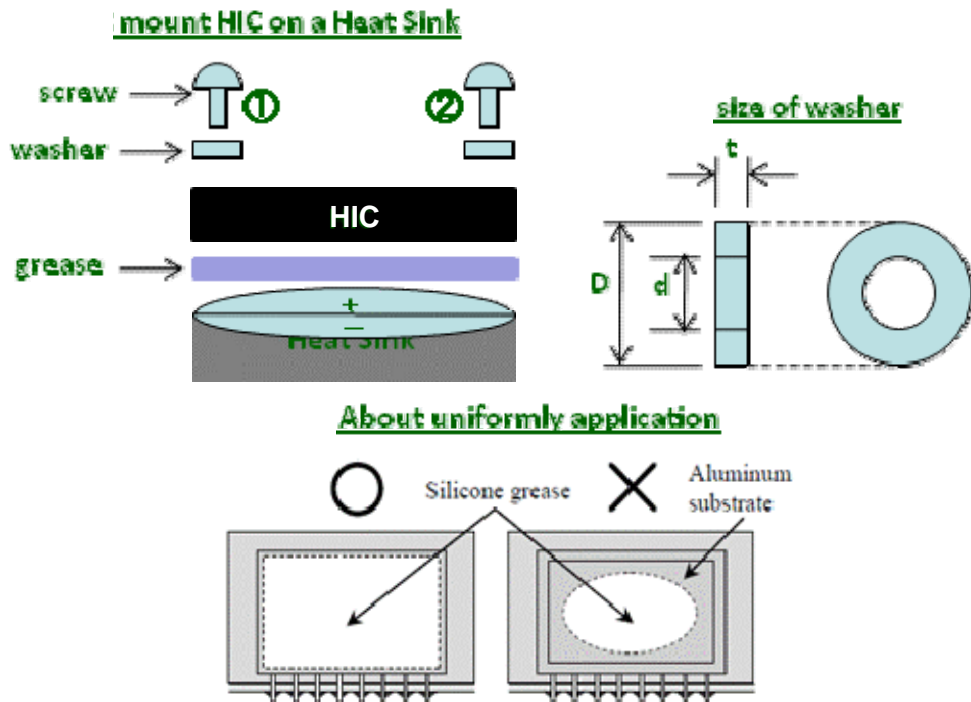


Figure 25. Mount on Heat Sink

steps to mount an HIC on a heat sink

1st: Temporarily tighten maintaining a left/right balance.

2nd : Finally tighten maintaining a left/right balance.

### 5.5. Mounting and PCB considerations (general information)

In designs in which the printed circuit board and the heat sink are mounted to the chassis independently, use a mechanical design which avoids a gap between H-IC and the heat sink, or which avoids stress to the lead frame of H-IC by an assembly that a moving H-IC is forcibly fixed to the heat sink with a screw.

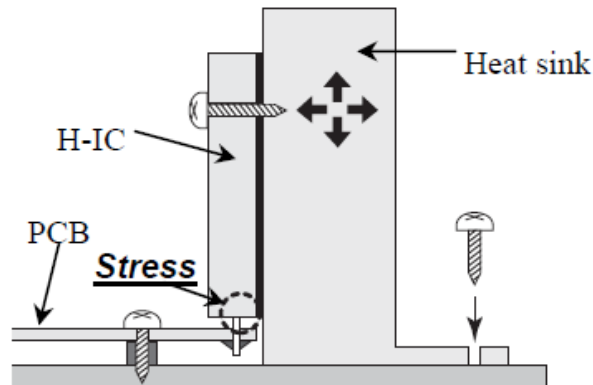


Figure 26. Fix to Heat Sink

Do not mount H-IC with a tilted orientation. This can result in stress being applied to the lead frame and H-IC substrate could short out tracks on the printed circuit board. Always mount the H-IC vertically. If stress is given by compulsory correction of a lead frame after the mounting, a lead frame may drop out. Be careful of this point.

When designing the PCB layout take care that the bent part portion of the lead frame pins does not short-circuit to VIA holes or tracks on the PCB.

Since the use of sockets to mount H-IC can result in poor contact with H-IC leads, we strongly recommend making direct connections to PCB.

H-IC modules are flame retardant. However, under certain conditions, it may burn, and poisonous gas may be generated or it may explode. Therefore, the mounting structure of the H-IC module should also be flame retardant.

#### Mounting on a Printed Circuit Board

1. Align the lead frame with the holes in the printed circuit board and do not use excessive force when inserting the pins into the printed circuit board. To avoid bending the lead frames, do not try to force pins into the printed circuit board unreasonably.
2. Do not insert H-IC into printed circuit board with an incorrect orientation, i.e. be sure to prevent reverse insertion. H-IC may be destroyed, exploded, burned or suffer a reduction in their operating lifetime by this mistake.
3. Do not bend the lead frame.

### 5.6. Cleaning

H-IC has a structure that is unable to withstand cleaning. As a basic policy, do not clean independent H-IC or printed circuit boards on which an H-IC is mounted.

## 6. Package Outline

STK5F1U3xx series is DIP4 package. (Dual-line-package)

### 6.1. Package outline and dimension

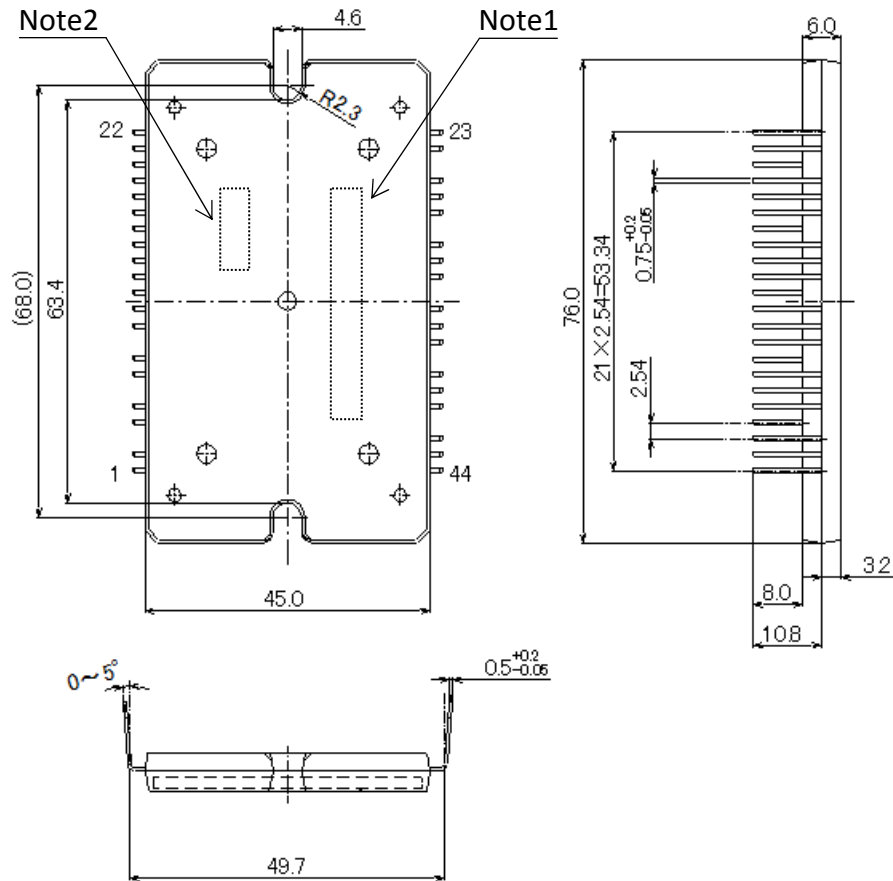


Figure 27. STK5F1U3xx series Package Outline

### 6.2. Laser Marking

- Note 1: The labeling designates the model number – centered within a field of 4.5 mm width and 35 mm length
- Note2: The labeling designates the order number – right justified within a field of 3.5 mm width and 14 mm length

\*We examine the design except for the above.

**6.3. Pin Out Description**

Pin No.	Name	Description	Pin No.	Name	Description
1	VB1	High side floating supply voltage 1	44	P	Positive bus input voltage
2	VS1	High side floating supply offset voltage	43	P	Positive bus input voltage
3	-	Without pin	42	P	Positive bus input voltage
4	VB2	High side floating supply voltage 2	41	-	Without pin
5	VS2	High side floating supply offset voltage	40	N	Negative bus input voltage
6	-	Without pin	39	N	Negative bus input voltage
7	VB3	High side floating supply voltage 3	38	N	Negative bus input voltage
8	VS3	High side floating supply offset voltage	37	-	Without pin
9	-	Without pin	36	U	U-phase output
10	HIN1	Logic input high side driver-Phase1	35	U	U-phase output
11	HIN2	Logic input high side driver-Phase2	34	U	U-phase output
12	HIN3	Logic input high side driver-Phase3	33	-	Without pin
13	LIN1	Logic input low side driver-Phase1	32	V	V-phase output
14	LIN2	Logic input low side driver-Phase2	31	V	V-phase output
15	LIN3	Logic input low side driver-Phase3	30	V	V-phase output
16	FAULT	Fault out (open drain)	29	-	Without pin
17	ISO	Current monitor pin	28	W	W-phase output
18	TH	Thermistor out	27	W	W-phase output
19	VDD	+15V main supply	26	W	W-phase output
20	VSS	Negative main supply	25	-	Without pin
21	ISD	Over-current protection level setting pin	24	NC	-
22	NC	-	23	NC	-

## 7. Demo Board

The demo board consists of the minimum required components such as snubber capacitor and bootstrap circuit elements of STK5F1U3xx series.

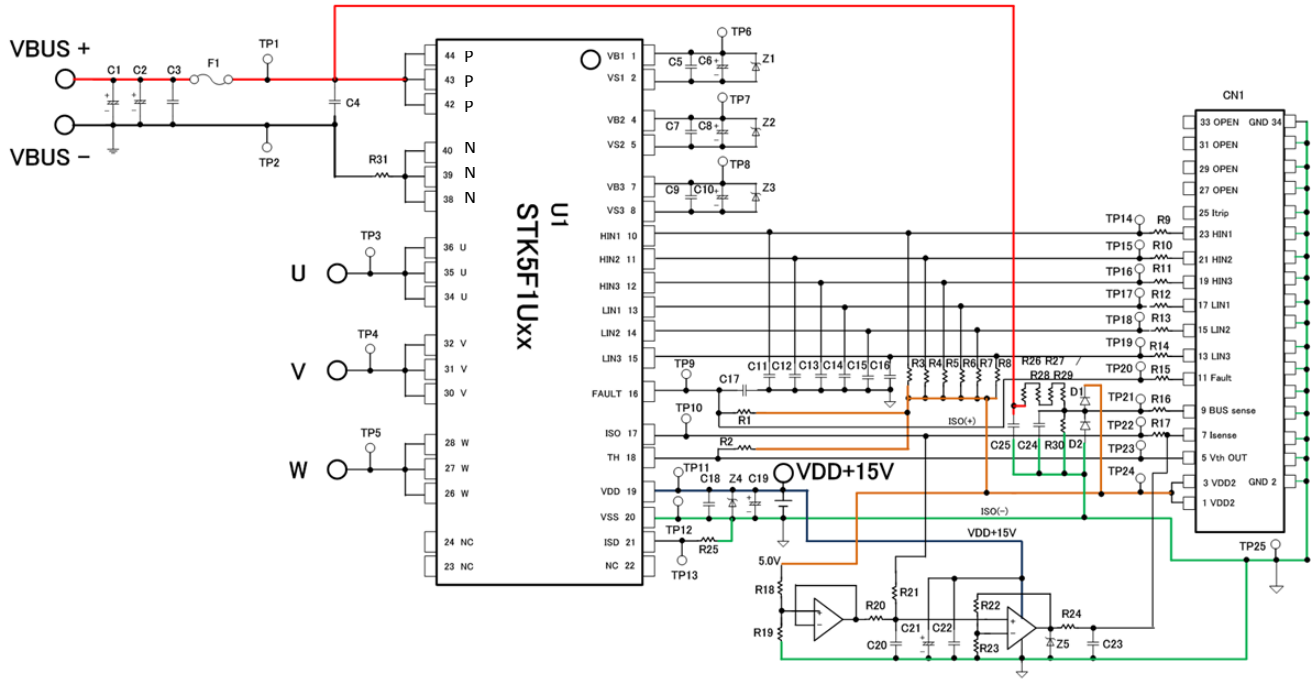
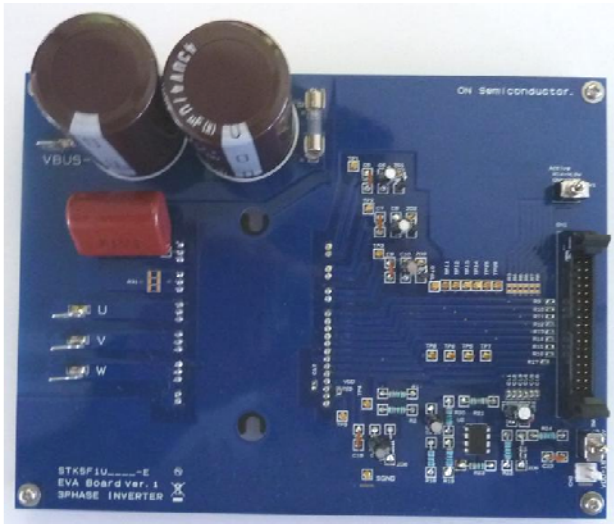
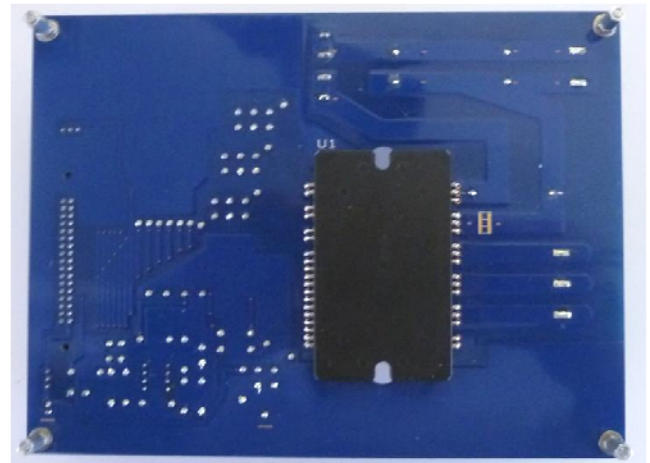


Figure 28. evaluation board schematic



Top view

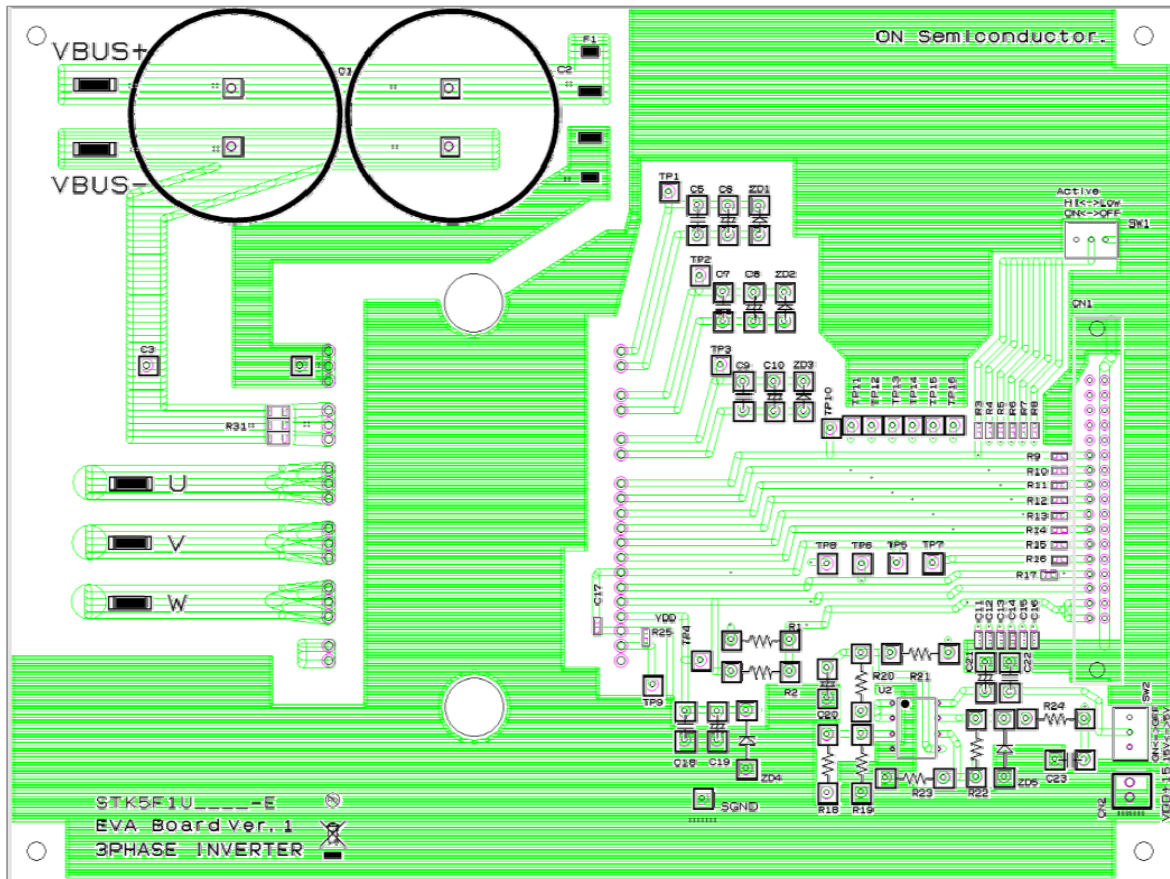


Bottom view

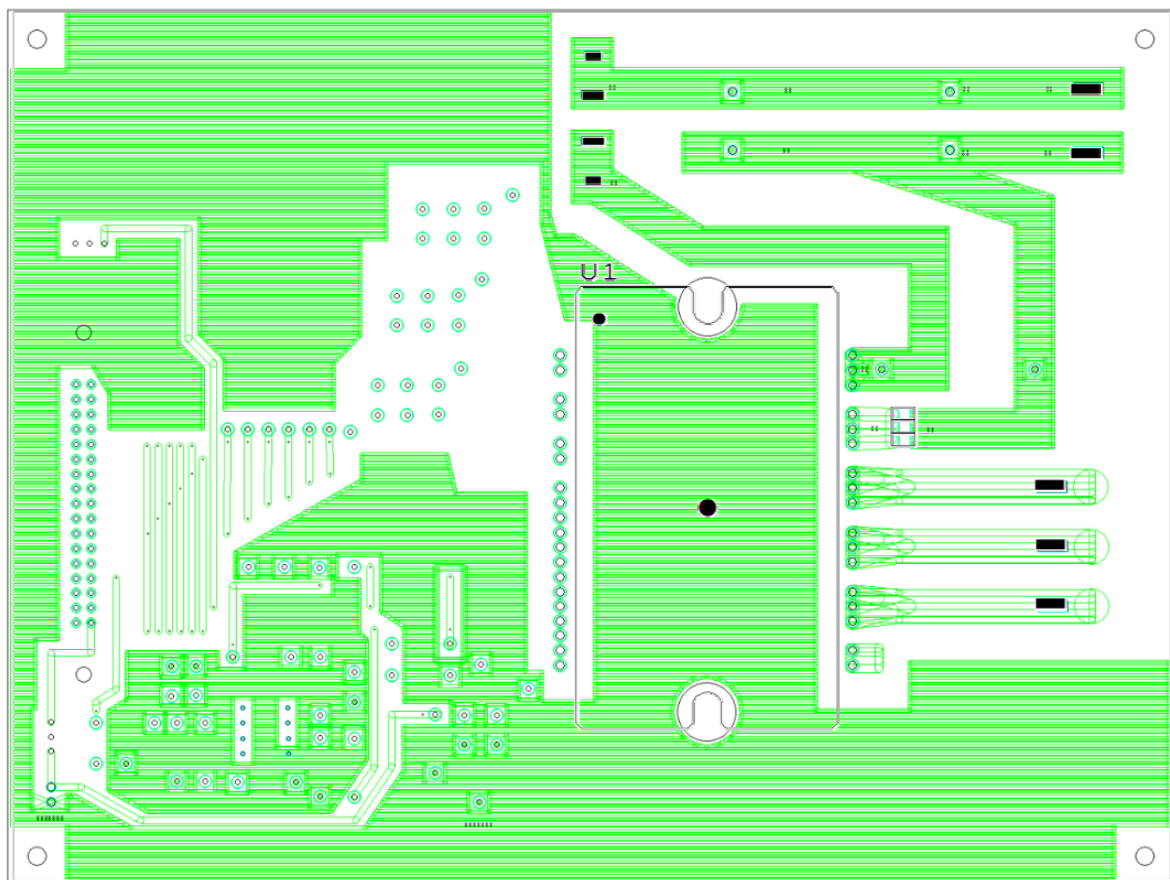
PCB dimension	: 200 x 150 x 1.5 t (mm)
Material	: FR-4, Dabble layer
Cu thickness	: 70um

Figure 29. evaluation board picture

# STK5F1U3xx series Application Note



Top view



Bottom view

Figure 30. evaluation board PCB layout

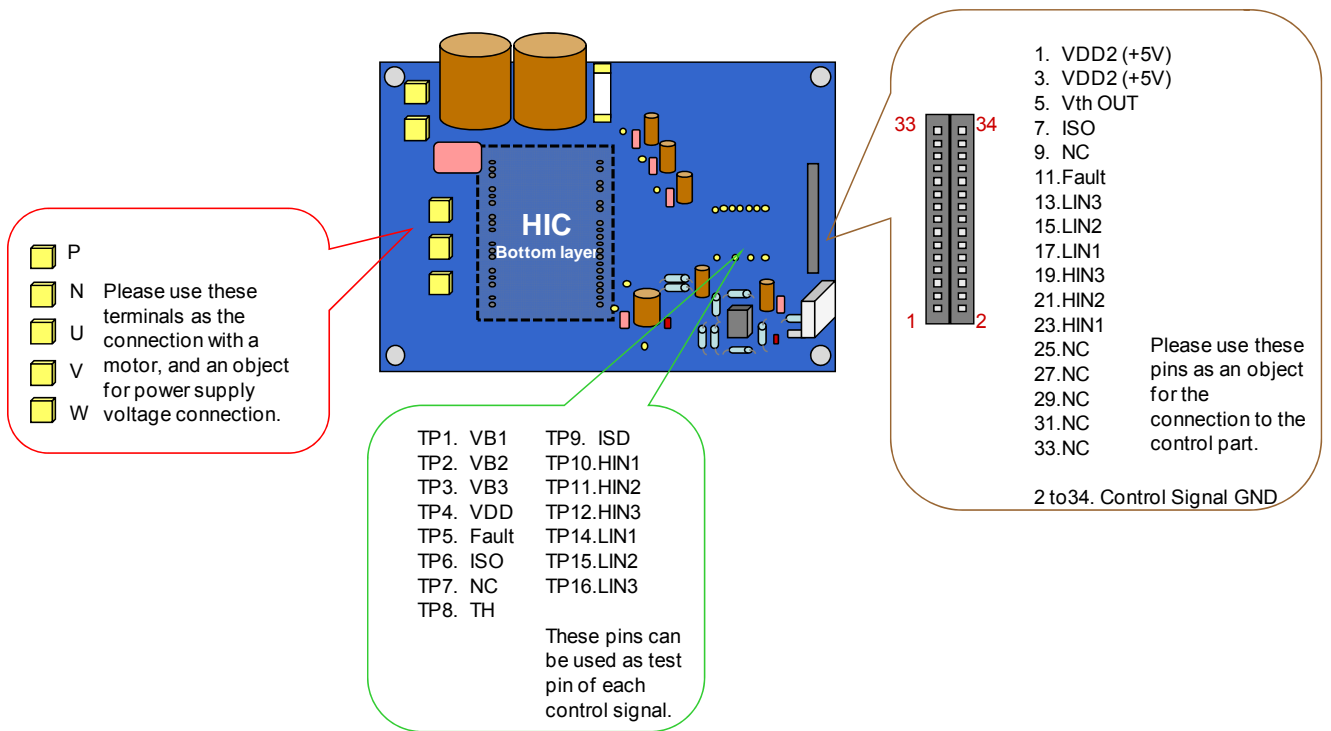
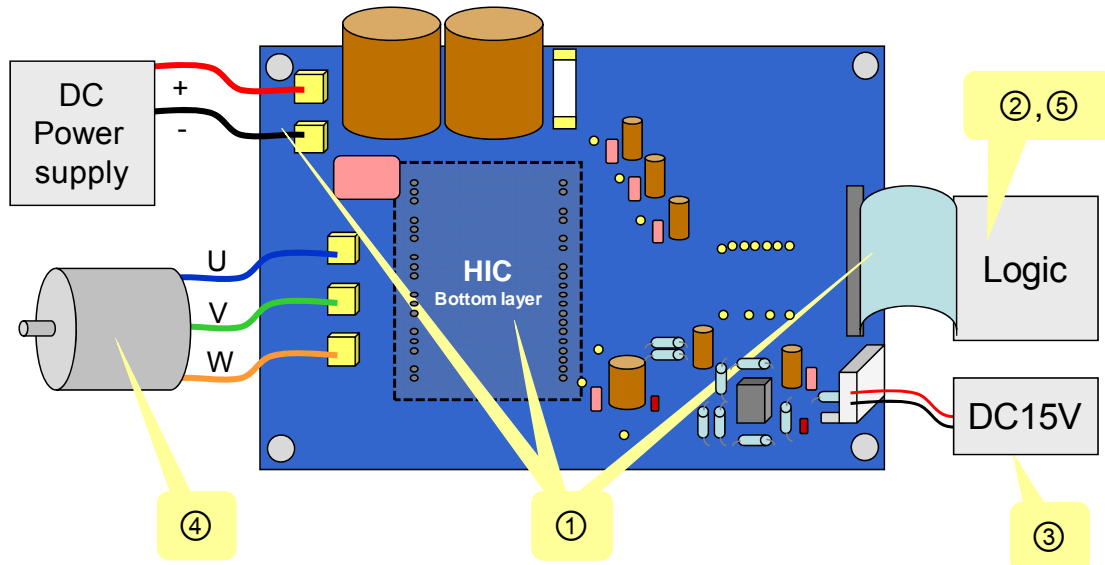


Figure 31. evaluation board connectors



- ①: HIC, each power supply, the logic parts, and the motor are connected to an evaluation board. Please confirm that each power supply is OFF at this time.
- ②: Please stand by for operation of the logic parts.
- ③: The power supply of DC 15V is switched on.
- ④: Please perform a voltage setup according to specifications, and switch on the power supply between the P and the N terminal.
- ⑤: Control of HIC is started from the logic parts.  
(Boot strap circuit has included in STK 5FxU3xx-E. So before running please set electric charge to upper side of boot strap capacitor to turn on Lower side of IGBT.)

※ When you turn off a power supply, please turn OFF the switch of a power supply part and a logic part in a reverse order from ④.

Figure 32. evaluation board instructions

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