AND9073/D

Through-hole Package Lead Resistance

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APPLICATION NOTE

INTRODUCTION

Power applications commonly require thoughtful consideration of thermal implications by the system design engineer. Power components, such as MOSFETs and diodes, are often used in packages that allow them to be mounted to specialized heat sinks. In many applications, this is the only way such components may be kept within their thermal ratings while in operation. The most common mounting for heat sinks is perpendicular to a printed circuit board (PCB), because power components and heat sinks then occupy a minimum of board space. To keep cost down, manufacturers regularly choose single−sided printed circuit boards, and use a wave soldering process to attach components. To address these thermal and cost concerns, power packages with leads extending far from a plastic−encased body are still in heavy use, and will continue to be for the foreseeable future. These through−hole packages include TO−220AB, TO−220FP, and IPAK (TO−251).

For most traditional devices, the electrical resistance of these packages has not been a concern. The resistance of the semiconductor component inside the package has been much more significant than the resistance of the package itself. With the introduction of MOSFETs below 10 mΩ, however, the situation has changed. For these devices, the package itself contributes a significant portion of the total resistance. Semiconductor device manufacturers can work to minimize added resistance inside the package, but the designer must consider the implications of his/her choices as well. Longer leads between package body and PCB result in more resistance in the current path, causing additional power dissipation when the device is in use. The purpose of this paper is to quantify the additional resistance for various packages, so the designer may choose how to mount such products and understand the impact to on−state resistance.

Procedure

As with most common materials, the copper leads on through−hole power packages have increasing resistance with temperature. To assess package resistance at room temperature, care was taken to ensure that the forcing current was low enough to not significantly raise the temperature of the leads being measured. To keep the change in temperature low, measurements were made at 100 mA, resulting in measured voltages of hundreds of micro−volts. Voltages were measured using an Agilent 34401 digital multimeter, set to 6 digit resolution.

Probe needles connected to micrometer probe holders were used to ensure measurement at precise points for reproducible results. This method also guaranteed consistent low contact resistance.

To avoid the influence of silicon power dissipation heating the leads, and enable measuring the lowest voltage drop possible, specially−built units were measured with a wire shorting the source post to the flag in each package.

Since the current in a power MOSFET flows between source (S) and drain (D) terminals, the complete path was measured with the assumption that the device would be mounted with equal drain and source lead lengths, as indicated in Figure 1. The reported additional resistance values represent the current path through both leads.

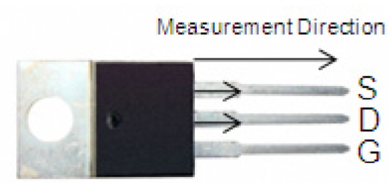

Figure 1. Pin configuration of a typical power MOSFET (G = Gate, S = Source, D = Drain) and measurement approach of the lead resistance.

TO−220AB Results

Figure 2 shows the resulting relationship between distance from package body and measured additional resistance due to the leads. The plot starts at zero since the point where the leads come out of the package is the reference point. Lead position shown in Figure 2 indicates the position from the package body along both drain and source leads. There is an inflection at about 3.5 mm due to the narrowing of the leads. On the narrower portion of the leads, there is an addition of ~0.13 Ω/m resistance. Up to the inflection point, the resistance is approximately 0.08 Ω/m. With a typical mounting of this package on a PCB, the

shoulder length extends between PCB and package body, causing about 0.3 mΩ additional resistance. For a device such as NTP5860NL, with a typical resistance of 2.6 mΩ (at 10 V Vgs and 30 A Id), the leads contribute more than 10%.

TO−220FP Results

Figure 3 shows the resulting relationship between distance from package body and measured additional resistance due to the leads. There is an inflection at about 2 mm due to the narrowing of the leads. On the narrower portion of the leads, there is an addition of ~0.14 Ω/m resistance. Up to the inflection point, the resistance is approximately 0.07 Ω/m.

IPAK Results

Figure 4 shows the resulting relationship between distance from package body and measured additional resistance due to the leads. There is only a slight inflection after 2 mm due to the narrowing of the leads. Closest to the package body, the resistance is approximately 0.08 Ω/m. Farther away, it is about 0.10 Ω/m.

Conclusions

The lead resistance of several through−hole packages was measured and reported to assist customers in deciding how much lead length to leave between PCB and package body. It has been shown that a typical mounting can result in greater than 10% of the total resistance due to the leads. For power MOSFETs with ON−resistance less than 10 mΩ, ON Semiconductor reports datasheet values without the added lead resistance, and the appropriate value from the charts in this application note must be added.

Table 1. LEAD RESISTANCE PER UNIT LENGTH FOR SEVERAL THROUGH−HOLE PACKAGES

Package	Resistance before inflection (Ω/m)	Inflection point (mm)	Resistance after inflection (Ω/m)
IPAK	0.08	2.0	0.10
TO−220AB	0.08	3.5	0.13
TO−220FP	0.07	2.0	0.14

Figure 2. Added Lead Resistance for TO−220AB (mΩ)

Figure 3. Added Lead Resistance for TO−220FP (mΩ)

Figure 4. Added Lead Resistance for IPAK (mΩ)

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