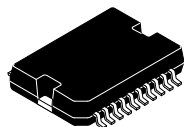


MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®

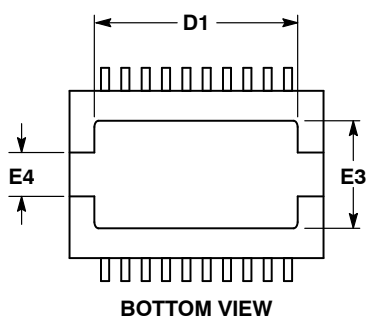
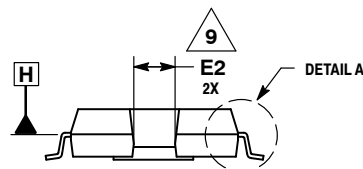
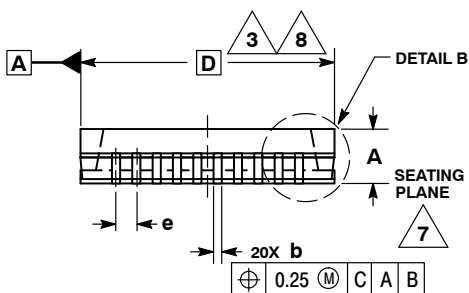
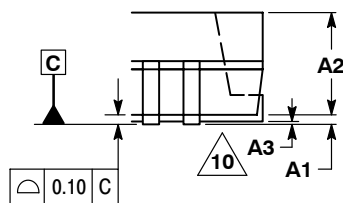
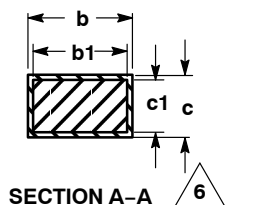
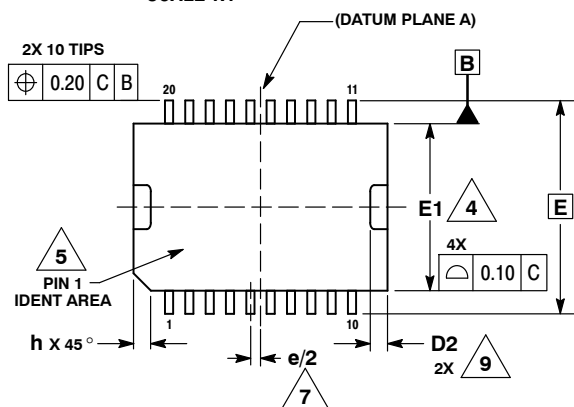
ON



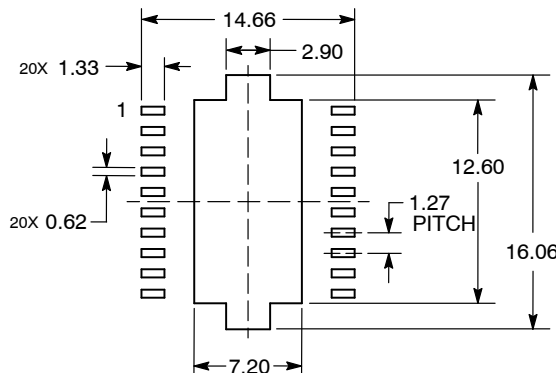
SCALE 1:1

PSOP-20
CASE 525AB-01
ISSUE B

DATE 14 SEP 2010



MOUNTING FOOTPRINT



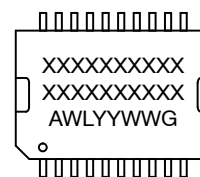
DIMENSIONS: MILLIMETERS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE LEAD AND IS COINCIDENT WITH THE LEAD WHERE IT EXITS THE BODY AT THE BOTTOM OF THE PARTING LINE.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. D IS DETERMINED AT DATUM H.
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH PROTRUSION. INTERLEAD FLASH PROTRUSION SHALL NOT EXCEED 0.15 PER SIDE. E1 IS DETERMINED AT DATUM H.
6. A VISUAL IDENTIFIER IS LOCATED WITHIN THE CROSS-HATCHED AREA.
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 AND 0.25mm FROM THE TIP.
8. SEATING PLANE IS DEFINED BY THE LEAD TIPS ONLY.
9. DIMENSION D DOES NOT INCLUDE TIEBAR PROTRUSIONS. TIEBAR PROTRUSIONS SHALL NOT EXCEED 0.15 PER SIDE.
10. DATUMS A AND B TO BE DETERMINED AT DATUM H.

DIM	MILLIMETERS	
	MIN	MAX
A	3.00	3.40
A1	0.10	0.30
A2	2.90	3.10
A3	0.00	0.10
b	0.40	0.52
b1	0.40	0.49
c	0.23	0.32
c1	0.23	0.28
D	15.90 BSC	
D1	11.70	12.60
D2	0.90	1.10
e	1.27 BSC	
E	13.95	14.45
E1	11.00 BSC	
E2	2.50	2.70
E3	6.40	7.20
E4	2.70	2.90
h	---	1.10
L	0.84	1.10
L1	0.35 BSC	
θ	0°	8°


GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

DOCUMENT NUMBER:	98AON34973E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
STATUS:	ON SEMICONDUCTOR STANDARD	
NEW STANDARD:		
DESCRIPTION:	PSOP-20	
		PAGE 1 OF 2

[illegible]

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.