



FINAL PRODUCT/PROCESS CHANGE NOTIFICATION #16416Generic Copy

03 Mar 2010

TITLE: Piestany to Oudenaarde Wafer Fabrication Transfer of NCP102**PROPOSED FIRST SHIP DATE:** 03 Jun 2010**AFFECTED CHANGE CATEGORY(S):** Manufacturing Transfer (Wafer Fabrication)**AFFECTED PRODUCT DIVISION:** Consumer and Computing Product Group, AC/DC BU**FOR ANY QUESTIONS CONCERNING THIS NOTIFICATION:**Contact your local ON Semiconductor Sales Office or Scott Brow < Scott.Brow@onsemi.com >**SAMPLES:** Contact your local ON Semiconductor Sales Office or Grant Floyd < grant.floyd@onsemi.com > or Scott Brow < Scott.Brow@onsemi.com > for the availability of samples.**ADDITIONAL RELIABILITY DATA:** Contact your local ON Semiconductor Sales Office or Ken Fergus < ken.fergus@onsemi.com >**NOTIFICATION TYPE:**

Final Product/Process Change Notification (FPCN)

Final change notification sent to customers. FPCNs are issued at least 90 days prior to implementation of the change.

ON Semiconductor will consider this change approved unless specific conditions of acceptance are provided in writing within 30 days of receipt of this notice. To do so, contact your local ON Semiconductor Sales Office.

DESCRIPTION AND PURPOSE:

The purpose of this final PCN is to notify customers of the qualification and production transfer of NCP102 device to ON Semiconductor Oudenaarde, Belgium.

Transfer is made due to the closure of ON Semiconductor's wafer fabrication facilities at Piestany, Slovakia Republic.

The Oudenaarde site is certified according to ISO/TS16949 standards.

The affected devices will continue to meet datasheet performance and are qualified in compliance with ON Semiconductor's quality standards.



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RELIABILITY DATA SUMMARY:

The product qualification vehicles were chosen to represent the broadest use of possible design library elements and available process modules. An automotive component, NCV7708, was selected as the technology qualification vehicle with reference to IPCN#16168. It has the largest die, complex design, high test coverage, historical data and in production. As announced in FPCN#16368, it has successfully completed the reliability requirement of the technology platform, fulfilling the generic qualification requirement of NCP102 device.

Other completed reliability data are also available from other devices if requested.

AEC Q100 IC Device Semiconductor Component Qualification Summary										AEC Q100 Rev G 2/07	
Supplier Name/Code: ON Semiconductor					Customer PIN:						
Supplier P/N: NCV7708DWR2G					Customer Comp. Eng. Sign.:						
Description: Double Hex Driver					Customer Gen. Qual Spec: AEC Q100 Rev G						
Supplier Contact:					Customer ID Number:						
Supplier Fab site: Fab2, P05B, (2.577 x 5.73)					Automotive Grade Level: Grade 1 (-40C to +125C)						
Supplier Assembly site: O8PI, 28L 80W 1, G6001084P2.0Au (2034)					PPAP Submission Date:					PT/Waz 01/10	
Reason for Qual:											
Results											
Test	#	Reference	Test Conditions	Comments	# Lots	S.S.	Fail/Total	Comments/ Test Results			
Test Group A- Accelerated Environment Stress Tests											
PC	A1	JESD22 A113	Preconditioning (Test @ RH) SMD only; Moisture Load and Reflow	Preconditioning for AC, TC, THB/HAST	all	all	0 / 720	For AC, TC, THB/HAST (MSL= 3 @ 260°C)			
THB	A2	JESD22 A104	Highly Accelerated Stress Test (Test @ R) 85°C/85% RH, bias, 1008hrs	Extended to T1250	3	80	0 / 240	Pass.			
AC	A3	JESD22 A102	Autoclave (Test @ R) 121°C/100% RH, 15 psi for 96 hrs		3	80	0 / 240	Pass.			
TC	A4	JESD22 A104	Temperature Cycle (Test @ R) -65°C to +150°C, for 500cycs		3	80	0 / 240	Pass.			
PTC	A5	JESD22 A105	Power Temperature Cycling (Test @ RH)		-	-	-	waived			
HTSL	A6	JESD22 A103	High Temperature Storage Life (Test @ RH) TA=150°C for 1008 hrs.	Extended to T2000	3	80	0 / 240	Pass.			
Test Group B- Accelerated LifeTime Simulation Tests											
HTOL	B1	JESD22 A108	High Temperature Operational Life (Test @ RH) Tj=150°C for 504hrs		3	160	0 / 480	Pass			
ELFR	B2	AEC-Q100-008	Early Life Fail Rate (Test @ RH) TA= 125°C for 48hrs		3	800	0 / 2400	Pass			
EDR	B3	AEC-Q100-005	NBV Endurance and Data Retention (Test @ RH)		-	-	-	n/a			
Test Group C- Package Assembly Integrity Test											
WBS	C1	AEC-Q100-001	Wire Bond Shear Test: Cpk > 1.33	In-line data per control plan	30 bonds	5 parts	0 / 90	Cpk>1.33			
WBP	C2	Method 2011	Wire Bond Pull: >3gr. Condition C, 0 fails or Cpk>1.33.		30 bonds	5 parts	0 / 90	Pass. > 3gr, Cpk>1.33			
SD	C3	JESD22 B102	Solderability, 8hr steam age, 245°C PbSn solder, >95% cov	Using 68140 (RMS0517)	3	15	0 / 45	Pass.			
PD	C4	JESD22 B1008	Physical Dimension	In-line data per control plan	3	10	0 / 30	Cpk>1.33			
SBS	C5	AEC-Q100-010	Solder Ball Shear (Ppk>1.67 and Cpk>1.33)		-	-	-	n/a			
LI	C6	Lead Integrity	Through Hole only		-	-	-	n/a			
Test Group D- Die Fab Reliability Tests											
EM	D1	JESD61	Electromigration	Reporting per J-P-001	-	-	-	Pass			
TDDB	D2	JESD35	Time Dependant Dielectric Breakdown	Reporting per J-P-001	-	-	-	Pass			
HCI	D3	JESD60 & 28	Hot Carrier Injection	Reporting per J-P-001	-	-	-	Pass			
NBTI	D4	JESD90	Negative Bias Temperature Instability	Reporting per J-P-001	-	-	-	Pass			
SM	D5	JESD61, 87, 202	Stress Migration	Reporting per J-P-001	-	-	-	Pass			
Test Group E- Electrical Verification											
Test	E1		Pre and Post Stress Electrical Test		All	All					
HBM	E2	AEC-Q100-002	Electrostatic Discharge, Human Body Model Machine Model		1	3/V level model	>>>	HBM - Pass 4kV, MM - Pass 200V			
CDM	E3	AEC-Q100-011	Electrostatic Discharge, Charge Device Model (Test @ RH)		1	per spec	>>>	CDM - Pass 1000V			
LU	E4	AEC-Q100-004	Latch-up (Test @ RH)		1	5	0 / 6	Pass, Class II, Level A			
ED	E5	AEC-Q100-009	Electrical Distribution (Test @ C / R / H)		3	30	>>>	Pass, Tri-Temp Cpk > 1.87			
FG	E6	AEC-Q100-007	Fault Grading		-	-	-	note			
CHAR	E7	AEC-Q103	Characterization (Test @ C / R / H)		-	-	-	note			
GL	E8	AEC-Q100-006	Electro-Thermally Induced Gate Leakage (Test @ R)		1	5	-	waived			
EMC	E9	SAE/J752/3	Electromagnetic Compatibility (Radiated Emissions)	Use DPI according to IEC61324-4 (7608)	1	1	-	Pass, 1MHz to 1GHz			
SC	E10	AEC-Q100-012	Short Circuit Characterization		1	10	-	Pass, Grade D			
SER	E11	JESD89	Soft Error rate		1	3	-	n/a			
Test Group F- Defect Screening Tests											
Test			Pre and Post Stress Electrical Test		All	All					
PAT	F1	AEC-Q001	Reject Units Outside of Average		All	All	>>>	note			
SBA	F2	AEC-Q002	Reject Units Outside Criteria		All	All	>>>	note			
Test Group G- Cavity Package Integrity Tests											
Test	G1 to G8		Pre and Post Stress Electrical Test	For Ceramic Package testing only	All	All		n/a			
Notes:											
PTC	A5	ON Semi does not use this test. PTC does not induce any failure mechanisms in ON Semi analog IC products that are also not accelerated by Temperature Cycling.									
HTOL	B1	Post stress HTOL testing is not performed at cold temperatures as it does not detect any failure mechanisms in ON Semi analog IC products that could only be detected at cold temperatures.									
GL	E8	GL testing is performed where applicable and is for information only.									
E6, F1, F2 Defect Screening Test methodologies are constantly evolving under the Continuous Improvement Initiatives. Testing and Characterization may include, but may not be necessarily limited to the AEC cited methodologies.											



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ELECTRICAL CHARACTERISTIC SUMMARY:

There is no change in the electrical performance. Datasheet specifications remain unchanged.

CHANGED PART IDENTIFICATION:

Affected products with date code WW24-2010 and greater may be sourced from Oudenaarde wafer fabrication site

List of affected General Parts:

NCP102SNT1G