



FINAL PRODUCT/PROCESS CHANGE NOTIFICATIONGeneric Copy

16 Apr 2008**SUBJECT: ON Semiconductor Final Product/Process Change Notification #16113****TITLE: Die replacement and Manufacturing flow change for ADP3120A, ADP3110A, and ADP3118****PROPOSED FIRST SHIP DATE: 16 Jul 2008****AFFECTED CHANGE CATEGORY(S): Die, Wafer Fab Process/Location; Assembly/Test Site Change****AFFECTED PRODUCT DIVISION(S): Computing Products group****FOR ANY QUESTIONS CONCERNING THIS NOTIFICATION:**Contact your local ON Semiconductor Sales Office or <david.chu@onsemi.com>**SAMPLES:** Contact your local ON Semiconductor Sales Office or <david.chu@onsemi.com>**ADDITIONAL RELIABILITY DATA:** AvailableContact your local ON Semiconductor Sales Office or <m.wasilewski@onsemi.com>**NOTIFICATION TYPE:**

Final Product/Process Change Notification (FPCN)

Final change notification sent to customers. FPCNs are issued at least 90 days prior to implementation of the change.

ON Semiconductor will consider this change approved unless specific conditions of acceptance are provided in writing within 30 days of receipt of this notice. To do so, contact your local ON Semiconductor Sales Office.

DESCRIPTION AND PURPOSE:This is a Final Process Change Notice to IPCN 16103 located at www.onsemi.com

- ON Semiconductor has acquired the voltage regulation and thermal monitoring products (ADI-PTC) for computing applications from Analog Devices, Inc. Analog Devices will continue to provide the subject products for a limited time period.
- To eliminate supply constraints for the subject products and integrate product manufacturing flow into ON systems.
- The subject products will have change in die process technology and location as well as assembly /test locations. It is believed that the products will continue to meet (or exceed) the current device specifications and that functionality there will be no difference in performance; however samples may be requested for verification.
- As part of the assembly/test location changes, the package outline from LFCSP to DFN changes slightly, but the solderable footprint for board placement is the same.



Final Product/Process Change Notification #16113

RELIABILITY DATA SUMMARY:

Design/Process/Package Technology is qualified via NCP5359 qual data.

TEST	CONDITIONS	Time	Sample Size	# of Lots	Results
HTOL	Ta=125C 504,	1008 Hrs	84	3	0/252
AutoClave	121 C; 100% RH 15 PSIG	96 Hrs	84	3	0/252
HAST	Ta=130C; 85% RH 18.8 PSIG	96 Hrs	84	3	0/252
ESD					
HBM and MM	1Kv and 100v		27	1	Pass
LU	Latch Up		6	1	Pass

ELECTRICAL CHARACTERISTIC SUMMARY:

Characterization data is available upon request. Parametric and bench evaluations indicate material conforms to required performance in accordance with the datasheet specification for the most parameters exception listed as noted below (exceptions noted in red).

UNLESS OTHERWISE NOTED, VCC = 12V, TA = 0 - 85C

Condition		ADP3120A			NEW ADP3120A			ADP3110A			NEW ADP3110A			ADP3118			NEW ADP3118		
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
HIGH-SIDE DRIVER																			
- Output Resistance, Sourcing Current	Ta = 25°C	-	-	3.3 Ω			3.3 Ω	-	2.6 Ω	3.4 Ω									
	Ta = 0°C to 85°C	-	2.5	3.9 Ω	-	2.2	3.9 Ω				-	2.2	3.4 Ω	-	2.2 Ω	3.5 Ω	-	1.8 Ω	3.5 Ω
- Output Resistance, Sinking Current	Ta = 25°C	-	-	1.8 Ω			1.8 Ω	-	1.4 Ω	1.8 Ω									
	Ta = 0°C to 85°C	-	1.4	2.6 Ω	-	1.0	2.6 Ω				-	1.0	1.8 Ω	-	1.0 Ω	2.5 Ω	-	1.0 Ω	2.5 Ω
- Output Resistance, Unbiased		-	10k	-	-	15 kΩ	-	-	10k	-	-	15 kΩ	-	-	10k	-	-	15 kΩ	-
- Transition Time, trDRVH		-	25 ns	40 ns	-	20ns	40 ns	-	40 ns	55 ns	-	20ns	55 ns	-	25 ns	40 ns	-	16 ns	40 ns
- Transition Time, tfDRVH		-	20 ns	30 ns	-	11 ns	30 ns	-	30 ns	45 ns	-	11 ns	45 ns	-	20 ns	30 ns	-	11 ns	30 ns
- Propagation Delay, tpdhDRVH*	25°C ≤ Ta ≤ 85°C	32 ns	45 ns	70 ns															
	Ta = 25°C							-	45 ns	65 ns									
	Ta = 0°C to 85°C				32 ns	45 ns	70 ns				32 ns	45 ns	70 ns	-	25 ns	40 ns		25 ns	40 ns
- Propagation Delay, tpdIDRVH		-	25 ns	35 ns	25ns		35 ns	-	25 ns	35 ns	25ns		35 ns	-	25 ns	35 ns	25 ns		35 ns
- Propagation Delay, tpdIOD_		-	20 ns	35 ns	20 ns		35 ns	-	20 ns	35 ns	20 ns		35 ns	-	20 ns	35 ns	20 ns		35 ns
- Propagation Delay, tpdhOD_		-	40 ns	55 ns	25 ns		55 ns	-	40 ns	55 ns	25 ns		55 ns	-	40 ns	55 ns	25 ns		55 ns
- SW Pull-Down Resistance		-	10k	-	-	15 kΩ	-	-	10k	-	-	15 kΩ	-	-	10k	-	-	15 kΩ	-



Final Product/Process Change Notification #16113

Condition		ADP3120A			NEW ADP3120A			ADP3110A			NEW ADP3110A			ADP3118			NEW ADP3118		
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
LOW-SIDE DRIVER																			
- Output Resistance, Sourcing Current	Ta = 25°C	-	-	3.3 Ω				-	2.5 Ω	3.4 Ω									
	Ta = 0°C to 85°C	-	2.4 Ω	3.9 Ω	-	1.8 Ω	3.9 Ω				-	1.8 Ω	3.4 Ω	-	2.0 Ω	3.2 Ω	-	1.8 Ω	3.2 Ω
- Output Resistance, Sinking Current	Ta = 25°C	-	-	1.8 Ω				-	1.4 Ω	1.8 Ω									
	Ta = 0°C to 85°C	-	1.4 Ω	2.6 Ω	-	1.0 Ω	2.6 Ω				-	1.0 Ω	1.8 Ω	-	1.0 Ω	2.5 Ω	-	1.0 Ω	2.5 Ω
- Output Resistance, Unbiased		-	10k	-	-	15 kΩ	-	-	10k	-	-	15 kΩ	-	-	10 kΩ	-	-	15 kΩ	-
- Transition Time, trDRV1		-	20 ns	35 ns	-	16 ns	35 ns	-	40 ns	50 ns	-	16 ns	50 ns	-	20 ns	35 ns	-	16 ns	35 ns
- Transition Time, tfDRV1		-	16 ns	30 ns	-	11 ns	30 ns	-	20 ns	30 ns	-	11 ns	30 ns	-	16 ns	30 ns	-	11 ns	30 ns
- Propagation Delay, tpdhDRV1**		-	12 ns	35 ns	-	12 ns	35 ns	-	15 ns	35 ns	-	12 ns	35 ns	-	12 ns	35 ns	-	12 ns	35 ns
- Propagation Delay, tpdIDRV1		-	30 ns	45 ns	-	15 ns	45 ns	-	30 ns	40 ns	-	15 ns	40 ns	-	30 ns	45 ns	-	15 ns	45 ns
- Propagation Delay, tpdIOD_		-	20 ns	35 ns	-	20 ns	35 ns	-	20 ns	35 ns	-	20 ns	35 ns	-	20 ns	35 ns	-	20 ns	35 ns
- Propagation Delay, tpdhOD_		110 ns	190 ns	-	-	20 ns	35 ns	110 ns	190 ns	-	-	20 ns	35 ns	-	40 ns	55 ns	-	20 ns	55 ns
- Timeout Delay	SW = 5 V	110 ns	190 ns	-				110 ns	190 ns	-				110 ns	190 ns	-			
	SW = PGND	95 ns	150 ns	-				95 ns	150 ns	-				95 ns	150 ns	-			
	DRVH-SW = 0	ns	ns	-	-	85 ns	-	-	85 ns	-	-	85 ns	-	-	85 ns	-	-	85 ns	-
SUPPLY																			
- Supply Voltage Range		4.15 V	-	13.2 V	4.6 V	-	13.2 V	4.15 V	-	13.2 V	4.6 V	-	13.2 V	4.15 V	-	13.2 V	4.6 V	-	13.2 V
- Supply Current		-	2 mA	5 mA	-	0.7 mA	5 mA	-	2 mA	5 mA	-	0.7 mA	5 mA	-	2 mA	5 mA	-	0.7 mA	5 mA
- UVLO Voltage	Startup	1.5 V	-	3.0 V				1.5 V	-	3.0 V				1.5 V	-	3.0 V			
- UVLO Voltage					4.1 V	4.3 V	4.5 V				4.1 V	4.3 V	4.5 V				4.1 V	4.3 V	4.5 V
- UVLO Voltage					3.9 V	4.1 V	4.3 V				3.9 V	4.1 V	4.3 V				3.9 V	4.1 V	4.3 V
- Hysteresis		-	350 mV	-	0.1 V	0.2 V	0.4 V	-	350 mV	-	0.1 V	0.2 V	0.4 V	-	350 mV	-	0.1 V	0.2 V	0.4 V
OD_ INPUT																			
- Input Voltage High		2.0 V	-	-	2.0 V	-	-	2.0 V	-	-	2	-	-	2.0 V	-	-	2	-	-
- Input Voltage Low		-	-	0.8 V	-	-	0.8 V	-	-	0.8 V	-	-	0.8	-	-	0.8 V	-	-	0.8
- Input Current		-1 μA	-	+1 μA	-1 μA	-	+1 μA	-1 μA	-	+1 μA	-1 μA	-	+1 μA	-1 μA	-	+1 μA	-1 μA	-	+1 μA
- Hysteresis		90 mV	250 mV	-	-	400 mV	-	90 mV	250 mV	-	-	400 mV	-	90 mV	250 mV	-	-	400 mV	-
PWM INPUT																			
- Input Voltage High		2.0 V	-	-	2.0 V	-	-	2.0 V	-	-	2	-	-	2.0 V	-	-	2	-	-
- Input Voltage Low		-	-	0.8 V	-	-	0.8 V	-	-	0.8 V	-	-	0.8	-	-	0.8 V	-	-	0.8
- Input Current		-1 μA	-	+1 μA	-1 μA	-	+1 μA	-1 μA	-	+1 μA	-1 μA	-	+1 μA	-1 μA	-	+1 μA	-1 μA	-	+1 μA
- Hysteresis		90 mV	250 mV	-	-	400 mV	-	90 mV	250 mV	-	-	400 mV	-	90 mV	250 mV	-	-	400 mV	-

Notes:

* tpdhDRVH originally measured from falling edge of DRV1 (10%) to rising edge of DRVH-SW (10%). New data reflects measurement from falling edge of DRV1 (2V) to rising edge of DRVH-SW (10%).

** tpdhDRV1 originally measured from falling edge of SW (1V) to the rising edge of DRV1 (10%). New data reflects measurement from falling edge of DRVH-SW (2V) to rising edge of DRV1 (10%).

**Final Product/Process Change Notification #16113****CHANGED PART IDENTIFICATION:**

Product with a Finished Good Date Code of 0826 or newer may be new die process technology and location as well as assembly / test location. The product affected by the change will not have ADI logo and the new product will be differentiated via micro dot (·) as opposed to (#).

AFFECTED DEVICE LIST

ADP3110A0001RZR
ADP3110AKCPZ-RL
ADP3110AKRZ
ADP3110AKRZ-RL
ADP3118JCPZ-RL
ADP3118JRZ
ADP3118JRZ-RL
ADP3120AJCPZ-RL
ADP3120AJRZ
ADP3120AJRZ-RL